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ภาคผนวก

Synertek.

SY6500

8-Bit Microprocessor Family

Features

- Single 5 V ±5% power supply
- N channel, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable interrupt
- Use with any type or speed memory
- Bi-directional Data Bus

- Instruction decoding and control
- Addressable memory range of up to 65 K bytes
- "Ready" input
- Direct memory access capability
- Bus compatible with MC6800
- Choice of external or on-board clocks
- 1 MHz, 2 MHz, 3 MHz and 4 MHz operation
- On-chip clock options
  * External single clock input
  * Crystal time base input
- 40 and 28 pin package versions
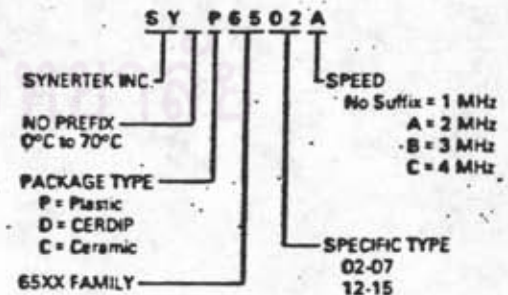- Pipeline architecture

Description

The SY6500 Series Microprocessors represent the first totally software compatible microprocessor family. This family of products includes a range of software compatible microprocessors which provide a selection of addressable memory range, interrupt input options and on-chip clock oscillators and drivers. All of the microprocessors in the SY6500 family are software compatible within the group and are bus compatible with the MC6800 product offering.

The family includes six microprocessors with on-board clock oscillators and drivers and four microprocessors driven by external clocks. The on-chip clock versions are aimed at high performance, low cost applications where single phase inputs or crystals provide the time base. The external clock versions are geared for the multi-processor system applications where maximum timing control is mandatory. All versions of the microprocessors are available in 1 MHz, 2 MHz, 3 MHz and 4 MHz maximum operating frequencies.

Members of the Family

PART NUMBERS	CLOCKS	PINS	IRQ	NMI	RYD	ADDRESSING
SY6502	On-Chip	40	✓	✓	✓	64 K
SY6503	"	28	✓	✓		4 K
SY6504	"	28	✓			8 K
SY6505	"	28	✓		✓	4 K
SY6506	"	28	✓			4 K
SY6507	"	28			✓	8 K
SY6512	External	40	✓	✓	✓	64 K
SY6513	"	28	✓	✓		4 K
SY6514	"	28	✓			8 K
SY6515	"	28	✓		✓	4 K

Ordering Information

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          S Y  P 6 5 0 2 A
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SYNERTEK INC.

NO PREFIX
0°C to 70°C

PACKAGE TYPE
P = Plastic
D = CERDIP
C = Ceramic

65XX FAMILY

SPEED
No Suffix = 1 MHz
A = 2 MHz
B = 3 MHz
C = 4 MHz

SPECIFIC TYPE
02-07
12-15

Only 6502 and E512 are available in 3 and 4 MHz

Synertek.

SY6500

Comments on the Data Sheet

The data sheet is constructed to review first the basic "Common Characteristics" — those features which are common to the general family of microprocessors. Subsequent to a review of the family characteristics will be sections devoted to each member of the group with specific features of each.

SY6500 Internal Architecture
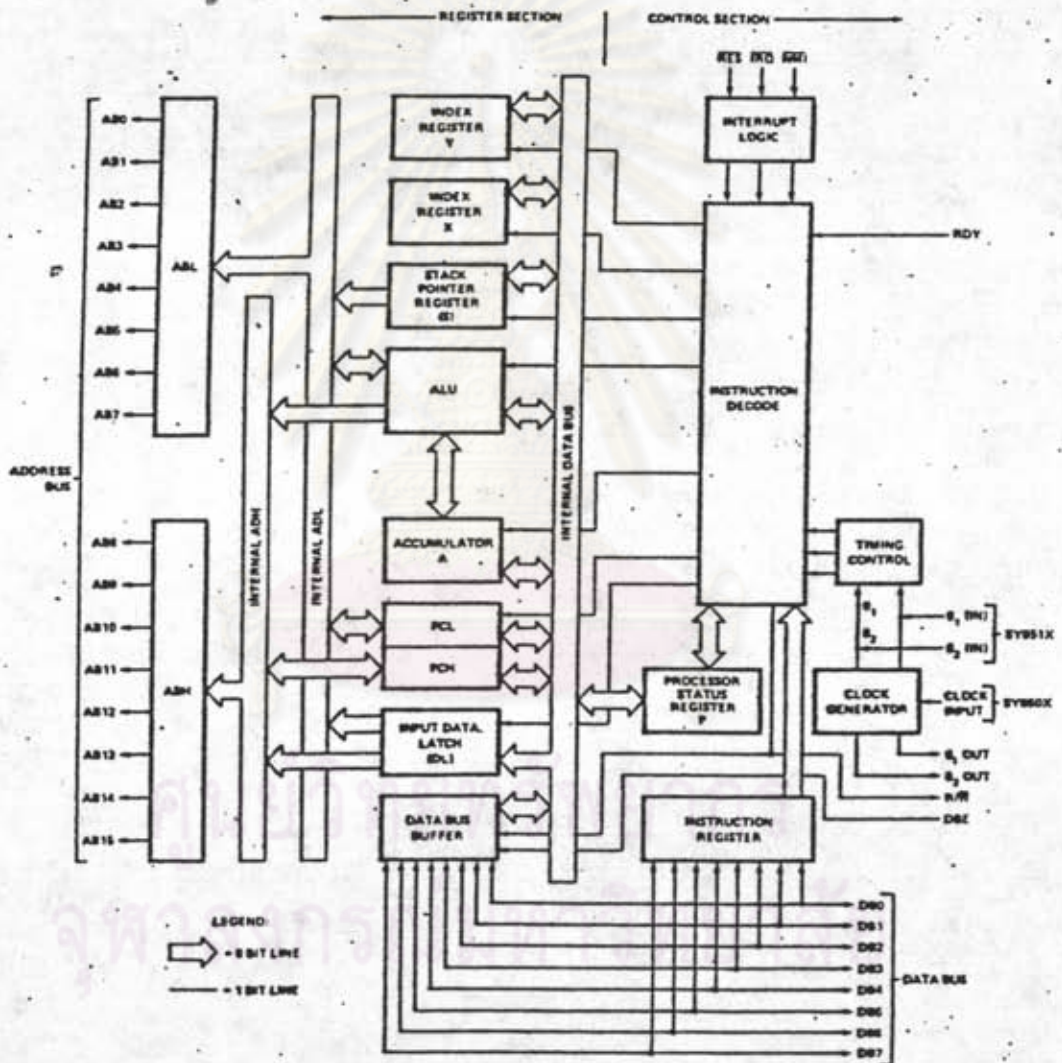
NOTE:
1. CLOCK GENERATOR IS NOT INCLUDED ON SY6512X
2. ADDRESSING CAPABILITY AND CONTROL OPTIONS VARY WITH EACH OF THE SY6500 PRODUCTS.

Synertek.

Absolute Maximum Ratings*

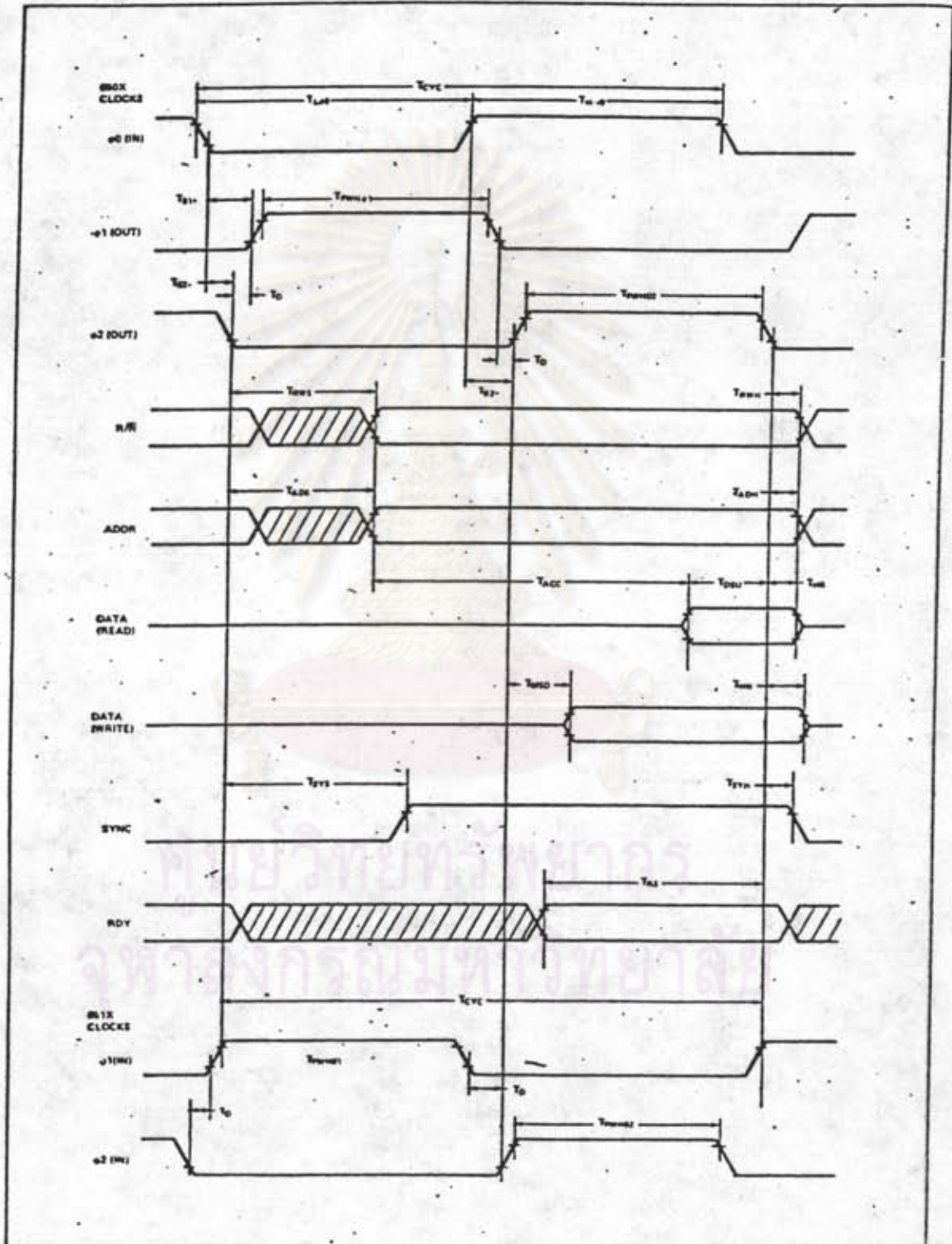| Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage	V_{in}	−0.3 to +7.0	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

Comment*

This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

D.C. Characteristics (V_{CC} = 5.0V ±5%, T_A = 0-70°C)

(θ_1, θ_2 applies to SY651X, $\theta_{o(in)}$ applies to SY650X)

Symbol	Characteristic		Min.	Max.	Unit
V_{IH}	Input High Voltage Logic and θ_o (in) for all 650X devices	1,2,3 MHz	+2.0	V_{CC}	V
		4 MHz	+3.3	V_{CC}	V
	θ_1 and θ_2 only for all 651X devices. Logic as 650X	All Speeds	V_{CC} −0.5	V_{CC} + 0.25	V
V_{IL}	Input Low Voltage				
	Logic, $\theta_{o(in)}$ (650X)		−0.3	+0.8	
	θ_1, θ_2 (651X)		−0.3	+0.2	V
I_{IL}	Input Loading (V_{in} = 0 V, V_{CC} = 5.25 V) RDY, S.O.		−10	−300	μA
I_{in}	Input Leakage Current (V_{in} = 0 to 5.25 V, V_{CC} = 0)				
	Logic (Excl. RDY, S.O.)		—	2.5	μA
	θ_1, θ_2 (651X)		—	100	μA
	$\theta_{o(in)}$ (650X)		—	10.0	μA
I_{TSI}	Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 V, V_{CC} = 5.25 V) DB0-DB7		—	±10	μA
V_{OH}	Output High Voltage (I_{LOAD} = −100μAdc, V_{CC} = 4.75 V) SYNC, DB0-DB7, A0-A15, R/$\overline{W}$	1,2,3 MHz	2.4	—	V
		4 MHz	2.0	—	V
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mAdc, V_{CC} = 4.75 V) SYNC, DB0-DB7, A0-A15, R/$\overline{W}$	1,2,3 MHz	—	0.4	V
		4 MHz	—	0.8	V
P_D	Power Dissipation (V_{CC} = 5.25V)	1 MHz and 2 MHz	—	700	mW
		3 MHz	—	800	mW
		4 MHz	—	900	mW
C	Capacitance (V_{in} = 0, T_A = 25°C, f = 1 MHz)				
C_{in}	$\overline{RES}$, $\overline{NMI}$, RDY, $\overline{IRQ}$, S.O., DBE		—	10	
	DB0-DB7		—	15	
C_{out}	A0-A15, R/$\overline{W}$, SYNC		—	12	pF
$C_{\theta_{o(in)}}$	$\theta_{o(in)}$ (650X)		—	15	
C_{θ_1}	θ_1 (651X)		—	50	
C_{θ_2}	θ_2 (651X)		—	80	

Synertek.

SY6500

8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel® Microprocessor Families
- Improved Timing Characteristics

- Direct Bit Set/Reset Capability Easing Control Application Interface
- Reduces System Package Count
- Improved DC Driving Capability
- Available in EXPRESS
  —Standard Temperature Range
  —Extended Temperature Range

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.
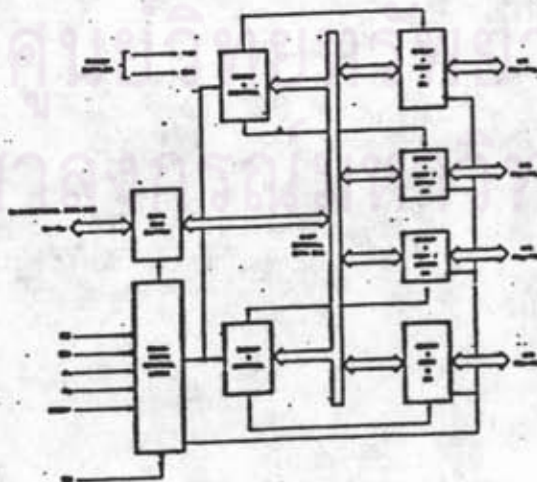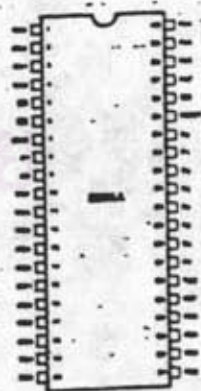

Figure 1. 8255A Block Diagram

Figure 2. Pin Configuration

intel   8255A/8255A-5

8255A FUNCTIONAL DESCRIPTION

General

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

(CS)

Chip Select. A "low" on this input pin enables the communiction between the 8255A and the CPU.

(RD)

Read. A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

(WR)

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

(A0 and A1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

8255A BASIC OPERATION

A_1	A_0	RD	WR	CS	INPUT OPERATION (READ)
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS → 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS → 3-STATE
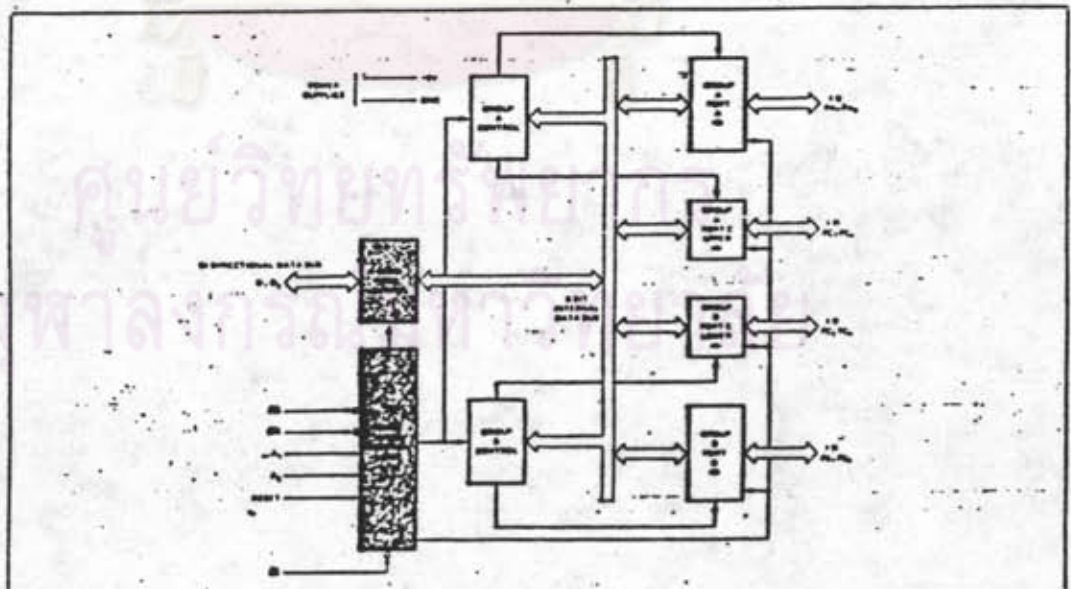
Figure 3. 8255A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions

intel 8255A/8255A-5

(RESET)

Reset. A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

  Control Group A – Port A and Port C upper (C7-C4)
  Control Group B – Port B and Port C lower (C3-C0)

The Control Word Register can Only be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

Port A. One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.
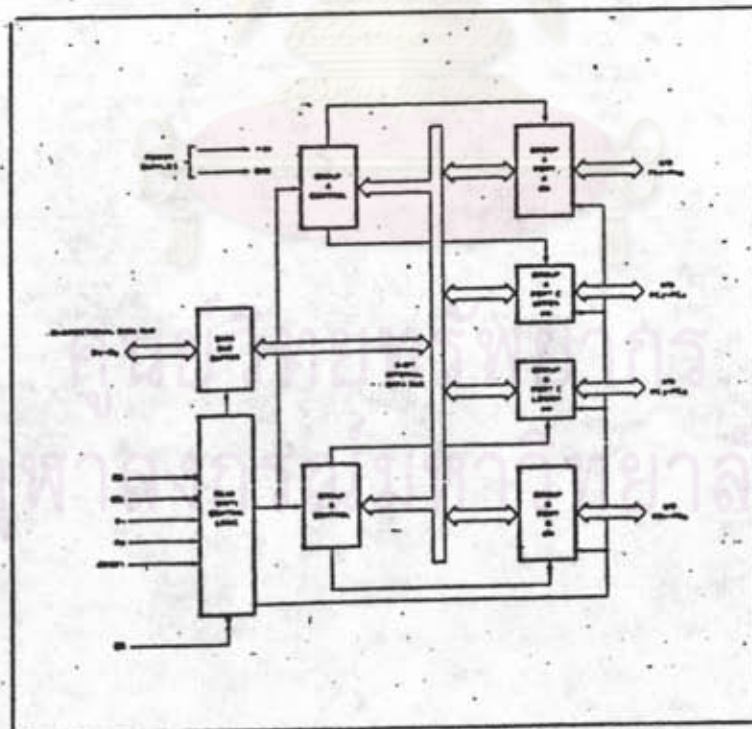

PIN CONFIGURATION

PIN NAMES

D₇-D₀	DATA BUS (BIDIRECTIONAL)
RESET	RESET INPUT
CS	CHIP SELECT
RD	READ INPUT
WR	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
Vcc	+5 VOLTS
GND	0 VOLTS

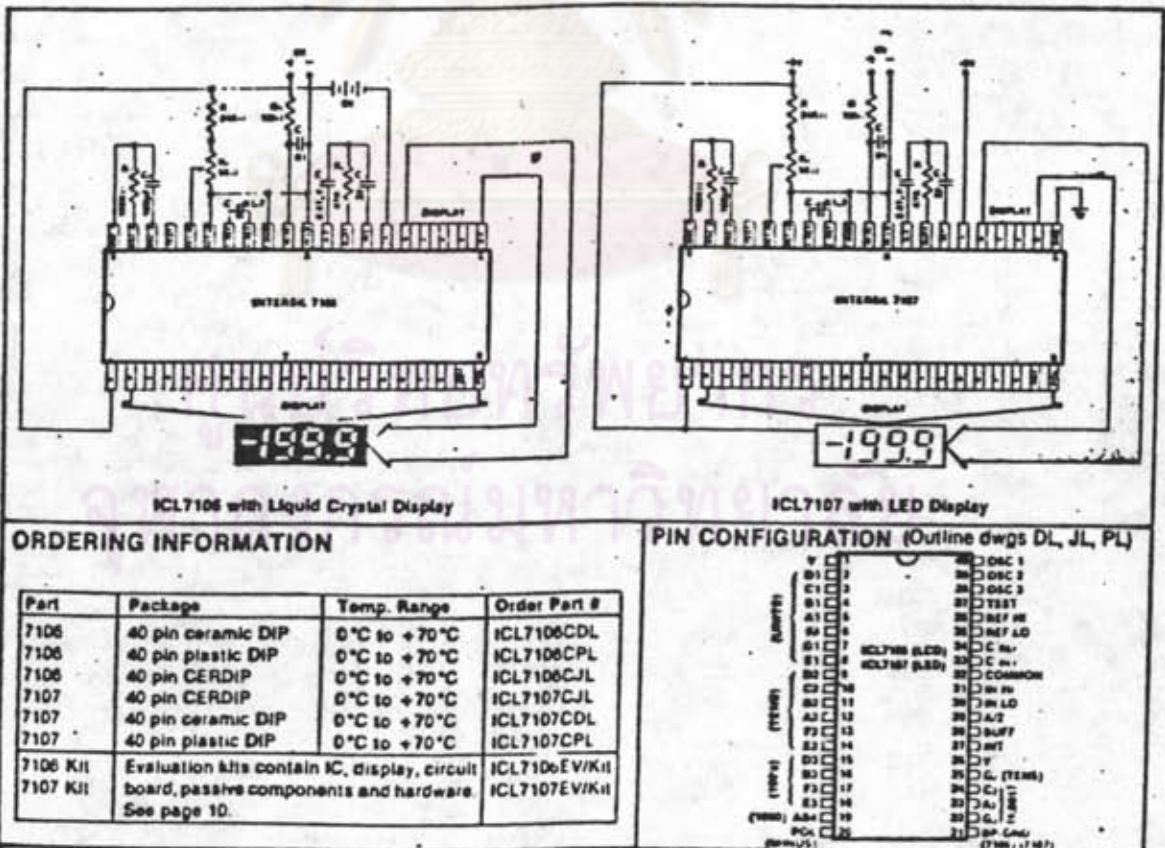Figure 4. 8225A Block Diagram Showing Group A and
Group B Control Functions

FEATURES

- Guaranteed zero reading for 0 volts input on all scales.
- True polarity at zero for precise null detection.
- 1 pA typical input current.
- True differential input and reference.
- Direct display drive - no external components required. — LCD ICL7106
  — LED ICL7107
- Low noise - less than 15µV p-p.
- On-chip clock and reference.
- Low power dissipation - typically less than 10mW.
- No additional active circuits required.
- Evaluation Kit available.

GENERAL DESCRIPTION

The Intersil ICL7106 and 7107 are high performance, low power 3-1/2 digit A/D converters containing all the necessary active devices on a single CMOS I.C. Included are seven-segment decoders, display drivers, reference, and a clock. The 7106 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7107 will directly drive an instrument-size light emitting diode (LED) display.

The 7106 and 7107 bring together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy like auto-zero to less than 10µV, zero drift of less than 1µV/°C, input bias current of 10 pA max., and roll-over error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation (7106), enabling a high performance panel meter to be built with the addition of only 7 passive components and a display.

ICL7106 with Liquid Crystal Display

ICL7107 with LED Display

ORDERING INFORMATION

Part	Package	Temp. Range	Order Part #
7106	40 pin ceramic DIP	0°C to +70°C	ICL7106CDL
7106	40 pin plastic DIP	0°C to +70°C	ICL7106CPL
7106	40 pin CERDIP	0°C to +70°C	ICL7106CJL
7107	40 pin CERDIP	0°C to +70°C	ICL7107CJL
7107	40 pin ceramic DIP	0°C to +70°C	ICL7107CDL
7107	40 pin plastic DIP	0°C to +70°C	ICL7107CPL
7106 Kit	Evaluation kits contain IC, display, circuit board, passive components and hardware. See page 10.		ICL7106EV/Kit
7107 Kit			ICL7107EV/Kit

PIN CONFIGURATION (Outline dwgs DL, JL, PL)

ICL7106/ICL7107

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V⁺)
ICL7106 .... 15V
ICL7107 .... +6V
Supply Voltage (V⁻)
ICL7106 .... 15V
ICL7107 .... −9V
Analog Input Voltage (either input) (Note 1) ..... V⁺ to V
Reference Input Voltage (either input) .... V⁺ to V⁻
Clock Input
ICL7106 .... Test to V⁺
ICL7107 .... Gnd to V⁺

Power Dissipation (ICL7106 Note 2; ICL7107 Note 1)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature .... 0°C to +70°C
Storage Temperature .... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) .... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF} V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$-V_{IN}$ = $+V_{IN}$ = 200.0mV	−1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V. Full Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current	Input	V_{IN} = 0		1	10	pA
Zero Reading Drift	V_{IN} = 0 0° < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° < T_A < 70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
V⁺ Supply Current (Does not include LED current for 7107)	V_{IN} = 0		0.8	1.8	mA
V⁻ Supply Current (7107 only)			0.6	1.8	mA
Analog Common Voltage (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply		80		ppm/°C
7106 ONLY Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage (Note 5)	V⁺ to V⁻ = 9V	4	5	6	V
7107 ONLY Segment Sinking Current (Except Pin 19)	V⁺ = 5.0V Segment voltage = 3V	5	8.0		mA
(Pin 19 only)		10	16		mA

Note 3: Unless otherwise noted, specifications apply to both the 7106 and 7107 at T_A = 25°C, f_{clock} = 48kHz. 7106 is tested in the circuit of Figure 1. 7107 is tested in the circuit of Figure 2.

Note 4: Refer to "Differential Input" discussion below.

Note 5: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
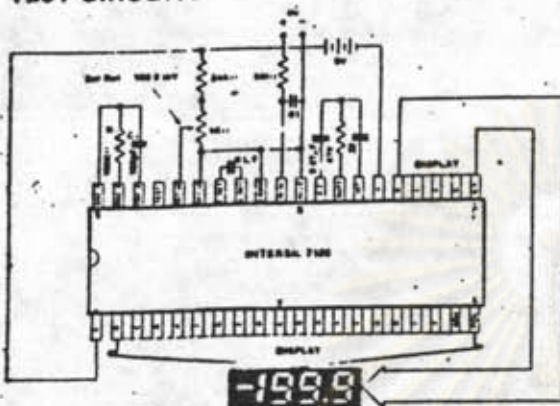
ICL7106/ICL7107
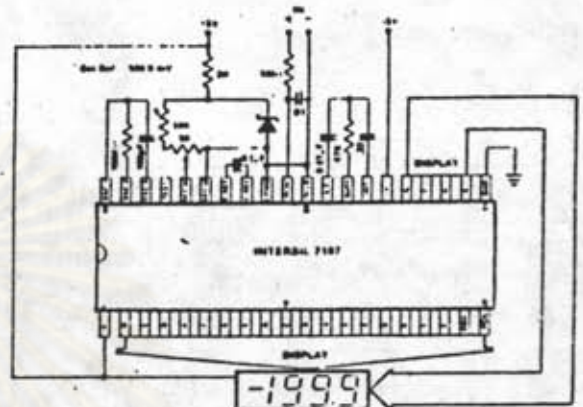
TEST CIRCUITS

Figure 1: 7106

Figure 2: 7107

DETAILED DESCRIPTION
ANALOG SECTION

Figure 3 shows the Block Diagram of the Analog Section for the ICL 7106 and 7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) deintegrate (DE).
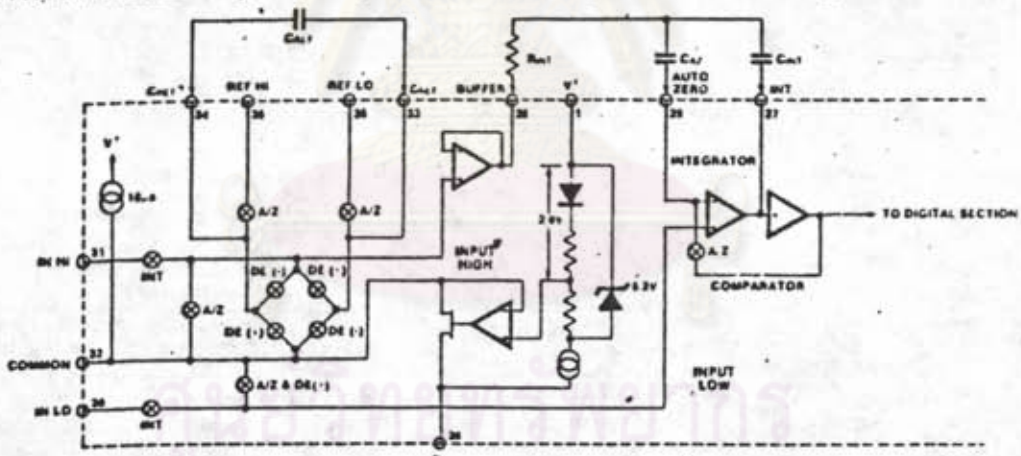

Figure 3: Analog Section of 7106/7107

1. Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. Signal integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range, within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is 1000 $\left(\frac{V_{IN}}{V_{REF}}\right)$.

ⓂMOTOROLA

DESCRIPTION — The SN54LS/74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high impedence state.

The SN54LS/74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN54LS/74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all Motorola TTL families.

● EIGHT LATCHES IN A SINGLE PACKAGE
● 3-STATE OUTPUTS FOR BUS INTERFACING
● HYSTERESIS ON LATCH ENABLE
● EDGE-TRIGGERED D-TYPE INPUTS
● BUFFERED POSITIVE EDGE-TRIGGERED CLOCK
● HYSTERESIS ON CLOCK INPUT TO IMPROVE NOISE MARGIN
● INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
D_0-D_7	Data Inputs	0.5 U.L.	0.25 U.L.
LE	Latch Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH going edge) Input	0.5 U.L.	0.25 U.L.
OE	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
O_0—O_7	Outputs (Note b)	65(25)U.L.	15(7.5) U.L.

NOTES:
a 1 TTL Unit Load (U.L.) = 40 μA HIGH /1.6 mA LOW
b The Output LOW drive factor is 7.5 U.L. for Military and 25 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.
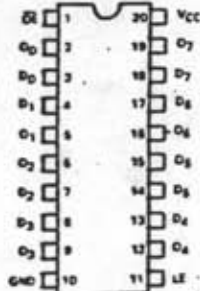
SN54LS/74LS373
SN54LS/74LS374

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS;

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

LOW POWER SCHOTTKY

CONNECTION DIAGRAM
DIP (TOP VIEW)

SN54LS/74LS373

CONNECTION DIAGRAM
DIP (TOP VIEW)

SN54LS/74LS374

J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-01 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

TRUTH TABLE

LS373

Dn	LE	$\overline{OE}$	On
H	H	L	H
L	H	L	L
X	X	H	Z*

LS374

Dn	CP	$\overline{OE}$	On
H	⌐	L	H
L	⌐	L	L
X	X	H	Z*

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

*Note: Consists of flip-flops unaffected by the state of the Output Enable input (OE)

LOGIC DIAGRAMS

SN54LS/74LS373
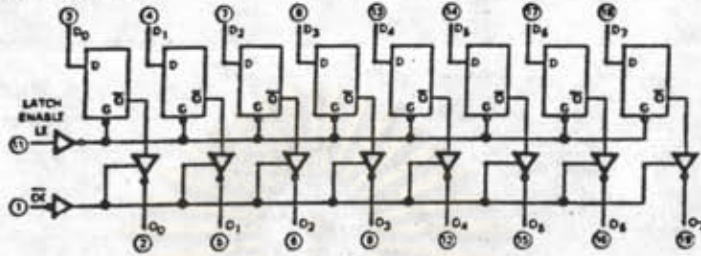
SN54LS/74LS374
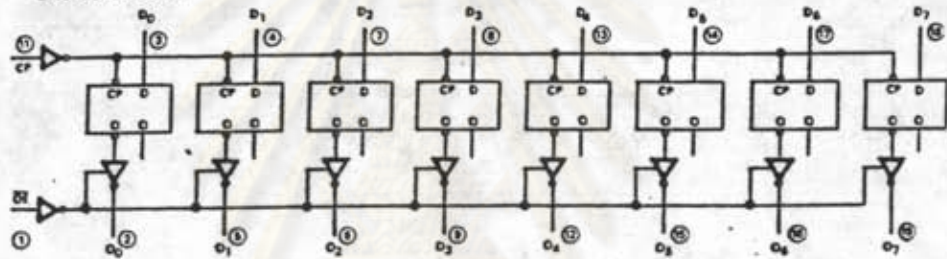
V_{CC} = Pin 20
GND = Pin 10
○ = Pin Numbers

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54			−1.0	mA
		74			−2.6	
I_{OL}	Output Current — Low	54			12	mA
		74			24	

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS	
			MIN	TYP	MAX			
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			-0.65	-1.5	V	V_{CC} = MIN, I_{IN} = -18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.4	3.1		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V	
I_{OZL}	Output Off Current LOW				-20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				-0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		-30		-130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				40	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS						UNITS	TEST CONDITIONS
		LS373			LS374				
		MIN	TYP	MAX	MIN	TYP	MAX		
f_{MAX}	Maximum Clock Frequency				35	50		MHz	
t_{PLH}	Propagation Delay, Data to Output		12	18				ns	C_L = 45 pF,
t_{PHL}			12	18					R_L = 667 Ω
t_{PLH}	Clock or Enable to Output		20	30		15	28	ns	
t_{PHL}			18	30		19	28		
t_{PZH}	Output Enable Time		15	28		20	28	ns	
t_{PZL}			25	36		21	28		
t_{PHZ}	Output Disable Time		12	20		12	20	ns	C_L = 5.0 pF
t_{PLZ}			15	25		15	25		

AC SETUP REQUIREMENTS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS				UNITS
		LS373		LS374		
		MIN	MAX	MIN	MAX	
t_W	Clock Pulse Width	15		15		ns
t_s	Setup Time	50		20		ns
t_h	Hold Time	20		0		ns

DEFINITION OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs

HOLD TIME (t_h) — is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

MOTOROLA SCHOTTKY TTL DEVICES

โปรแกรมที่ใช้ควบคุมการทดลอง

```
10   INPUT "number of detection?";M
20   DIM F(M),G(M),H(M),V(M),T(M),C(M),B(M),K(M),D(M *
     2),U(30 * M),SUM(3 * M)
30   INPUT "resistance?";Y
40   INPUT "average cond.at room temp.?";E
50   INPUT "room temp?";R
55   INPUT "period of mesurement in minute?";S
57 S = S * 60
58 R = R * .04
60   A = 49312:B = A + 1:C = A + 2:D = A + 3
70   POKE D,155
71   FOR T = 1 TO 39: PRINT "-";: NEXT T
73   PRINT
75   PRINT " cond"; TAB( 12);"kelvin"; TAB( 20);"log.c
     ond"; TAB( 30);"kel^-.25 "
76   PRINT
77   FOR T = 1 TO 39: PRINT "-";: NEXT T
78   PRINT
80   FOR I = 1 TO M
85   POKE 49664,3
87   FOR J = 1 TO 800: NEXT :SUM(I) = 0
88   FOR Q = 1 TO 10
90   GOSUB 140:U(Q) =  - N * (P0 * 100 + P1 * 10 + P2 +
     P3 / 10)
91 SUM(I) = SUM(I) + U(Q): NEXT Q:F(I) = SUM(I) / 10:
     PRINT F(I):F(I) =  - .0838667 + .1031025 * F(I)
92 F(I) = F(I) - .22:F(I) =  INT (F(I) / .01 + .5) *
     .01: PRINT "thermocouple   = ";F(I);"mV": GOTO 8
     0
94   POKE 49680,6
95   FOR J = 1 TO 800: NEXT
97 SUM(I) = 0
100   FOR Q = 1 TO 10
110   GOSUB 140:U(Q) =  - N * (P0 * 100 + P1 * 10 + P2
     + P3 / 10) / 10
111 SUM(I) = SUM(I) + U(Q): NEXT Q:G(I) = SUM(I) / 10
112 G(I) = G(I) - .2 + .752
113   PRINT "current        = ";G(I);"  mA"
114   POKE 49696,5
115   FOR J = 1 TO 800: NEXT
116 SUM(I) = 0
117   FOR Q = 1 TO 10
120   GOSUB 140:U(Q) =  - N * (P0 * 100 + P1 * 10 + P2
     + P3 / 10) / 10
121 SUM(I) = SUM(I) + U(Q): NEXT Q:H(I) = SUM(I) / 10
```

```
122 H(I) = H(I) + .19 + .16 + .049
125   PRINT "voltage            = ";H(I);"    mV"
135   PRINT
137   GOTO 1030
140 P1 =   PEEK (A):P2 =   PEEK (B):P3 =   PEEK (C)
150 X = P2: GOSUB 200:P2 = X
160 X = P3: GOSUB 200:P3 = X
165   IF P1 >  = 192 THEN 220
170   IF P1 >  = 128 THEN 230
180   IF P1 >  = 64 THEN 240
185 P0 = 1:N =  - 1:X = P1: GOSUB 200:P1 = X
190   RETURN
200   IF X = 0 THEN X = 8
201   IF X = 2 THEN X = 0
202   IF X = 36 THEN X = 2
203   IF X = 5 THEN X = 3
204   IF X = 9 THEN X = 4
205   IF X = 17 THEN X = 5
206   IF X = 16 THEN X = 6
208   IF X = 1 THEN X = 9
209   IF X = 15 THEN X = 1
210   RETURN
220 N = 1:P0 = 0:P1 = P1 - 192
222 X = P1: GOSUB 200:P1 = X: RETURN
230 N = 1:P0 = 1:P1 = P1 - 128
235 X = P1: GOSUB 200:P1 = X: RETURN
240 N =  - 1:P0 = 0:P1 = P1 - 64
245 X = P1: GOSUB 200:P1 = X
250   RETURN
993   GOTO 85
1030 V(I) = F(I) + R
1040   IF V(I) <  =  - 5.03 THEN 1140
1050   IF V(I) <  =  - 4.32 THEN 1160
1060   IF V(I) <  =  - 3.49 THEN 1180
1070   IF V(I) <  =  - 2.54 THEN 1200
1080   IF V(I) <  =  - 1.50 THEN 1220
1090   IF V(I) <  =  - 0.95 THEN 1240
1100   IF V(I) <  = 0 THEN 1260
1110   IF V(I) >  = 0 THEN 1280
1140 T(I) =  - 61.57775564 * V(I) - 56.40002411 * V(I
) ^ 2 - 11.89350092 * V(I) ^ 3 - .869149705 * V(I
) ^ 4
1150   GOTO 1290
1160 T(I) = 245.6788615 * V(I) + 137.9676961 * V(I) ^
2 + 28.9590096 * V(I) ^ 3 + 1.98471013 * V(I) ^ 4
1170   GOTO 1290
1180 T(I) =  - 16.55258623 * V(I) - 33.79202327 * V(I
) ^ 2 - 8.696918304 * V(I) ^ 3 - .78104418 * V(I)
^ 4
1190   GOTO 1290
1200 T(I) = 13.97126382 * V(I) - 13.09475853 * V(I) ^
2 - 4.39319606 * V(I) ^ 3 - .529091016 * V(I) ^ 4
```

```
1210   GOTO 1290
1220 T(I) = 35.30504193 * V(I) + 14.21756197 * V(I) ^
     2 + 7.430820452 * V(I) ^ 3 + 1.194482467 * V(I) ^
     4
1230   GOTO 1290
1240 T(I) = 39.25736753 * V(I) + 32.3232325 * V(I) ^
     2 + 26.13059638 * V(I) ^ 3 + 6.785094509 * V(I) ^
     4
1250 .GOTO 1290
1260 T(I) = 24.69864159 *. V(I) - 8.10435311 * V(I) ^
     2 - 16.05722274 * V(I) ^ 3 - 9.883571527 * V(I) ^
     4
1270   GOTO 1290
1280 T(I) = V(I) / .04
1290 T(I) = T(I) + 273.15
1300   IF H(I) = 0 THEN 1420
1370 C(I) = E * Y * G(I) / H(I)
1375   IF C(I) < 0 THEN 1378
1378 C(I) =   ABS (C(I))
1380 B(I) =   LOG (C(I)) /  LOG (10)
1390 K(I) = T(I) ^ ( - 1 / 4)
1392 C(I) =   INT (C(I) / .001 + .5) * .001
1394 T(I).=   INT (T(I) / .01 + .5) * .01
1396 B(I) =   INT (B(I) / .001 + .5) * .001
1398 K(I) =   INT (K(I) / .0001 + .5) * .0001
1400   PRINT
```

ประวัติผู้เขียน

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รามคำแหง เมื่อ พ.ศ. 2524 ปัจจุบันเป็นอาจารย์สอนอยู่ที่ โรงเรียน
หนองแค "สรกิจพิทยา" อ. หนองแค จ. สระบุรี

ผลงานทางวิชาการ ได้เสนอผลงานวิจัยเรื่อง สภาพนำไฟฟ้าของ
พอลิพิรโรล์ที่โรงแรมเชอราตันออคิด ในการประชุม วทท. ครั้งที่ 14
พ.ศ. 2531