เอกสารอ้างอิง

1. Sruce, S., Arjmand, M. and Ni, M., "Speech Analysis and Synthesis Become Practical on Microcomputer Chip", Electronic Design, May. 1982.

2. Flanagan, J.L., "Voice of Men and Machines", J.Acoust. Soc. Am., vol.51 pp.1375-1387, Mar. 1972.

3. Schroeder, M.R., "Vocoder :Analysis and Synthesis of Speech", Proc. IEEE, vol.54, pp.770-784, May. 1966.

4. Schafer, R.W. and Rabiner, L.R., "Digital Repersentation of Speech Signals", Proc. IEEE, vol.63, Apr. 1975.

5. Portnoff, M.R., "Implementation of the Digital Phase Vocoder Using the Fast Fourier Transform", IEEE. Acoust., Speech, and Signal Processing., vol. ASSP-24, pp.243-248, Jun. 1976.

6. Bruckert, E., Minow, M., and Tetschner, W., "Three-tiered Software and VLSI aid developmental system to read text aloud", Electronics, pp.133-138, Apr.21, 1983.

7. Rabiner, L.R., and Schafer, R.W., "Digital Processing of Speech Signals", Prentice-Hall, New York, 1978.

8. O' Shaughnessy, D., "Automatic Speech Synthesis", IEEE Communication Magazine, pp.26-33, 1983.

9. Oppenheim, A.V., and Schafer, R.W., "Homomorphic Analysis of Speech", IEE Trans. Audio Electroacoust., vol.AU-16, pp.221-226, Jun. 1968.

10. Oppenheim, A.V., "Speech Analysis-Synthesis System Based on Homomorphic Filtering", J.Acoust. Soc. Am., vol.45, pp. 458-465, Feb. 1969.
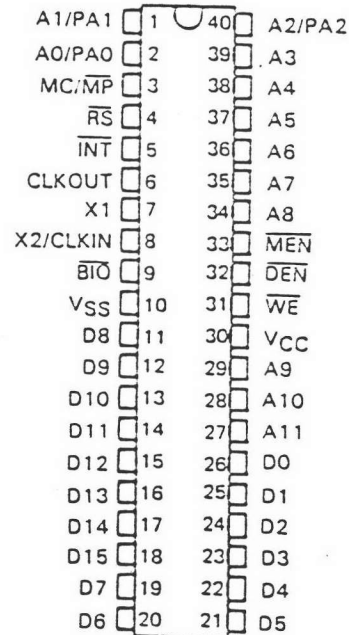
11. Oppenheim, A.V., and Schafer, R.W., "Digital Signal Processing", Prentice-hall, New York, 1975.

12. Markel, J.D. and Gray, A.H. Jr., "A Linear Precition Vocoder Simulation Based upon the autocorrelation Method", IEEE Trans. Acoust., Speech, and Signal Process., ASSP-22, pp. 124-134, Apr. 1974.

13. Makhoul, J., "Linear Prediction: A Tutorial Review", Proc. IEEE, vol.63, pp.561-580, Apr. 1975.

14. Markel, J.D. and Gray, A.H. Jr., "Linear Prediction of Speech", Springer-Verlag, New York, 1978.

15. Itakura, F., and Saito, S., "A Statistical Method for Estimate of Speech Spectral Density and Formant Frequency", Electron. and Commun., vol.53-A, pp.36-43, 1970.

16. Kitawaki, N., Itoh, K. and Itakura, F., "PARCOR Speech Analysis-Synthesis System", Review of the Electrical Communication Labs, Nippon Telegraph and Telephone Public Corp., Nov.-Dec. 1978.

17. Wiggins, R., and Brantingham, L., "Three-Chip system synthesizes human speech", Electronics, pp.109-116, Aug.31, 1978.

18. Rabiner, L.R., Cheng, M.J., Rosenberg, A.E. and Mcgonegal, C.A., "A Comparative Performance Study of Seven Pitch Detection Algorithms", IEEE Trans. Acoust., Speech, and Signal Process. vol. ASSP-24, pp.399-417, Oct. 1976.

19. Makel J.D., "The SIFT Algorithm for Fundamental Frequency Estimation", IEE Trans. Audio Electroacoust., vol.AU-20, pp.307-377, Sep. 1972.

20. Atal, B.S. and Hanauer, S., "Speech Analysis and Synthesis by Linear Prediction of Speech Wave", J. Acoust. Soc. Am., vol.50, Apr. 1972.

21. Itakura, F. and Saito, S., "On the Optimum Quantization of Feature
    Parameters in the PARCOR Speech Synthesizer", <u>IEEE 1972 conf</u>.
    on Speech Commun. and Process., April 24-26, 1972., pp.434-437.

22. Gray A.H. Jr., and Markel, J.D., "Quantization and Bit Allocation
    in Speech Processing", <u>IEEE Trans. Acoust., Speech, and Signal
    Procseeing</u>, vol. ASSP-24, pp.459-473, Dec. 1976.

ภาคผนวก

PROGRAMMABLE
PRODUCTS

TMS32010
DIGITAL SIGNAL PROCESSOR

MAY 1983
REV.·

- 200-ns Instruction Cycle

- 288-Byte On-Chip Data RAM

- ROMless Version – TMS32010

- 3K-Byte On-Chip Program ROM – TMS320M10

- External Memory Expansion to A Total of 8K Bytes at Full Speed

- 16-Bit Instruction/Data Word

- 32-Bit ALU/Accumulator

- 16 × 16-Bit Multiply in 200 ns

- 0 to 15-Bit Barrel Shifter

- Eight Input and Eight Output Channels

- 16-bit Bidirectional Data Bus with 40-Megabits-per-Second Transfer Rate

- Interrupt with Full Context Save

- Signed Two's Complement Fixed-Point Arithmetic

- NMOS Technology

- Single 5-V Supply

description

The TMS32010 is the first member of the new TMS320 digital signal processing family, designed to support a wide range of high-speed or numeric-intensive applications. This 16/32-bit single-chip microcomputer combines the flexibility of a high-speed controller with the numerical capability of an array processor, thereby offering an inexpensive alternative to multichip bit-slice processors. The TMS320 family contains the first MOS microcomputers capable of executing five million instructions per second. This high throughput is the result of the comprehensive, efficient, and easily programmed instruction set and of the highly pipelined architecture. Special instructions have been incorporated to speed the execution of digital signal processing (DSP) algorithms.

The TMS320 family's unique versatility and power give the design engineer a new approach to a variety of complicated applications. In addition, these microcomputers are capable of providing the multiple functions often required for a single application. For example, the TMS320 family can enable an industrial robot to synthesize and recognize speech, sense objects with radar or optical intelligence, and perform mechanical operations through digital servo loop computations.

TMS32010 . . . JDL PACKAGE
(TOP VIEW)

```
        A1/PA1  [ 1    40 ]  A2/PA2
        A0/PA0  [ 2    39 ]  A3
        MC/MP   [ 3    38 ]  A4
          RS    [ 4    37 ]  A5
         INT    [ 5    36 ]  A6
       CLKOUT   [ 6    35 ]  A7
          X1    [ 7    34 ]  A8
      X2/CLKIN  [ 8    33 ]  MEN
          BIO   [ 9    32 ]  DEN
          VSS   [ 10   31 ]  WE
          D8    [ 11   30 ]  VCC
          D9    [ 12   29 ]  A9
          D10   [ 13   28 ]  A10
          D11   [ 14   27 ]  A11
          D12   [ 15   26 ]  D0
          D13   [ 16   25 ]  D1
          D14   [ 17   24 ]  D2
          D15   [ 18   23 ]  D3
          D7    [ 19   22 ]  D4
          D6    [ 20   21 ]  D5
```

PIN NOMENCLATURE

SIGNATURE	I/O	DEFINITION
A11-A0/ PA2-PA0	OUT	External address bus. I/O port address multiplexed over PA2-PA0.
BIO	IN	External polling input for bit test and jump operations.
CLKOUT	OUT	System clock output, ¼ crystal/CLKIN frequency.
D15-D0	I/O	16-bit data bus.
DEN	OUT	Data enable indicates the processor accepting input data on D15-D0.
INT	IN	Interrupt.
MC/MP	IN	Memory mode select pin. High selects microcomputer mode. Low selects microprocessor mode.
MEN	OUT	Memory enable indicates that D15-D0 will accept external memory instruction.
RS	IN	Reset used to initialize the device.
VCC	IN	Power.
VSS	IN	Ground.
WE	OUT	Write enable indicates valid data on D15-D0.
X1	IN	Crystal input.
X2/CLKIN	IN	Crystal input or external clock input.

3

functional block diagram
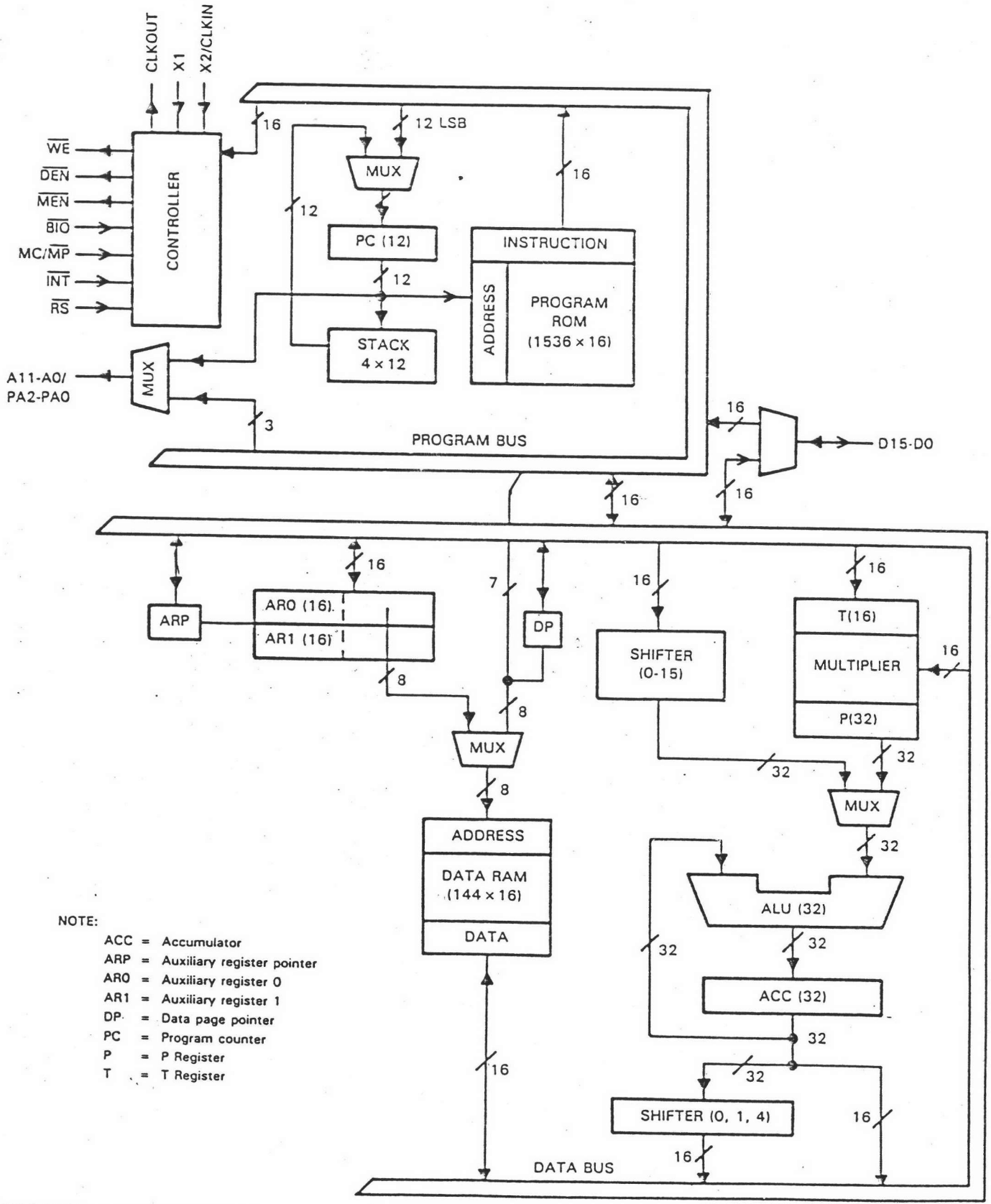
NOTE:

ACC	=	Accumulator
ARP	=	Auxiliary register pointer
AR0	=	Auxiliary register 0
AR1	=	Auxiliary register 1
DP	=	Data page pointer
PC	=	Program counter
P	=	P Register
T	=	T Register

TEXAS
INSTRUMENTS
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

architecture

The TMS320 family utilizes a modified Harvard architecture for speed and flexibility. In a strict Harvard architecture, program and data memory lie in two separate spaces, permitting a full overlap of the instruction fetch and execution. The TMS320 family's modification of the Harvard architecture allows transfers between program and data spaces, thereby increasing the flexibility of the device. This modification permits coefficients stored in program memory to be read into the RAM, eliminating the need for a separate coefficient ROM. It also makes available immediate instructions and subroutines based on computed values.

The TMS32010 utilizes hardware to implement functions that other processors typically perform in software. For example, this device contains a hardware multiplier to perform a multiplication in a single 200-ns cycle. There is also a hardware barrel shifter for shifting data on its way into the ALU. Finally, extra hardware has been included so that auxiliary registers, which provide indirect data RAM addresses, can be configured in an autoincrement/decrement mode for single-cycle manipulation of data tables. This hardware-intensive approach gives the design engineer the type of power previously unavailable on a single chip.

32-bit ALU/accumulator

The TMS32010 contains a 32-bit ALU and accumulator that support double-precision arithmetic. The ALU operates on 16-bit words taken from the data RAM or derived from immediate instructions. Besides the usual arithmetic instructions, the ALU can perform Boolean operations, providing the bit manipulation ability required of a high-speed controller.

shifters

A barrel shifter is available for left-shifting data 0 to 15 places before it is loaded into, subtracted from, or added to the accumulator. This shifter extends the high-order bit of the data word and zero-fills the low-order bits for two's complement arithmetic. A second shifter left-shifts the upper half of the accumulator 0, 1, or 4 places while it is being stored in the data RAM. Both shifters are very useful for scaling and bit extraction.

16 × 16-bit parallel multiplier

The TMS32010's multiplier performs a 16 × 16-bit, two's complement multiplication in one 200-ns instruction cycle. The 16-bit T Register temporarily stores the multiplicand; the P Register stores the 32-bit result. Multiplier values either come from the data memory or are derived immediately from the MPYK (multiply immediate) instruction word. The fast on-chip multiplier allows the TMS32010 to perform such fundamental operations as convolution, correlation, and filtering at the rate of 2.5 million samples per second.

program memory expansion

The TMS320M10 is equipped with a 1536-word ROM which is mask-programmed at the factory with a customer's program. It can also execute from an additional 2560 words of off-chip program memory at full speed. This memory expansion capability is especially useful for those situations where a customer has a number of different applications that share the same subroutines. In this case, the common subroutines can be stored on-chip while the application specific code is stored off-chip.

The TMS320M10 can operate in either of the following memory modes via the MC/$\overline{\text{MP}}$ pin:

Microcomputer Mode (MC) — Instruction addresses 0-1535 fetched from on-chip ROM. Those with addresses 1536-4095 fetched from off-chip memory at full speed.

Microprocessor Mode ($\overline{\text{MP}}$) — Full speed execution from all 4096 off-chip instruction addresses.

The TMS32010 is identical to the TMS320M10, except that the TMS32010 operates only in the microprocessor mode. Henceforth, TMS32010 refers to both versions.

The ability of the TMS32010 to execute at full speed from off-chip memory provides the following important benefits:

- Easier prototyping and development work than is possible with a device that can address only on-chip ROM,
- Purchase of a standard off-the-shelf product rather than a semi-custom mask-programmed device,
- Ease of updating code,
- Execution from external RAM,
- Downloading of code from another microprocessor, and
- Use of off-chip RAM to expand data storage capability.

input/output

The TMS32010's 16-bit parallel data bus can be utilized to perform I/O functions at burst rates of 40 million bits per second. Available for interfacing to peripheral devices are 128 input and 128 output bits consisting of eight 16-bit multiplexed input ports and eight 16-bit multiplexed output ports. In addition, a polling input for bit test and jump operations ($\overline{BIO}$) and an interrupt pin ($\overline{INT}$) have been incorporated for multi-tasking.

interrupts and subroutines

The TMS32010 contains a four-level hardware stack for saving the contents of the program counter during interrupts and subroutine calls. Instructions are available for saving the TMS32010's complete context. The instructions, PUSH stack from accumulator, and POP stack to accumulator permit a level of nesting restricted only by the amount of available RAM. The interrupts used in the TMS32010 are maskable.

instruction set

The TMS32010's comprehensive instruction set supports both numeric-intensive operations, such as signal processing, and general purpose operations, such as high-speed control. The instruction set, explained in Tables 1 and 2, consists primarily of single-cycle single-word instructions, permitting execution rates of up to five million instructions per seconds. Only infrequently used branch and I/O instructions are multicycle.

The TMS32010 also contains a number of instructions that shift data a part of an arithmetic operation. These all execute in a single cycle and are very useful for scaling data in parallel with other operations.

Three main addressing modes are available with the TMS32010 instruction set: direct, indirect, and immediate addressing.

direct addressing

In direct addressing, seven bits of the instruction word concatenated with the data page pointer form the data memory address. This implements a paging scheme in which the first page contains 128 words and the second page contains 16 words. In a typical application, infrequently accessed variables, such as those used for servicing an interrupt, are stored on the second page. The instruction format for direct addressing is shown below.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPCODE								0	dma						
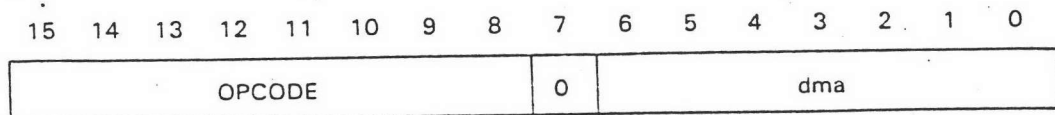
Bit 7 = 0 defines direct addressing mode. The opcode is contained in bits 15 through 8. Bits 6 through 0 contain data memory address.

The seven bits of the data memory address (dma) field can directly address up to 128 words (1 page) of data memory. Use of the data memory page pointer is required to address the full 144 words of data memory.

Direct addressing can be used with all instructions requiring data operands except for the immediate operand instructions.

indirect addressing

Indirect addressing forms the data memory address from the least significant eight bits of one of two auxiliary registers, AR0 and AR1. The auxiliary register pointer (ARP) selects the current auxiliary register. The auxiliary registers can be automatically incremented or decremented in parallel with the execution of any indirect instruction to permit single-cycle manipulation of data tables. The instruction format for indirect addressing is as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPCODE								1	0	INC	DEC	ARP	0	0	ARP
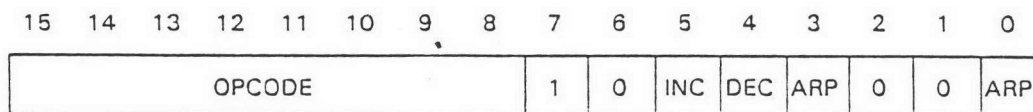
Bit 7 = 1 defines indirect addressing mode. The opcode is contained in bits 15 through 8. Bits 6 through 0 contain indirect addressing control bits.

Bit 3 and bit 0 control the Auxiliary Register Pointer (ARP). If bit 3 = 0, then the contents of bit 0 are loaded into the ARP. If bit 3 = 1, then the contents of the ARP remain unchanged. ARP = 0 defines the contents of AR0 as a memory address. ARP = 1 defines the contents of AR1 as a memory address.

Bit 5 and bit 4 control the auxiliary registers. If bit 5 = 1, then the ARP defines which auxiliary register is to be incremented by 1. If bit 4 = 1, then the ARP defines which auxiliary register is to be decremented by 1. If bit 5 and bit 4 are zero, then neither auxiliary register is incremented or decremented. Bits 6, 2, and 1 are reserved and should always be programmed to zero.

Indirect addressing can be used with all instructions requiring data operands, except for the immediate operand instructions.

immediate addressing

The TMS32010 instruction set contains special "immediate" instructions. These instructions derive data from part of the instruction word rather than from the data RAM. Some very useful immediate instructions are multiply immediate (MPYK), load accumulator immediate (LACK), and load auxiliary register immediate (LARK).

TABLE 1 — INSTRUCTION SYMBOLS

SYMBOL	MEANING
ACC	Accumulator
D	Data memory address field
I	Addressing mode bit
K	Immediate operand field
PA	3-bit port address field
R	1-bit operand field specifying auxiliary register
S	4-bit left-shift code
X	3-bit accumulator left-shift field

A-7

ประวัติผู้เขียน

    นายกฤษดา เรเยส เกิดเมื่อวันที่ 19 กรกฎาคม 2503 ที่จังหวัดลำปาง สำเร็จ ปริญญาวิศวกรรมศาสตรบัณฑิต สาขาวิศวกรรมไฟฟ้า จากจุฬาลงกรณ์มหาวิทยาลัย เมื่อ พ.ศ.2524 ปัจจุบันทำงานในตำแหน่งวิศวกรเครื่องฝึกบินจำลอง ประจำศูนย์ฝึกและปฏิบัติการ บริษัทการบินไทย จำกัด