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1.1 หน้า 487 - 489

1.2 หน้า 470 - 479

1.3 หน้า 459 - 463

1.4 หน้า 516 - 518

1.5 หน้า 520 - 521

1.6 หน้า 522 - 526

1.7 หน้า 529 - 531

1.8 หน้า 420 - 425

1.9 หน้า 495 - 509

1.10 หน้า 77 - 82

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2.1 หน้า II - 17 — II - 23

2.2 หน้า III - 73 — II - 78

2.3 หน้า II - 52 — II - 53

2.4 หน้า II - 40 — II - 41

2.5 หน้า II - 83 — II - 87

2.6 หน้า III - 77

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5.1 บท "Active filters"

5.3 หน้า 245 - 247

6. B.P. Lathi, Communication System, (John Wiley & Sons, Inc., 1968)

6.1 หน้า 89 - 94

6.2 หน้า 23 - 25

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8. Application hints for LM 139/Lm 239/Lm 339 Comparators, NS Linear Data Book.

ภาคผนวก ก.

โปรแกรมและผลการวิเคราะห์สเปคตรัมของสัญญาณที่ได้จากการสุ่ม

โปรแกรมนี้เขียนด้วยภาษา PL/I โดยใช้สมการ (3.3-4), (3.3-5) และ (3.3-6) ผลการคำนวณที่รวบรวมไว้ ณ ที่นี้ แสดงสำหรับค่าอัตราส่วนของความถี่สุ่มต่อความถี่สัญญาณเข้าจาก 4 ถึง 15 ส่วนผลการคำนวณส่วนต่อมาแสดงผลการคำนวนที่ไม่ขึ้นกับเฟสของสัญญาณเข้า

```
/*****************************************************************SPE00010
*  PROGRAM FOR FINDING MAGNITUDE SPECTRUM OF SAMPLED SINE WAVE  *SPE00020
*          PHASE SHIFT OF SAMPLED SINE WAVE = P                 *SPE00030
*          SAMPLING TO INPUT FREQUENCY RATIO = S                *SPE00040
*****************************************************************/SPE00050
SPECTRM: PROC OPTIONS (MAIN);                                     SPE00060
DECLARE (F(20),PI,AK,BK,ANGLE_1,ANGLE_2,CK) DECIMAL FLOAT (16);   SPE00070
PI = 3.1415926535;                                                SPE00080
ON ENDFILE (SYSIN) STOP;                                          SPE00090
DO WHILE (6=6);                                                   SPE00100
   GET LIST (P,S);                                                SPE00110
   /*****************************                                 SPE00120
   * INPUT SINE WAVE GENERATION *                                 SPE00130
   *****************************/                                 SPE00140
   ANGLE = 0;                                                     SPE00150
   DIFF = 360/S;                                                  SPE00160
   DO I = 1 TO S;                                                 SPE00170
      ANGLE = ANGLE+DIFF;                                         SPE00180
      F(I) = SIND(-P+DIFF*(I-1));                                 SPE00190
   END;                                                           SPE00200
   /*****************                                             SPE00210
   * PRINT HEADING *                                             SPE00220
   *****************/                                            SPE00230
   PUT PAGE;                                                      SPE00240
   PUT SKIP(6);                                                   SPE00250
   PUT EDIT ('MAGNITUDE SPECTRUM OF SAMPLED SINE WAVE')(X(10),A);SPE00260
   PUT SKIP(2) EDIT ('PHASE SHIFT OF SAMPLED SINE WAVE  =',P,     SPE00270
                     'DEGREE') (X(10),A,F(5),X(2),A);             SPE00280
   PUT SKIP EDIT ('SAMPLING TO INPUT FREQUENCY RATIO  =',S)       SPE00290
                 (X(10),A,F(4));                                  SPE00300
   PUT SKIP(2) EDIT ('NORMALIZED FREQUENCY','AMPLITUDE')          SPE00310
                    (X(20),A,X(10),A,SKIP);                       SPE00320
   /*************************************                         SPE00330
   * CALCULATE K_TH HARMONIC MAGNITUDE *                         SPE00340
   *************************************/                        SPE00350
   DO K = 1 TO 3*S;                                               SPE00360
      AK,BK = 0;                                                  SPE00370
      DO I = 1 TO S;                                              SPE00380
         ANGLE_1 = 2*PI*K*(((I-1)/S)-0.5);                        SPE00390
         ANGLE_2 = 2*PI*K*((I/S)-0.5);                            SPE00400
         AK = AK+F(I)*(SIN(ANGLE_2)-SIN(ANGLE_1));                SPE00410
         BK = BK+F(I)*(COS(ANGLE_1)-COS(ANGLE_2));                SPE00420
      END;                                                        SPE00430
      CK = SQRT(AK*AK+BK*BK)/(2*PI*K);                            SPE00440
      PUT SKIP EDIT (K,CK) (X(29),F(2),X(16),F(15,13));           SPE00450
   END;                                                           SPE00460
END;                                                              SPE00470
END SPECTRM;                                                      SPE00480
```

MAGNITUDE SPECTRUM OF SAMPLED SINE WAVE

PHASE SHIFT OF SAMPLED SINE WAVE = 0 DEGREE
SAMPLING TO INPUT FREQUENCY RATIO = 4

NORMALIZED FREQUENCY	AMPLITUDE
1	0.4501581580813
2	0.0000000000408
3	0.1500527193739
4	0.0000000000000
5	0.0900316316082
6	0.0000000000302
7	0.0643083083089
8	0.0000000000000
9	0.0500175731112
10	0.0000000000292
11	0.0409234689275
12	0.0000000000000

MAGNITUDE SPECTRUM OF SAMPLED SINE WAVE

PHASE SHIFT OF SAMPLED SINE WAVE = 0 DEGREE
SAMPLING TO INPUT FREQUENCY RATIO = 5

NORMALIZED FREQUENCY	AMPLITUDE
1	0.4677446634140
2	0.0000000213928
3	0.0000000175627
4	0.1169361472381
5	0.0000000566874
6	0.0779574563126
7	0.0000000190781
8	0.0000000179718
9	0.0519716127212
10	0.0000000566874
11	0.0425222556670
12	0.0000000187803
13	0.0000000181244
14	0.0334103171449
15	0.0000000566874

MAGNITUDE SPECTRUM OF SAMPLED SINE WAVE

PHASE SHIFT OF SAMPLED SINE WAVE = 0 DEGREE
SAMPLING TO INPUT FREQUENCY RATIO = 6

NORMALIZED FREQUENCY	AMPLITUDE
1	0.4774648551242
2	0.0000000000331
3	0.0000000688090
4	0.0000000000249
5	0.0954929297394
6	0.0000000000000
7	0.0682092945073
8	0.0000000000223
9	0.0000000688090
10	0.0000000000220
11	0.0434058583882
12	0.0000000000000
13	0.0367280975367
14	0.0000000000217
15	0.0000000688090
16	0.0000000000217
17	0.0280861315201
18	0.0000000000000

MAGNITUDE SPECTRUM OF SAMPLED SINE WAVE

PHASE SHIFT OF SAMPLED SINE WAVE = 0 DEGREE
SAMPLING TO INPUT FREQUENCY RATIO = 7

NORMALIZED FREQUENCY	AMPLITUDE
1	0.4833832243928
2	0.0000002436681
3	0.0000002262563
4	0.0000001730006
5	0.0000001134769
6	0.0805638664476
7	0.0000000466009
8	0.0604229062625
9	0.0000000544486
10	0.0000000690668
11	0.0000000662729
12	0.0000000585366
13	0.0371833209983
14	0.0000000466009
15	0.0322255517204
16	0.0000000358950
17	0.0000000427333
18	0.0000000436899
19	0.0000000456406
20	0.0241691573635
21	0.0000000466009

MAGNITUDE SPECTRUM OF SAMPLED SINE WAVE

PHASE SHIFT OF SAMPLED SINE WAVE = 0 DEGREE
SAMPLING TO INPUT FREQUENCY RATIO = 8

NORMALIZED FREQUENCY	AMPLITUDE
1	0.4872476853069
2	0.0000000000288
3	0.0000000096193
4	0.0000000000188
5	0.0000000057823
6	0.0000000000213
7	0.0696068121955
8	0.0000000000000
9	0.0541386316939
10	0.0000000000206
11	0.0000000026186
12	0.0000000000128
13	0.0000000022281
14	0.0000000000204
15	0.0324831790287
16	0.0000000000000
17	0.0286616285402
18	0.0000000000203
19	0.0000000015132
20	0.0000000000122
21	0.0000000013819
22	0.0000000000203
23	0.0211846819779
24	0.0000000000000

MAGNITUDE SPECTRUM OF SAMPLED SINE WAVE

PHASE SHIFT OF SAMPLED SINE WAVE = 0 DEGREE
SAMPLING TO INPUT FREQUENCY RATIO = 10

NORMALIZED FREQUENCY	AMPLITUDE
1	0.4918158344873
2	0.0000000000261
3	0.0000000238254
4	0.0000000000170
5	0.0000000506935
6	0.0000000000135
7	0.0000000345375
8	0.0000000000202
9	0.0546461971906
10	0.0000000000000
11	0.0447105358417
12	0.0000000000200
13	0.0000000295934
14	0.0000000000106
15	0.0000000506935
16	0.0000000000105
17	0.0000000326471
18	0.0000000000198
19	0.0258850376286
20	0.0000000000000
21	0.0234198073347
22	0.0000000000198
23	0.0000000303458
24	0.0000000000101
25	0.0000000506935
26	0.0000000000101
27	0.0000000321571
28	0.0000000000198
29	0.0169591605231
30	0.0000000000000

MAGNITUDE SPECTRUM OF SAMPLED SINE WAVE

PHASE SHIFT OF SAMPLED SINE WAVE = 0 DEGREE
SAMPLING TO INPUT FREQUENCY RATIO = 15

NORMALIZED FREQUENCY	AMPLITUDE
1	0.4963525918074
2	0.0000000360043
3	0.0000000305900
4	0.0000000203521
5	0.0000000132091
6	0.0000000079282
7	0.0000000061029
8	0.0000000166343
9	0.0000000162136
10	0.0000000169356
11	0.0000000169441
12	0.0000000204523
13	0.0000000379590
14	0.0354537674871
15	0.0000000242434
16	0.0310220274246
17	0.0000000374940
18	0.0000000228330
19	0.0000000163901
20	0.0000000125601
21	0.0000000107038
22	0.0000000098431
23	0.0000000133687
24	0.0000000136688
25	0.0000000147546
26	0.0000000163773
27	0.0000000210934
28	0.0000000378175
29	0.0171156171666
30	0.0000000242434
31	0.0160113640574
32	0.0000000375883
33	0.0000000223035
34	0.0000000162642
35	0.0000000129332
36	0.0000000113203
37	0.0000000105687
38	0.0000000126844
39	0.0000000131054
40	0.0000000142850
41	0.0000000162950
42	0.0000000213063
43	0.0000000377747
44	0.0112807511555
45	0.0000000242434

MAGNITUDE SPECTRUM OF SAMPLED SINE WAVE

PHASE SHIFT OF SAMPLED SINE WAVE = 10 DEGREE
SAMPLING TO INPUT FREQUENCY RATIO = 10

NORMALIZED FREQUENCY	AMPLITUDE
1	0.49181583928 59
2	0.00000000002 30
3	0.00000003808 99
4	0.00000000001 45
5	0.00000005682 42
6	0.00000000001 45
7	0.00000002445 37
8	0.00000000002 30
9	0.05464619112 73
10	0.00000000000 00
11	0.04471054167 50
12	0.00000000002 30
13	0.00000002649 25
14	0.00000000001 45
15	0.00000005637 19
16	0.00000000001 45
17	0.00000002406 34
18	0.00000000002 30
19	0.02588503163 19
20	0.00000000000 00
21	0.02341981321 73
22	0.00000000002 30
23	0.00000002557 35
24	0.00000000001 45
25	0.00000005633 56
26	0.00000000001 45
27	0.00000002420 73
28	0.00000000002 30
29	0.01695915454 71
30	0.00000000000 00

MAGNITUDE SPECTRUM OF SAMPLED SINE WAVE

PHASE SHIFT OF SAMPLED SINE WAVE = 80 DEGREE
SAMPLING TO INPUT FREQUENCY RATIO = 10

NORMALIZED FREQUENCY	AMPLITUDE
1	0.49181582171 36
2	0.0000000000373
3	0.0000000207584
4	0.0000000000301
5	0.0000000450527
6	0.0000000000301
7	0.0000000437334
8	0.0000000000373
9	0.05464620168 47
10	0.0000000000000
11	0.04471052984 22
12	0.0000000000373
13	0.0000000324014
14	0.0000000000301
15	0.0000000450527
16	0.0000000000301
17	0.0000000393258
18	0.0000000000373
19	0.02588504255 85
20	0.0000000000000
21	0.02341980165 78
22	0.0000000000373
23	0.0000000340786
24	0.0000000000301
25	0.0000000450527
26	0.0000000000301
27	0.0000000381959
28	0.0000000000373
29	0.01695916558 83
30	0.0000000000000

MAGNITUDE SPECTRUM OF SAMPLED SINE WAVE

PHASE SHIFT OF SAMPLED SINE WAVE = 90 DEGREE
SAMPLING TO INPUT FREQUENCY RATIO = 10

NORMALIZED FREQUENCY	AMPLITUDE
1	0.49181581191 50
2	0.00000000003 61
3	0.00000003734 27
4	0.00000000002 89
5	0.00000003981 57
6	0.00000000002 89
7	0.00000004461 32
8	0.00000000003 61
9	0.05464620799 53
10	0.00000000000 00
11	0.04471052289 74
12	0.00000000003 61
13	0.00000004030 10
14	0.00000000002 89
15	0.00000003715 52
16	0.00000000002 89
17	0.00000004280 05
18	0.00000000003 61
19	0.02588504905 27
20	0.00000000000 00
21	0.02341979484 89
22	0.00000000003 61
23	0.00000004086 33
24	0.00000000002 89
25	0.00000003693 41
26	0.00000000002 89
27	0.00000004236 19
28	0.00000000003 61
29	0.01695917213 94
30	0.00000000000 00

MAGNITUDE SPECTRUM OF SAMPLED SINE WAVE

PHASE SHIFT OF SAMPLED SINE WAVE = 110 DEGREE
SAMPLING TO INPUT FREQUENCY RATIO = 10

NORMALIZED FREQUENCY	AMPLITUDE
1	0.49181581399 38
2	0.0000000000314
3	0.0000000689770
4	0.0000000000240
5	0.0000000180228
6	0.0000000000240
7	0.0000000428233
8	0.0000000000314
9	0.0546462198208
10	0.0000000000000
11	0.0447105136000
12	0.0000000000314
13	0.0000000529320
14	0.0000000000240
15	0.0000000173385
16	0.0000000000240
17	0.0000000461162
18	0.0000000000314
19	0.0258850601463
20	0.0000000000000
21	0.0234197850098
22	0.0000000000314
23	0.0000000511106
24	0.0000000000240
25	0.0000000172826
26	0.0000000000240
27	0.0000000470982
28	0.0000000000314
29	0.0169591830059
30	0.0000000000000

ภาคผนวก ข.

ข้อมูลของวงจรรวมที่สำคัญ ๆ จากผู้ผลิต

ในภาคผนวกตอนนี้ได้รวบรวมข้อมูลจากผู้ผลิต เฉพาะวงจรรวมที่สำคัญ ๆ ซึ่งหาได้ยาก เช่น DAC และ RAM ส่วนข้อมูลของวงจรตรรก และออพแอมป์ซึ่งหาได้ง่ายจากหนังสือคู่มือจะไม่รวบรวมไว้ ณ ที่นี้

National Semiconductor

MAY 1977

DAC0808, DAC0807, DAC0806(LM1508/LM1408) 8-bit D/A converter

general description

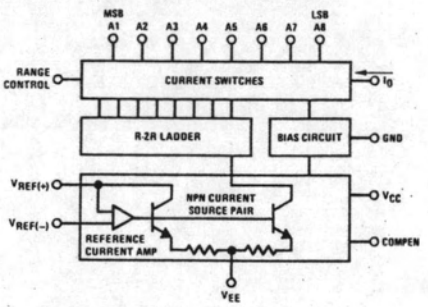
The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 I_{REF}/256. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

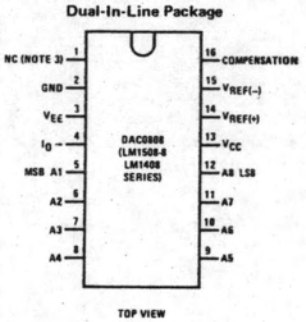
features

- Relative accuracy: ±0.19% error maximum (DAC0808)
- Full scale current match: ±1 LSB typ
- 7 and 6-bit accuracy available (DAC0807, DAC0806)
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/μs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

block and connection diagrams



Dual-In-Line Package



TOP VIEW

typical application

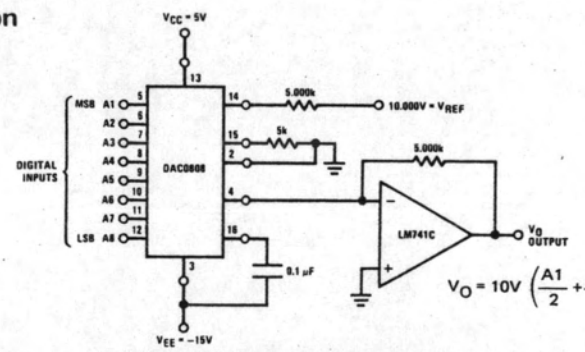


FIGURE 1. ±10V Output Digital to Analog Converter

ordering information

ACCURACY	OPERATING TEMPERATURE RANGE	ORDER NUMBERS*					
		D PACKAGE		J PACKAGE		N PACKAGE	
8-bit	$-55°C \leq T_A \leq +125°C$	DAC0808LD	LM1508D-8	DAC0808LJ	LM1508J-8		
8-bit	$0°C \leq T_A \leq +75°C$	DAC0808LCD	LM1408D-8	DAC0808LCJ	LM1408J-8	DAC0808LCN	LM1408N-8
7-bit	$0°C \leq T_A \leq +75°C$	DAC0807LCD	LM1408D-7	DAC0807LCJ	LM1408J-7	DAC0807LCN	LM1408N-7
6-bit	$0°C \leq T_A \leq +75°C$	DAC0806LCD	LM1408D-6	DAC0806LCJ	LM1408J-6	DAC0806LCN	LM1408N-6

*Note. Devices may be ordered by using either order number.

IM-B20M57/Printed in U.S.A.

absolute maximum ratings (T_A = 25°C unless otherwise noted)

Power Supply Voltage	
V_{CC}	5.5 V_{DC}
V_{EE}	−16.5 V_{DC}
Digital Input Voltage, V5–V12	−10 V_{DC} to +18 V_{DC}
Applied Output Voltage, V_O	−11 V_{DC} to +18 V_{DC}
Reference Current, I_{14}	5 mA
Reference Amplifier Inputs, V14, V15	V_{CC}, V_{EE}
Power Dissipation (Package Limitation)	
Cavity Package	1000 mW
Derate above T_A = 25°C	6.7 mW/°C
Operating Temperature Range	
DAC0808L (LM1508-8)	−55°C ≤ T_A ≤ +125°C
DAC0808LC Series (LM1408 Series)	0 ≤ T_A ≤ +75°C
Storage Temperature Range	−65°C to +150°C

electrical characteristics

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, $V_{REF}/R14$ = 2 mA, DAC0808L (LM1508-8): T_A = −55°C to +125°C, DAC0808LC, DAC0807LC, DAC0806LC (LM1408 Series), T_A = 0°C to +75°C, and all digital inputs at high logic level unless otherwise noted.)

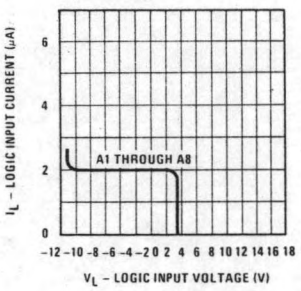
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	*(Figure 4)*				%
	DAC0808L (LM1508-8), DAC0808LC (LM1408-8)				±0.19	%
	DAC0807LC (LM1408-7), (Note 1)				±0.39	%
	DAC0806LC (LM1408-6), (Note 1)				±0.78	%
	Settling Time to Within 1/2 LSB (Includes t_{PLH})	T_A = 25°C (Note 2), *(Figure 5)*		150		ns
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = 25°C, *(Figure 5)*		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels	*(Figure 3)*				
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current	*(Figure 3)*				
	High Level	V_{IH} = 5V		0	0.040	mA
	Low Level	V_{IL} = 0.8V		−0.003	−0.8	mA
I_{15}	Reference Input Bias Current	*(Figure 3)*		−1	−5	μA
	Output Current Range	*(Figure 3)*				
		V_{EE} = −5V	0	2.0	2.1	mA
		V_{EE} = −15V, T_A = 25°C	0	2.0	4.2	mA
I_O	Output Current	V_{REF} = 2.000V, R14 = 1000Ω, *(Figure 3)*	1.9	1.99	2.1	mA
	Output Current, All Bits Low	*(Figure 3)*		0	4	μA
	Output Voltage Compliance	E_r ≤ 0.19%, T_A = 25°C				
	Pin 1 Grounded, V_{CC} Below −10V				−0.55, +0.4	V_{DC}
					−5.0, +0.4	V_{DC}
SRI_{REF}	Reference Current Slew Rate	*(Figure 6)*		8		mA/μs
	Output Current Power Supply Sensitivity	−5V ≤ V_{EE} ≤ −18V		0.05	2.7	μA/V
	Power Supply Current (All Bits Low)	*(Figure 3)*				
I_{CC}				2.3	22	mA
I_{EE}				−4.3	−13	mA
	Power Supply Voltage Range	T_A = 25°C, *(Figure 3)*				
V_{CC}			4.5	5.0	5.5	V_{DC}
V_{EE}			−4.5	−15	−16.5	V_{DC}
	Power Dissipation					
	All Bits Low	V_{CC} = 5V, V_{EE} = −5V		33	170	mW
		V_{CC} = 5V, V_{EE} = −15V		106	305	mW
	All Bits High	V_{CC} = 15V, V_{EE} = −5V		90		mW
		V_{CC} = 15V, V_{EE} = −15V		160		mW

Note 1: All current switches are tested to guarantee at least 50% of rated current.
Note 2: All bits switched.
Note 3: Range control is not required.

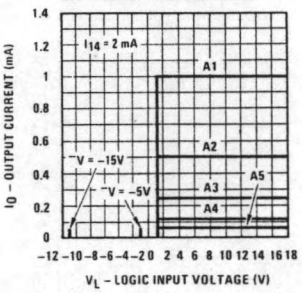
typical performance characteristics

V_{CC} = 5V, V_{EE} = −15V, T_A = 25°C, unless otherwise noted

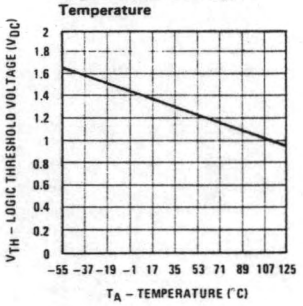
Logic Input Current vs Input Voltage



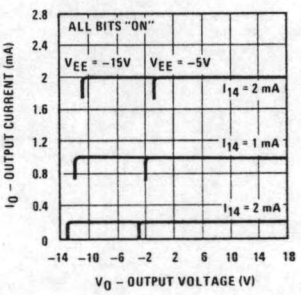
Bit Transfer Characteristics



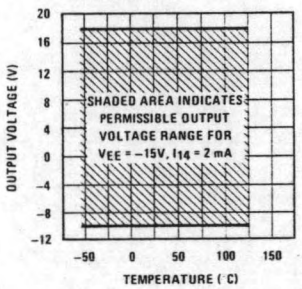
Logic Threshold Voltage vs Temperature



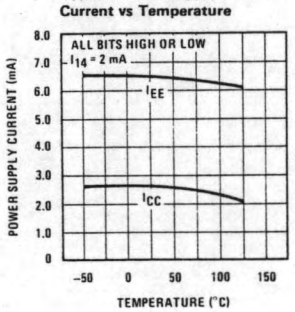
Output Current vs Output Voltage (Output Voltage Compliance)



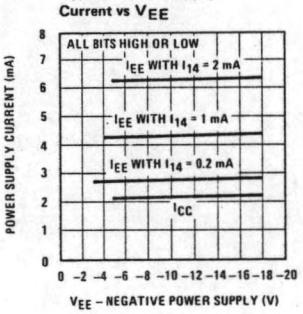
Output Voltage Compliance vs Temperature



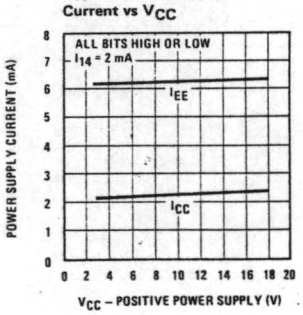
Typical Power Supply Current vs Temperature



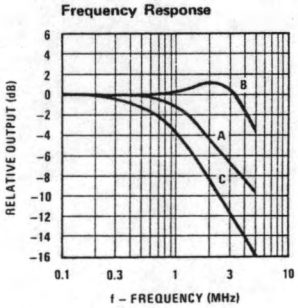
Typical Power Supply Current vs V_{EE}



Typical Power Supply Current vs V_{CC}



Reference Input Frequency Response



Unless otherwise specified: R14 = R15 = 1 kΩ, C = 15 pF, pin 16 to V_{EE}; R_L = 50Ω, pin 4 to ground.

Curve A: Large Signal Bandwidth Method of *Figure 7*, V_{REF} = 2 Vp-p offset 1 V above ground

Curve B: Small Signal Bandwidth Method of *Figure 7*, R_L = 250Ω, V_{REF} = 50 mVp-p offset 200 mV above ground.

Curve C: Large and Small Signal Bandwidth Method of *Figure 25* (no op amp, R_L = 50Ω), R_S = 50Ω, V_{REF} = 2V, V_S = 100 mVp-p centered at 0V.

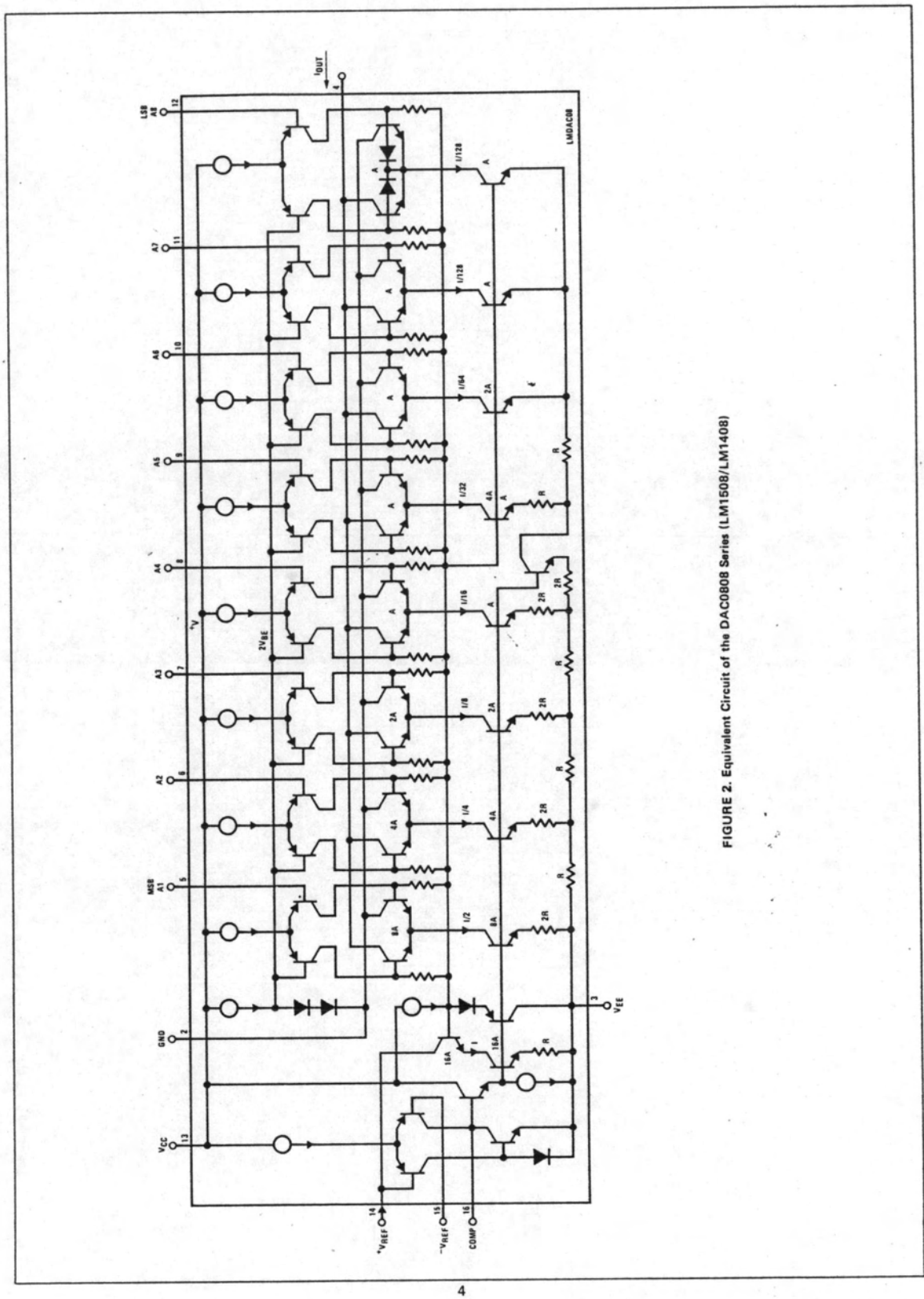
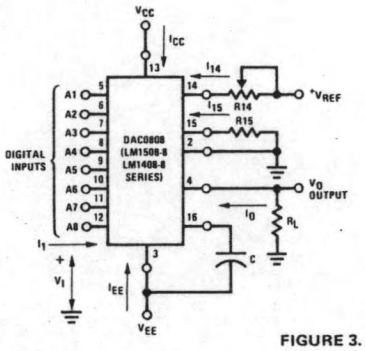


FIGURE 2. Equivalent Circuit of the DAC0808 Series (LM1508/LM1408)

test circuits



V_I and I_I apply to inputs A1–A8.

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right)$$

where $K \cong \frac{V_{REF}}{R14}$

and A_N = "1" if A_N is at high level

A_N = "0" if A_N is at low level

FIGURE 3. Notation Definitions Test Circuit

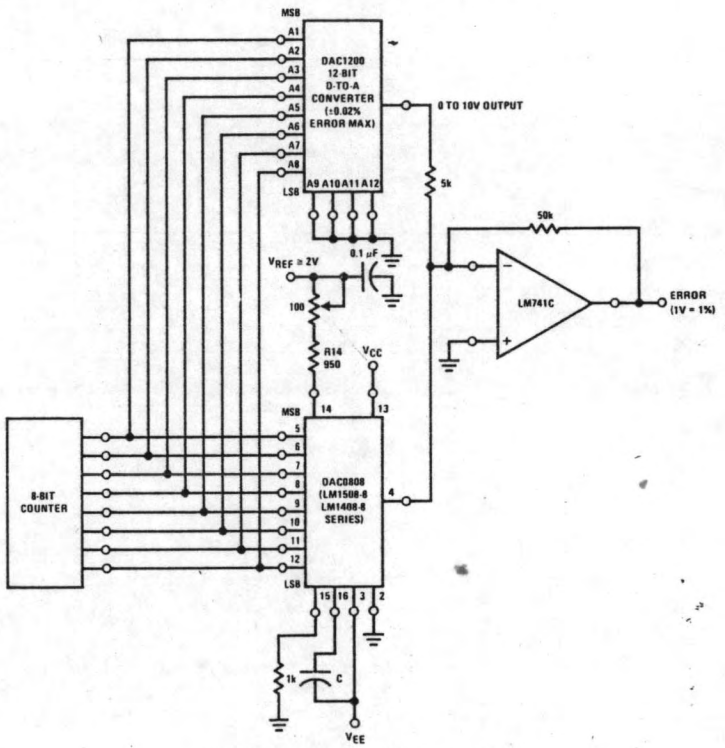


FIGURE 4. Relative Accuracy Test Circuit

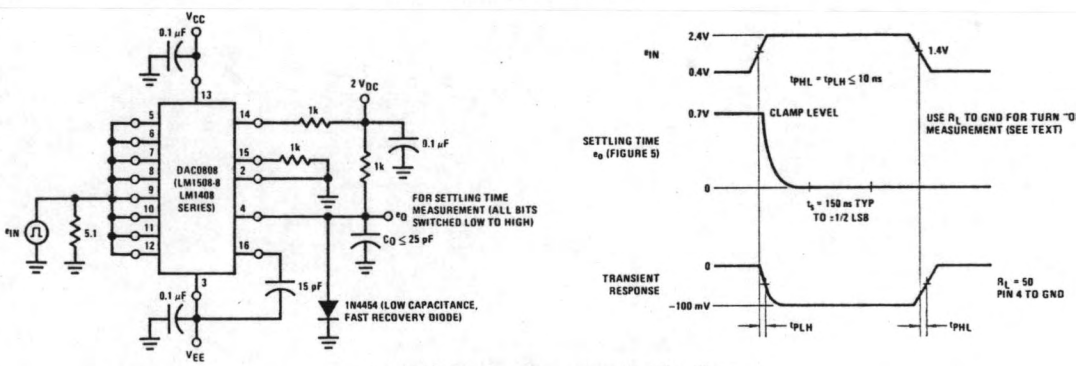


FIGURE 5. Transient Response and Settling Time

NATIONAL

Resistor Arrays

RA07, RA08, RA12, RA13, RA14, RA15 resistor arrays

general description

The RA07, RA08, RA12, RA13, RA14 and RA15 are arrays of 7 to 15 equal value resistors packaged in high reliability Epoxy B dual-in-line packages.

Each array is manufactured using precision automatic laser trimming of high stability thin films. The thin film array is then mounted on a high power dissipation lead frame and molded in the same Epoxy B used for National's semiconductor products. Complete automatic testing and inexpensive Epoxy B packages provide low costs unprecedented in the resistor industry. The RA07, RA08, RA12 and RA14 are symmetrical for goof-proof insertions.

Custom resistor arrays are also available from National. Possible options include unequal values, different configurations and tight tolerances to 0.01%.

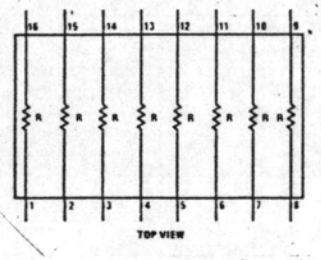
Resistor array applications range from pull-up and pull-down networks to line terminations and LED current limiting.

features

- Low cost
- Six configurations — 7 to 15 Resistors
- Wide resistance range — 22Ω to 100 kΩ
- Tight tolerance — ±2% or ±2Ω, max
- Excellent tracking — 2 ppm/°C
- Four symmetrical configurations

connection diagrams

RA08

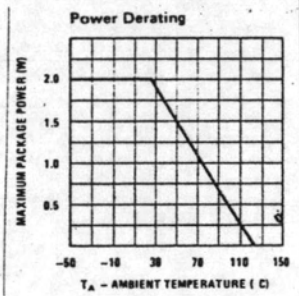


ordering information

RA07 – 10KN

- Resistor Array
- Configuration Number
- Resistance Value
- Molded Epoxy – B DIP Package

typical performance characteristics



absolute maximum ratings

Rated Voltage	(Note 1)
Package Power at 25°C (See curve)	2.0 W
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resistor Tolerance	T_A = 25°C		±1	±2 or ±2	% Ω
Resistor Matching	T_A = 25°C		0.2		%
Absolute Tempco	−55°C to +125°C		80		ppm/°C
Matching Tempco	−55°C to +125°C		2		ppm/°C
Resistance Voltage Coefficient			Negligible		μV/V
Overload Resistance Shift	2.5 x rated voltage for 5 seconds, T_A = 25°C			0.5	%
Rise Time			5		ns

Note 1: Rated voltage is determined from maximum package power dissipation and resistance ($P_{MAX} \geq \Sigma \left(\frac{V_i^2}{R_i}\right)$). Maximum power per resistor is 1/4 watt.

National Semiconductor

MOS RAMs

MM2102A, MM2102AL family
1024-bit (1024 × 1) static random access memories

general description

The MM2102A family of high speed 1024 x 1-bit static random access read/write memories are manufactured using N-channel depletion-mode silicon gate technology. Static storage cells eliminate the need for clocks or refresh circuitry and the resultant cost associated with them.

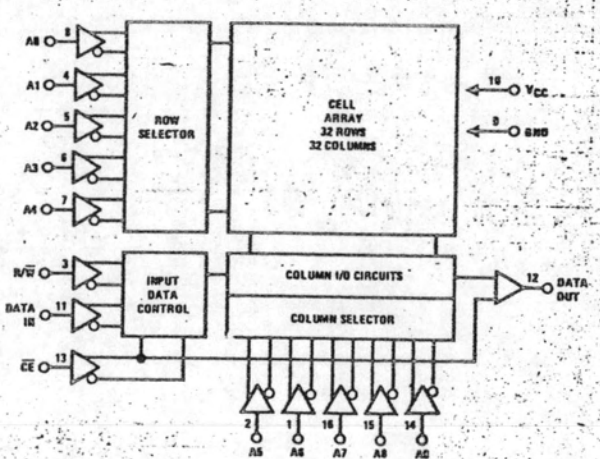
Low threshold silicon gate N-channel technology allows complete DTL/TTL compatibility of all inputs and outputs as well as a single 5V supply. The separate chip enable input ($\overline{CE}$) controlling the TRI-STATE® output allows easy memory expansion by OR-tying individual devices to a data bus. Data in and data out have the same polarity.

In addition to the MM2102A, a low power version, the MM2102AL, is also available. This selection offers a maximum operating current of 33 mA and a guaranteed standby mode down to a power supply voltage of 1.5V.

features

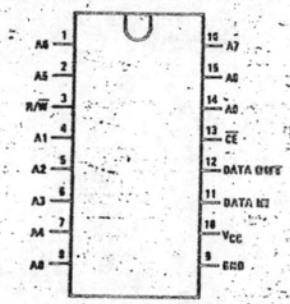
- Single 5V supply
- All inputs and outputs directly DTL/TTL compatible
- Static operation—no clocks or refresh
- TRI-STATE output for bus interface
- All inputs protected against static charge
- Access time down to 250 ns

block diagram



connection diagram

Dual-In-Line Package



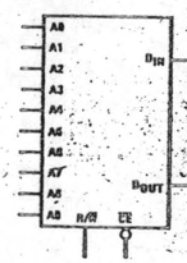
TOP VIEW

Order Number:	Order Number:
MM2102AJ-2L	MM2102AN-2L
MM2102AJ-2	MM2102AN-2
MM2102AJ-L	MM2102AN-L
MM2102AJ	MM2102AN
MM2102AJ-4L	MM2102AN-4L
MM2102AJ-4	MM2102AN-4
MM2102AJ-6L	MM2102AN-6L
MM2102AJ-6	MM2102AN-6
See Package 10	See Package 15

truth table

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	Hi-Z	Not selected
L	L	L	L	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{OUT}	Read

logic symbol



absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.5V to +7V
Voltage at Any Pin	−0.5V to +7V
Storage Temperature	−65°C to +150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C
Input Low Voltage	−0.5	0.8	V
Input High Voltag.	2.0	V_{CC}	V

dc electrical characteristics T_A = 0°C to +70°C, V_{CC} = ±5%, unless otherwise specified.

SYMBOL	PARAMETER	CONDITION	MM2102A, MM2102A-2, MM2102A-4, MM2102A-6		MM2102A-L, MM2102A-2L, MM2102A-4L, MM2102A-6L		UNITS
			MIN	MAX	MIN	MAX	
I_{LI}	Input Load Current	V_{IN} = 0 to 5.25V		10		10	μA
I_{LOH}	Output Leakage Current	$\overline{CE}$ = 2V, V_{OUT} = 2.4V		5		5	μA
I_{LOL}	Output Leakage Current	$\overline{CE}$ = 2V, V_{OUT} = 0.4V		−10		−10	μA
I_{CC}	Power Supply Current	All Inputs = 5.25V, Data Output Open, T_A = 25°C		45		31	mA
I_{CC}	Power Supply Current	All Inputs = 5.25V, Data Output Open, T_A = 0°C		50		33	mA
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −200 μA	2.4		2.4		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the device may be permanently damaged. They do not mean the device may be operated at these values.

ac electrical characteristics (With standard load) T_A = 0°C to +70°C, V_{CC} = 5V ±5% unless otherwise specified.

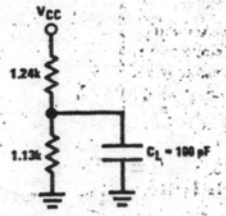
SYMBOL	PARAMETER	MM2102A-2, MM2102A-2L		MM2102A, MM2102A-L ✓		MM2102A-4, MM2102A-4L		MM2102A-6, MM2102A-6L		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE *(Figure 1)*										
t_{RC}	Read Cycle	250		350		450		650		ns
t_A	Access Time		250		350		450		650	ns
t_{CO}	Chip Enable to Output Time		100		150		200		200	ns
t_{OH1}	Previous Read Data Valid with Respect to Address	40		40		40		50		ns
t_{OH2}	Previous Read Data Valid with Respect to Chip Enable	0		0		0		0		ns
WRITE CYCLE *(Figure 2)*										
t_{WC}	Write Cycle	250		350		450		650		ns
t_{AW}	Address to Write Set-Up	20		20		20		20		ns
t_{WP}	Write Pulse Width	100		150		200		200		ns
t_{WR}	Write Recovery Time	0		0		0		0		ns
t_{DW}	Date Set-Up Time	85		125		175		175		ns
t_{DH}	Data Hold Time	0		0		0		0		ns
t_{CW}	Chip Enable To Write Set-Up	100		150		200		200		ns

ac electrical characteristics $T_A = 25°C$, f = 1 MHz

SYMBOL	PARAMETER	LIMIT (pF) TYP	LIMIT (pF) MAX
CAPACITANCE [2]			
C_{IN}	Input Capacitance (All Inputs $V_{IN} = 0V$)	3	5
C_{OUT}	Output Capacitance, $V_O = 0V$	4	6

Note 2: This parameter is guaranteed by periodic testing

ac test circuit



switching time waveforms

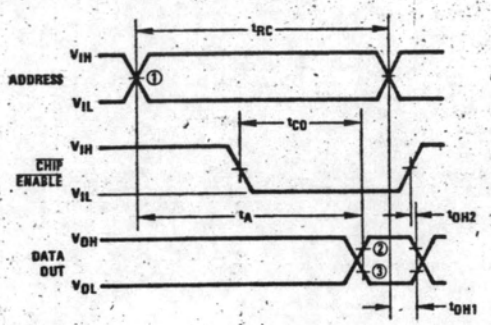


FIGURE 1. Read Cycle

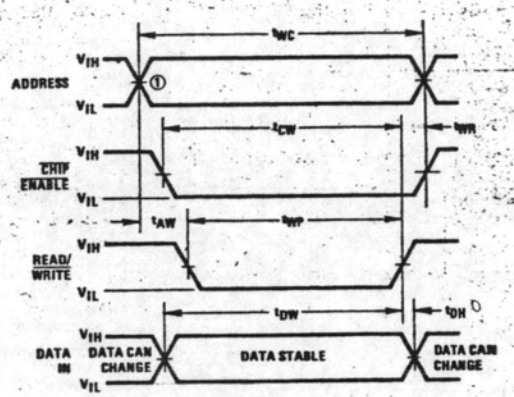


FIGURE 2. Write Cycle

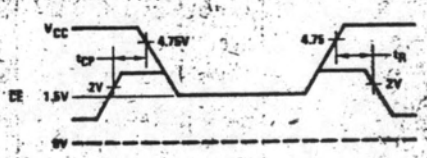
Note ①: Input reference level for timing is 1.5V.
Note ②: V_{OH} = 2V is reference level for output high.
Note ③: V_{OL} = 0.8V is reference level for output low.
Note ④: Input rise and fall times are 10 ns.

standby characteristics $T_A = 0°C$ to $+70°C$

SYMBOL	PARAMETER	CONDITIONS	MM2102A, MM2102A-2, MM2102A-4, MM2102-6 MIN	TYP(3)	MAX	MM2102A-L, MM2102A-2L, MM2102A-4L, MM2102A-6L MIN	TYP(3)	MAX	UNITS
V_{PD}	V_{CC} in Standby		1.5			1.5			V
V_{CES}	$\overline{CE}$ Bias in Standby	$2 \leq V_{PD} \leq V_{CCMAX}$	2.0			2.0			V
V_{CES}	$\overline{CE}$ Bias in Stand-by	$1.5 \leq V_{PD} \leq 2$	V_{PD}			V_{PD}			V
I_{PD1}	Standby Current	All Inputs = V_{PD} = 1.5V			28			23	mA
I_{PD2}	Standby Current	All Inputs = V_{PD} = 2V			38			28	mA
t_{CP}	Chip Deselect to Standby Time		0			0			ns
t_R	Recovery Time (Note 4)		t_{RC}			t_{RC}			ns

Note 3: Typical values at $T_A = 25°C$.
Note 4: $t_R = t_{RC}$ = read cycle time.

standby waveforms



MSI

DM54/DM74192,L192,LS192,193,L193,LS193

Synchronous Up/Down Counters with Dual Clock

General Description

These circuits are synchronous up/down counters; the 192, L192 and LS192 circuits are BCD counters and the 193, L193 and LS193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed, while the other count input is held high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

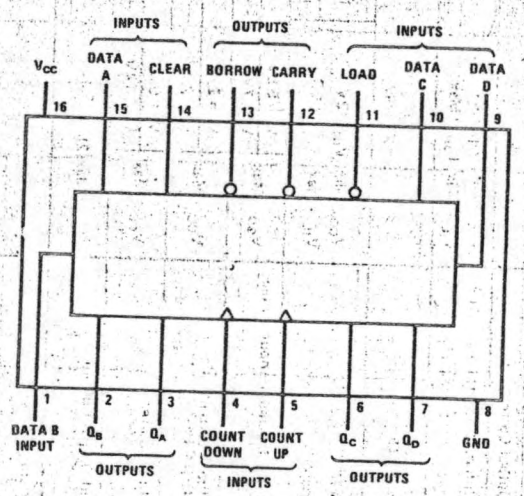
These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down counting functions. The borrow output produces a pulse equal in width to the count down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count down and count up inputs respectively of the succeeding counter.

Features

- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset each flip-flop

TYPE	TYPICAL COUNT FREQUENCY	TYPICAL POWER DISSIPATION
192, 193	25 MHz	325 mW
L192, L193	12 MHz	40 mW
LS192, LS193	32 MHz	95 mW

Connection Diagram



Note: Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D.

54192(J), (W); 74192(J), (N), (W); 54L192/74L192(J), (N), (W); 54LS192/74LS192(J), (N), (W); 54193(J), (W); 74193(J), (N), (W); 54L193/74L193(J), (N), (W); 54LS193/74LS193(J), (N), (W)

LS192, LS193 To Be Announced In 1976

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		CONDITIONS			DM54/74 192, 193			DM54L/74L L192, L193			DM54LS/74LS LS192, LS193			UNITS
					MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	MIN	TYP(1)	MAX	
V_{IH}	High Level Input Voltage				2			2			2			V
V_{IL}	Low Level Input Voltage			DM54			0.8			0.7			0.7	V
				DM74			0.8			0.7			0.8	
V_I	Input Clamp Voltage	V_{CC} = Min	I_I = −12 mA				−1.5			−1.5				V
			I_I = −18 mA										−1.5	
I_{OH}	High Level Output Current						−400			−200			−400	μA
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = Max, I_{OH} = Max		DM54	2.4			2.4			2.5	3.4		V
				DM74	2.4			2.4			2.7	3.4		
I_{OL}	Low Level Output Current			DM54			16			2			4	mA
				DM74			16			3.6			8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V V_{IL} = Max	I_{OL} = Max	DM54			0.4		0.15	0.3		0.25	0.4	V
				DM74			0.4		0.2	0.4		0.35	0.5	
			I_{OL} = 4 mA	DM74									0.4	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V				1			0.1				mA
			V_I = 7V										0.1	
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.4V				40		<1	10				μA
			V_I = 2.7V										20	
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.3V						−0.10	−0.18				mA
			V_I = 0.4V				−1.6						−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max(2)		DM54	−20		−55	−3	−9	−15	−30		−130	mA
				DM74	−18		−55	−3	−9	−15	−30		−130	
I_{CC}	Supply Current	V_{CC} = Max(3)		DM54		65	89		8	13		19	34	mA
				DM74		65	102		8	13		19	34	

Notes

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.

(2) Not more than one output should be shorted at a time, and for DM54LS/74LS duration of short circuit should not exceed one second.

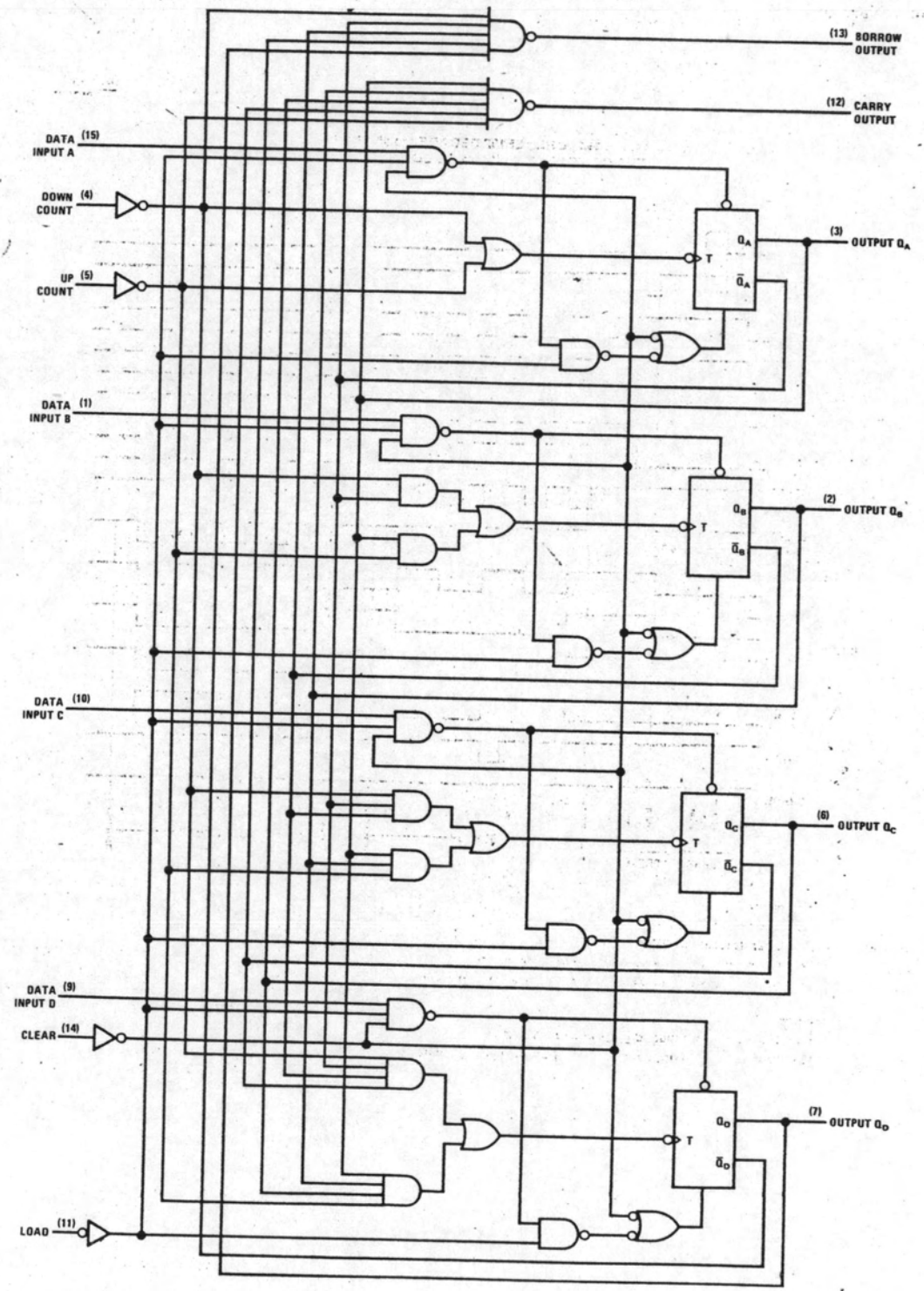
(3) I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5V.

Switching Characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		FROM INPUT	TO OUTPUT	DM54/74 192, 193				DM54L/74L L192, L193				DM54LS/74LS LS192, LS193				UNITS
				CONDITIONS	MIN	TYP	MAX	CONDITIONS	MIN	TYP	MAX	CONDITIONS	MIN	TYP	MAX	
f_{MAX}	Maximum Clock Frequency			C_L = 15 pF, R_L = 400Ω	20	25		C_L = 50 pF, R_L = 4 kΩ	6	12		C_L = 15 pF, R_L = 2 kΩ	25	32		MHz
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Count up	Carry			17	26			30	60			17	26	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					16	24			60	120			21	33	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Count down	Borrow			16	24			30	60			16	24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					16	24			50	100			21	33	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Either Count	Q			25	38			45	90			25	38	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					31	47			75	150			31	47	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Load	Q			27	40			55	110			27	40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					29	40			105	200			29	40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Clear	Q			22	35			95	190			22	35	ns
t_W	Width of Any Input Pulse				25				70				20			ns
t_{SETUP}	Data Setup Time				20				30				20			ns
t_{HOLD}	Data Hold Time				0				0				0			ns

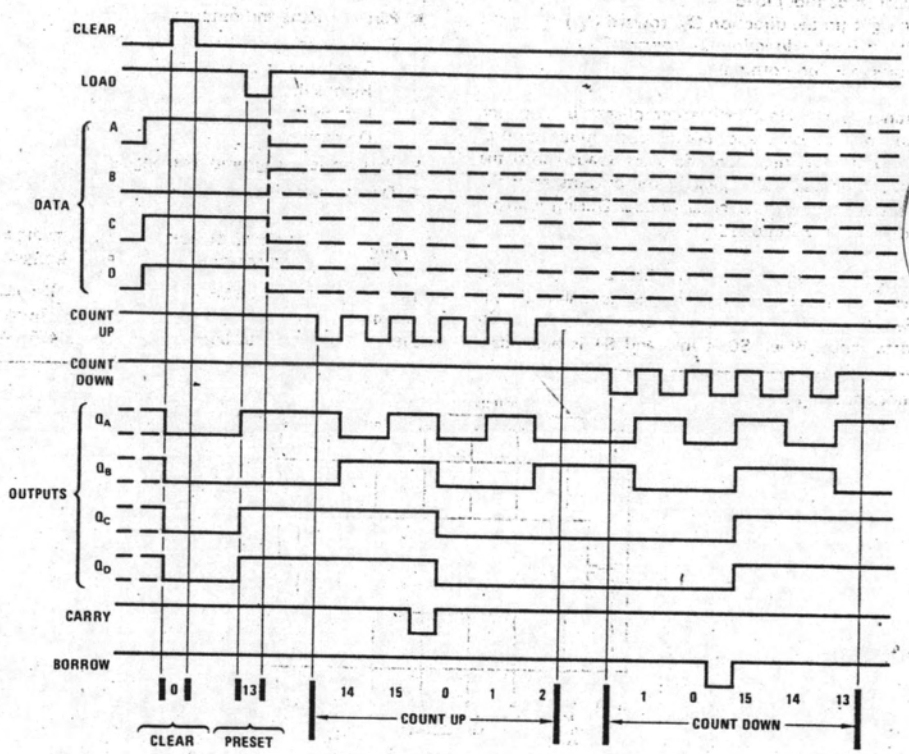
Logic Diagrams (Continued)

193, L193, LS193



Timing Diagrams (Continued)

193, L193, LS193 BINARY COUNTERS
TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES



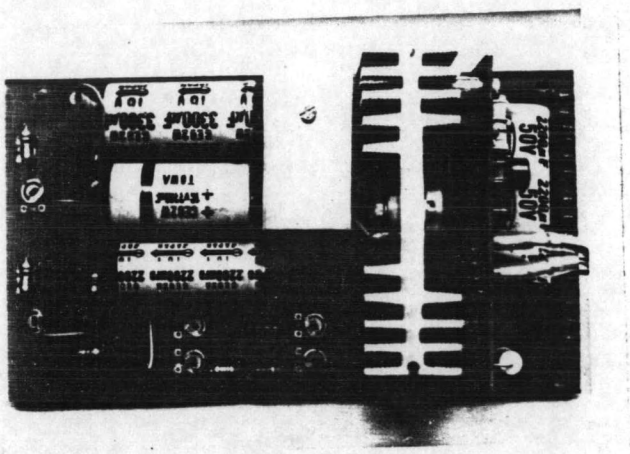
Sequence:

(1) Clear outputs to zero.
(2) Load (preset) to binary thirteen.
(3) Count up to fourteen, fifteen, carry, zero, one, and two.
(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

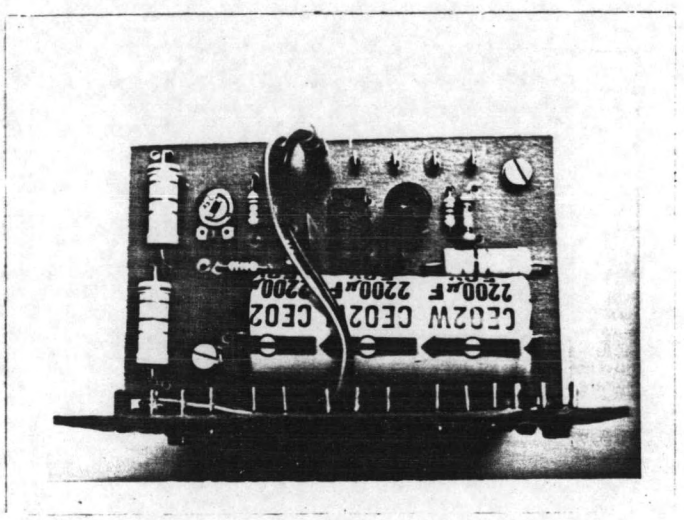
Notes:

(A) Clear overrides load, data, and count inputs.
(B) When counting up, count-down input must be high; when counting down, count-up input must be high.

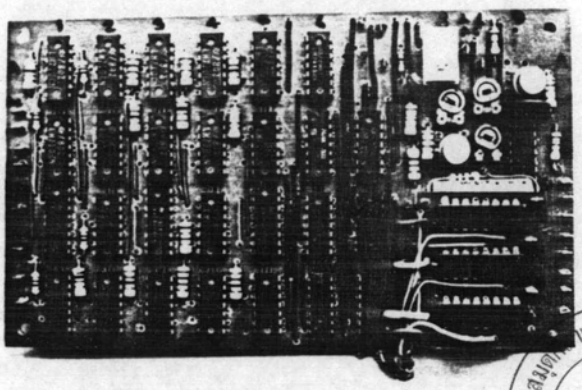
ภาคผนวก ค.



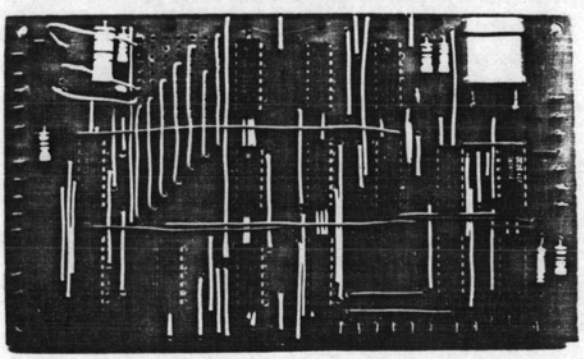
แผงวงจรแหล่งจ่ายไฟตรง



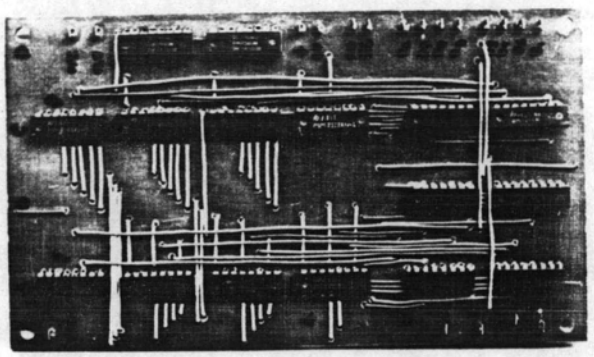
แผ่นวงจรย่อยที่เป็นส่วนของแผงวงจรแหล่งจ่ายไฟตรง



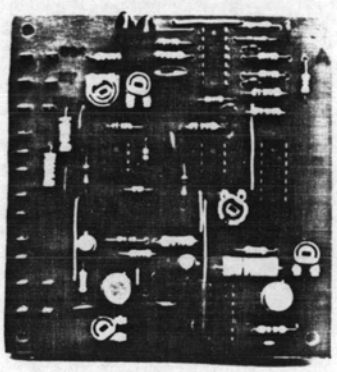
แผงวงจรแปลงสัญญาณ



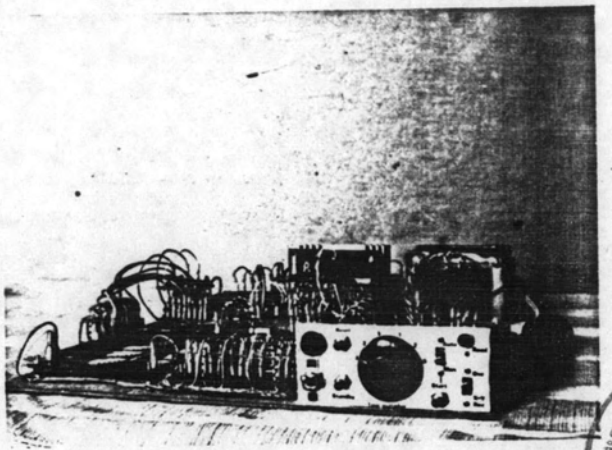
แผงวงจรควบคุม



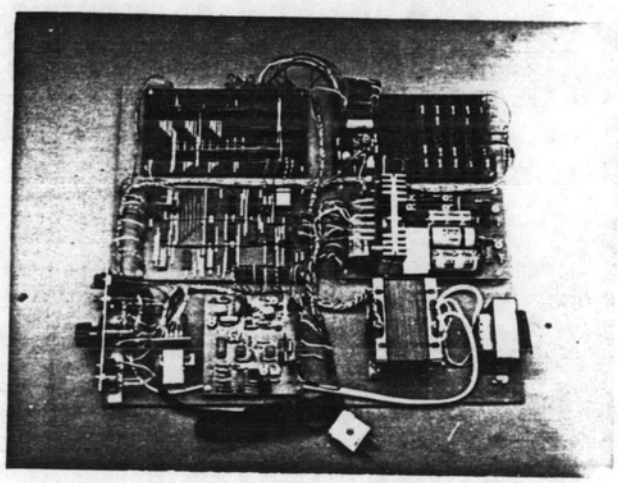
แผงวงจรจำ



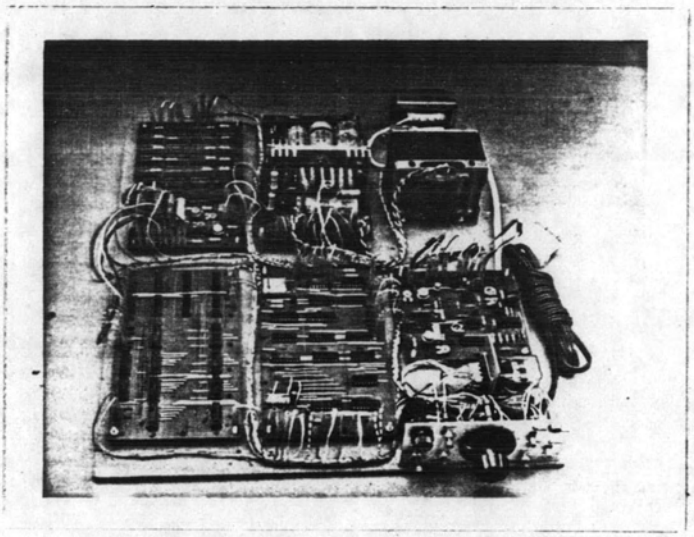
แผงวงจรภาคเข้าและภาคออก



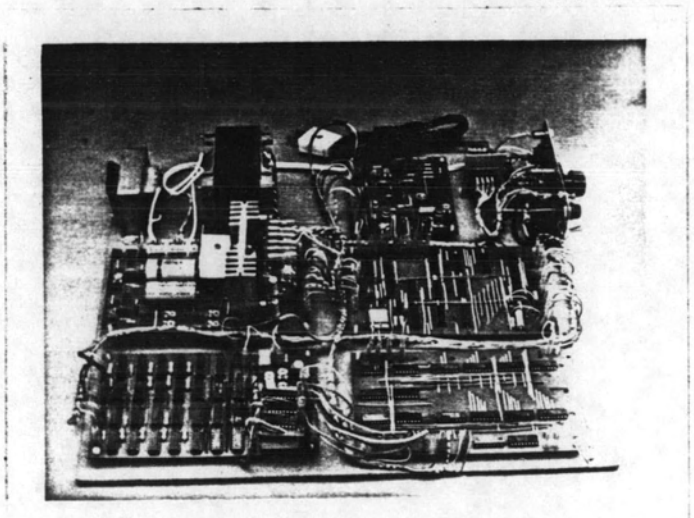
ระบบโดยสมบูรณ์ แสดงรายละเอียดหน้าปัทม์



ระบบโดยสมบูรณ์ มองจากด้านบน



มุมหนึ่งของระบบโดยสมบูรณ์



อีกมุมหนึ่งของระบบโดยสมบูรณ์

ประวัติผู้เขียน

นายประหยัด กรองอภิรดี เกิดวันที่ 8 พฤศจิกายน พ.ศ. 2494 ที่อำเภอแม่จัน จังหวัดเชียงราย วุฒิการศึกษา วิศวกรรมศาสตรบัณฑิต เกียรตินิยมอันดับหนึ่ง สาขาวิชาวิศวกรรมไฟฟ้า จากจุฬาลงกรณ์มหาวิทยาลัย ปี พ.ศ. 2517 มีประสบการณ์ทำงานในแผนกอีเล็คทรอนิคส์ และระบบสื่อสาร บริษัทไฟฟ้าฟิลิปส์แห่งประเทศไทย จำกัด เป็นเวลา 5 ปีเศษ ปัจจุบัน ศึกษาอยู่แผนก Computer Applications สถาบันเทคโนโลยีแห่งเอเชีย.