เอกสารอ้างอิง

1. ชวัช เมฆสวรรค์ และฟุมิโอะ มิคุมะ. เทคนิคการซ่อมเครื่องรับโทรทัศน์. พิมพ์ครั้งที่ 2. พระนคร: สำนักพิมพ์องค์การค้าของคุรุสภา, 2520.
2. Douglas V. Hall, Micro processors and digital system. New York : McGrall-Hill, 1980.
3. Arther A. Carapola, "CRT Monitor Design Using the Intel 8275," Interface Age. No.6, (June 1979): 92-105
4. Chris Tennant, "The Intel 8275 CRT Controller," Byte. No. 5, (may 1979): 130-148
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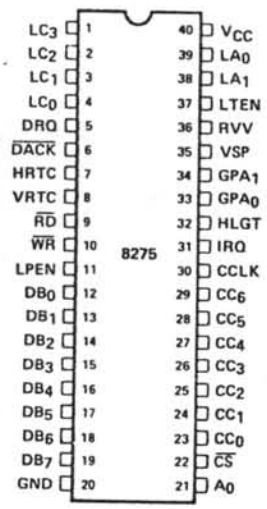
ภาคผนวก ก.

8275
PROGRAMMABLE CRT CONTROLLER

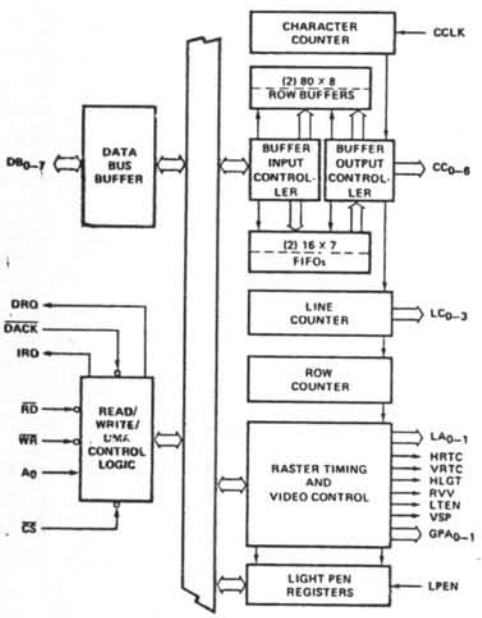
- Programmable Screen and Character Format
- 6 Independent Visual Field Attributes
- 11 Visual Character Attributes (Graphic Capability)
- Cursor Control (4 Types)
- Light Pen Detection and Registers
- Fully MCS-80™ and MCS-85™ Compatible
- Dual Row Buffers
- Programmable DMA Burst Mode
- Single +5V Supply
- 40-Pin Package

The Intel® 8275 Programmable CRT Controller is a single chip device to interface CRT raster scan displays with Intel® microcomputer systems. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the display position of the screen. The flexibility designed into the 8275 will allow simple interface to almost any raster scan CRT display with a minimum of external hardware and software overhead.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

DB_{0-7}	BI-DIRECTIONAL DATA BUS	LC_{0-3}	LINE COUNTER OUTPUTS
DRQ	DMA REQUEST OUTPUT	LA_{0-1}	LINE ATTRIBUTE OUTPUTS
$\overline{DACK}$	DMA ACKNOWLEDGE INPUT	HRTC	HORIZONTAL RETRACE OUTPUT
IRQ	INTERRUPT REQUEST OUTPUT	VRTC	VERTICAL RETRACE OUTPUT
$\overline{RD}$	READ STROBE INPUT	HLGT	HIGHLIGHT OUTPUT
$\overline{WR}$	WRITE STROBE INPUT	RVV	REVERSE VIDEO OUTPUT
A_0	REGISTER ADDRESS INPUT	LTEN	LIGHT ENABLE OUTPUT
CS	CHIP SELECT INPUT	VSP	VIDEO SUPPRESS OUTPUT
CCLK	CHARACTER CLOCK INPUT	GPA_{0-1}	GENERAL PURPOSE ATTRIBUTE OUTPUTS
CC_{0-6}	CHARACTER CODE OUTPUTS	LPEN	LIGHT PEN INPUT

PIN DESCRIPTIONS

Pin #	Pin Name	I/O	Pin Description
1	LC_3	O	Line count. Output from the line counter which is used to address the character generator for the line positions on the screen.
2	LC_2		
3	LC_1		
4	LC_0		
5	DRQ	O	DMA request. Output signal to the 8257 DMA controller requesting a DMA cycle.
6	$\overline{DACK}$	I	DMA acknowledge. Input signal from the 8257 DMA controller acknowledging that the requested DMA cycle has been granted.
7	HRTC	O	Horizontal retrace. Output signal which is active during the programmed horizontal retrace interval. During this period the VSP output is high and the LTEN output is low.
8	VRTC	O	Vertical retrace. Output signal which is active during the programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.
9	$\overline{RD}$	I	Read input. A control signal to read registers.
10	$\overline{WR}$	I	Write input. A control signal to write commands into the control registers or write data into the row buffers during a DMA cycle.
11	LPEN	I	Light pen. Input signal from the CRT system signifying that a light pen signal has been detected.
12	DB_0	I/O	Bi-directional three-state data bus lines. The outputs are enabled during a read of the C or P ports.
13	DB_1		
14	DB_2		
15	DB_3		
16	DB_4		
17	DB_5		
18	DB_6		
19	DB_7		
20	Ground		Ground

Pin #	Pin Name	I/O	Pin Description
40	V_{CC}		+5V power supply
39	LA_0	O	Line attribute codes. These attribute codes have to be decoded externally by the dot/timing logic to generate the horizontal and vertical line combinations for the graphic displays specified by the character attribute codes.
38	LA_1		
37	LTEN	O	Light enable. Output signal used to enable the video signal to the CRT. This output is active at the programmed underline cursor position, and at positions specified by attribute codes.
36	RVV	O	Reverse video. Output signal used to indicate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.
35	VSP	O	Video suppression. Output signal used to blank the video signal to the CRT. This output is active: – during the horizontal and vertical retrace intervals. – at the top and bottom lines of rows if underline is programmed to be number 8 or greater. – when an end of row or end of screen code is detected. – When a DMA underrun occurs. – at regular intervals (1/16 frame frequency for cursor, 1/32 frame frequency for character and field attributes) – to create blinking displays as specified by cursor, character attribute, or field attribute programming.
34	GPA_1	O	General purpose attribute codes. Outputs which are enabled by the general purpose field attribute codes.
33	GPA_0		
32	HLGT	O	Highlight. Output signal used to intensify the display at particular positions on the screen as specified by the character attribute codes or field attribute codes.
31	IRQ	O	Interrupt request.
30	CCLK	I	Character clock (from dot/timing logic).
29	CC_6	O	Character codes. Output from the row buffers used for character selection in the character generator.
28	CC_5		
27	CC_4		
26	CC_3		
25	CC_2		
24	CC_1		
23	CC_0		
22	$\overline{CS}$	I	Chip select. The read and write are enabled by $\overline{CS}$.
21	A_0	I	Port address. A high input on A_0 selects the "C" port or command registers and a low input selects the "P" port or parameter registers.

FUNCTIONAL DESCRIPTION

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the 8275 to the system Data Bus.

This functional block accepts inputs from the System Control Bus and generates control signals for overall device operation. It contains the Command, Parameter, and Status Registers that store the various control formats for the device functional definition.

A_0	OPERATION	REGISTER
0	Read	PREG
0	Write	PREG
1	Read	SREG
1	Write	CREG

$\overline{RD}$ (Read)

A "low" on this input informs the 8275 that the CPU is reading data or status information from the 8275.

$\overline{WR}$ (Write)

A "low" on this input informs the 8275 that the CPU is writing data or control words to the 8275.

$\overline{CS}$ (Chip Select)

A "low" on this input selects the 8275. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the Data Bus in the float state and $\overline{RD}$ and $\overline{WR}$ will have no effect on the chip.

DRQ (DMA Request)

A "high" on this output informs the DMA Controller that the 8275 desires a DMA transfer.

$\overline{DACK}$ (DMA Acknowledge)

A "low" on this input informs the 8275 that a DMA cycle is in progress.

IRQ (Interrupt Request)

A "high" on this output informs the CPU that the 8275 desires interrupt service.

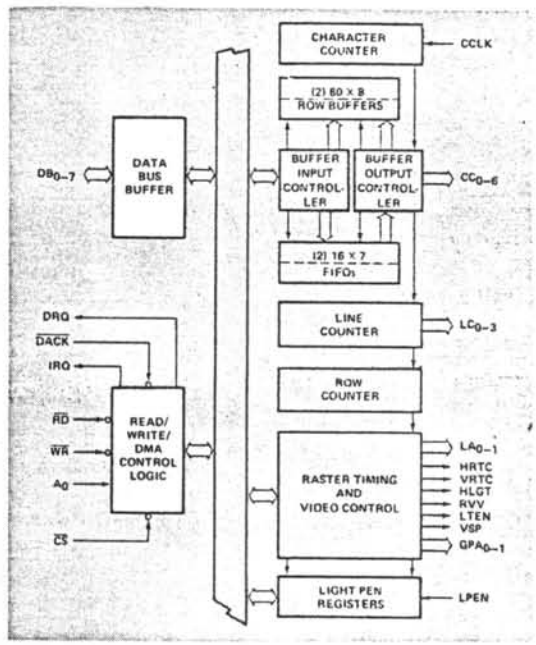


Figure 1. 8275 Block Diagram Showing Data Bus Buffer and Read/Write Functions

A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	1	0	0	Write 8275 Parameter
0	0	1	0	Read 8275 Parameter
1	1	0	0	Write 8275 Command
1	0	1	0	Read 8275 Status
X	1	1	0	Three-State
X	X	X	1	Three-state

Character Counter

The Character Counter is a programmable counter that is used to determine the number of characters to be displayed per row and the length of the horizontal retrace interval. It is driven by the CCLK (Character Clock) input, which should be a derivative of the external dot clock.

Line Counter

The Line Counter is a programmable counter that is used to determine the number of horizontal lines (Sweeps) per character row. Its outputs are used to address the external character generator ROM.

Row Counter

The Row Counter is a programmable counter that is used to determine the number of character rows to be displayed per frame and length of the vertical retrace interval.

Light Pen Registers

The Light Pen Registers are two registers that store the contents of the character counter and the row counter whenever there is a rising edge on the LPEN (Light Pen) input.

Note: Software correction is required.

Raster Timing and Video Controls

The Raster Timing circuitry controls the timing of the HRTC (Horizontal Retrace) and VRTC (Vertical Retrace) outputs. The Video Control circuitry controls the generation of LA_{0-1} (Line Attribute), HGLT (Highlight), RVV (Reverse Video), LTEN (Light Enable), VSP (Video Suppress), and GPA_{0-1} (General Purpose Attribute) outputs.

Row Buffers

The Row Buffers are two 80 character buffers. They are filled from the microcomputer system memory with the character codes to be displayed. While one row buffer is displaying a row of characters, the other is being filled with the next row of characters.

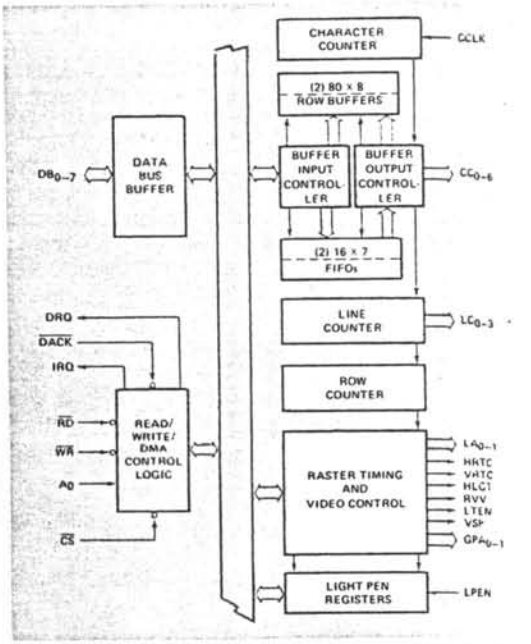


Figure 2. 8275 Block Diagram Showing Counter and Register Functions

FIFOs

There are two 16 character FIFOs in the 8275. They are used to provide extra row buffer length in the Transparent Attribute Mode (see Detailed Operation section).

Buffer Input/Output Controllers

The Buffer Input/Output Controllers decode the characters being placed in the row buffers. If the character is a character attribute, field attribute or special code, these controllers control the appropriate action. (Examples: An "End of Screen–Stop DMA" special code will cause the Buffer Input Controller to stop further DMA requests. A "Highlight" field attribute will cause the Buffer Output Controller to activate the HGLT output.)

SYSTEM OPERATION

The 8275 is programmable to a large number of different display formats. It provides raster timing, display row buffering, visual attribute decoding, cursor timing, and light pen detection.

It is designed to interface with the 8257 DMA Controller and standard character generator ROMs for dot matrix decoding. Dot level timing must be provided by external circuitry.

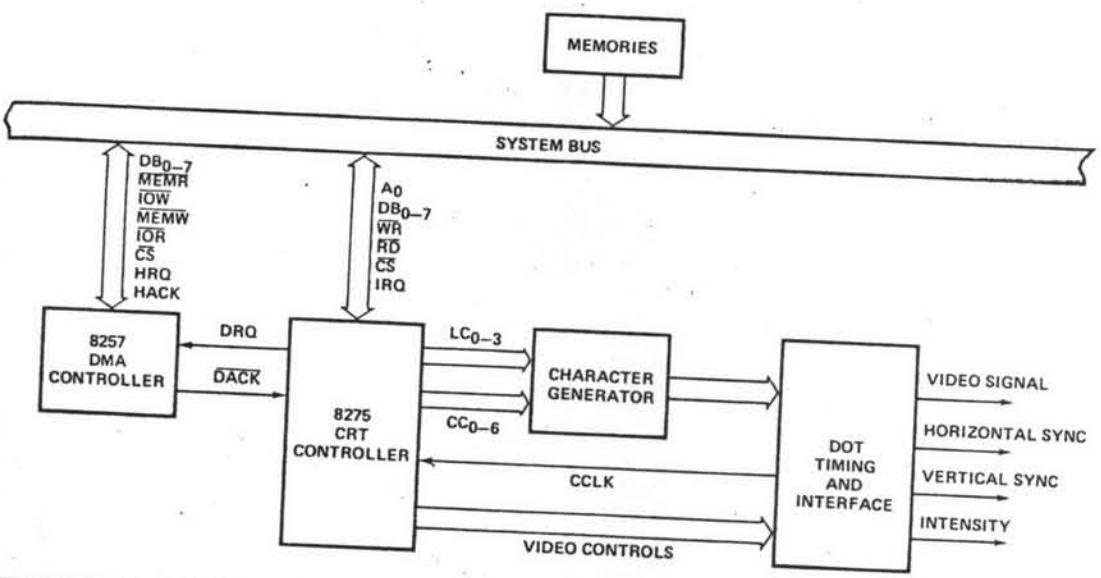


Figure 3. 8275 Systems Block Diagram Showing Systems Operation

General Systems Operational Description

The 8275 provides a "window" into the microcomputer system memory.

Display characters are retrieved from memory and displayed on a row by row basis. The 8275 has two row buffers. While one row buffer is being used for display, the other is being filled with the next row of characters to be displayed. The number of display characters per row and the number of character rows per frame are software programmable, providing easy interface to most CRT displays. (See Programming Section.)

The 8275 requests DMA to fill the row buffer that is not being used for display. DMA burst length and spacing is programmable. (See Programming Section.)

The 8275 displays character rows one line at a time.

The number of lines per character row, the underline position, and blanking of top and bottom lines are programmable. (See Programming Section.)

The 8275 provides special Control Codes which can be used to minimize DMA or software overhead. It also provides Visual Attribute Codes to cause special action or symbols on the screen without the use of the character generator (see Visual Attributes Section).

The 8275 also controls raster timing. This is done by generating Horizontal Retrace (HRTC) and Vertical Retrace (VRTC) signals. The timing of these signals is programmable.

The 8275 can generate a cursor. Cursor location and format are programmable. (See Programming Section.)

The 8275 has a light pen input and registers. The light pen input is used to load the registers. Light pen registers can be read on command. (See Programming Section.)

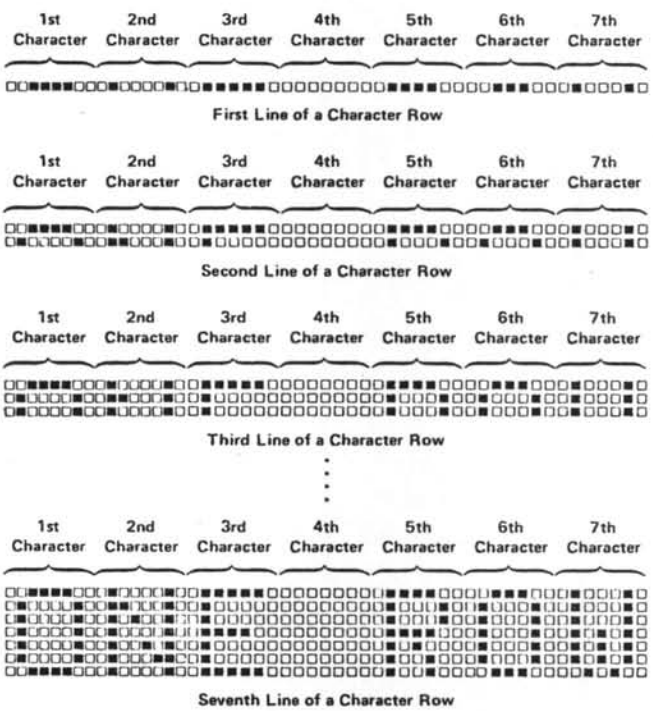


Figure 4. Display of a Character Row

Display Row Buffering

Before the start of a frame, the 8275 requests DMA and one row buffer is filled with characters.

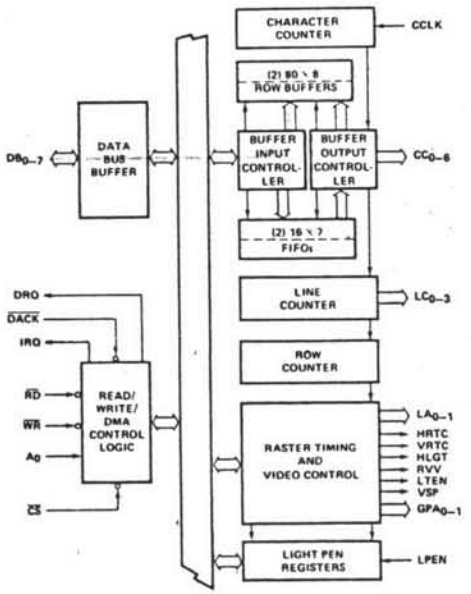


Figure 5. First Row Buffer Filled

When the first horizontal sweep is started, character codes are output to the character generator from the row buffer just filled. Simultaneously, DMA begins filling the other row buffer with the next row of characters.

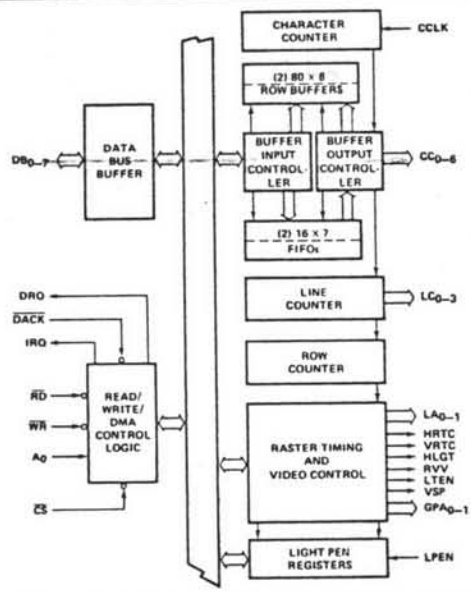


Figure 6. Second Buffer Filled, First Row Displayed

After all the lines of the character row are scanned, the roles of the two row buffers are reversed and the same procedure is followed for the next row.

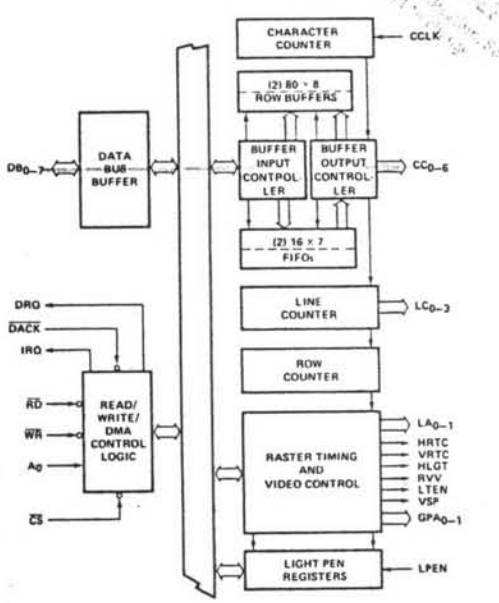


Figure 7. First Buffer Filled with Third Row, Second Row Displayed

This is repeated until all of the character rows are displayed.

Display Format

Screen Format

The 8275 can be programmed to generate from 1 to 80 characters per row, and from 1 to 64 rows per frame.

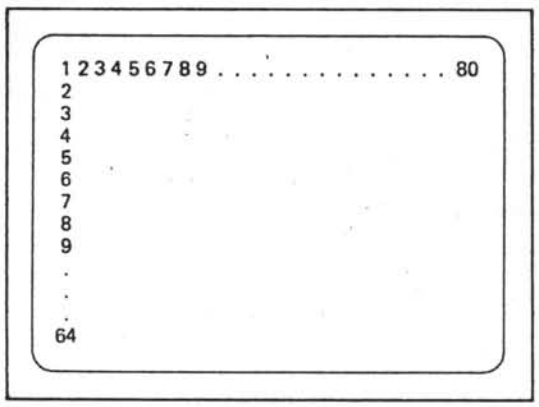


Figure 8. Screen Format

The 8275 can also be programmed to blank alternate rows. In this mode, the first row is displayed, the second blanked, the third displayed, etc. DMA is not requested for the blanked rows.

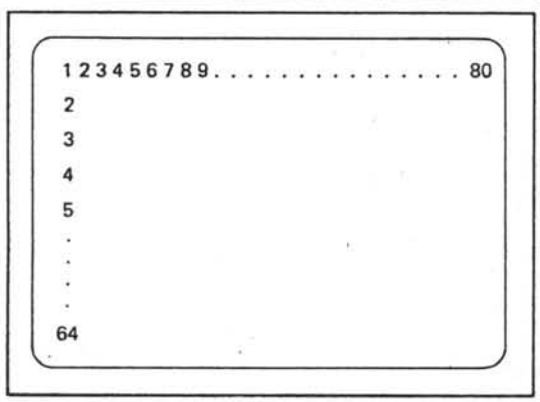


Figure 9. Blank Alternate Rows Mode

Row Format

The 8275 is designed to hold the line count stable while outputting the appropriate character codes during each horizontal sweep. The line count is incremented during horizontal retrace and the whole row of character codes are output again during the next sweep. This is continued until the whole character row is displayed.

The number of lines (horizontal sweeps) per character row is programmable from 1 to 16.

The output of the line counter can be programmed to be in one of two modes.

In mode 0, the output of the line *counter* is the same as the line *number*.

In mode 1, the line *counter* is offset by one from the line *number*.

Note: In mode 1, while the *first* line (line number 0) is being displayed, the *last* count is output by the line counter (see examples).

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □ □ □	0000	1111
1	□ □ □ □ ■ □ □ □ □	0001	0000
2	□ □ □ ■ □ ■ □ □ □	0010	0001
3	□ □ ■ □ □ □ ■ □ □	0011	0010
4	□ ■ □ □ □ □ □ ■ □	0100	0011
5	□ ■ □ □ □ □ □ ■ □	0101	0100
6	□ ■ ■ ■ ■ ■ ■ ■ □	0110	0101
7	□ ■ □ □ □ □ □ ■ □	0111	0110
8	□ ■ □ □ □ □ □ ■ □	1000	0111
9	□ ■ □ □ □ □ □ ■ □	1001	1000
10	□ □ □ □ □ □ □ □ □	1010	1001
11	□ □ □ □ □ □ □ □ □	1011	1010
12	□ □ □ □ □ □ □ □ □	1100	1011
13	□ □ □ □ □ □ □ □ □	1101	1100
14	□ □ □ □ □ □ □ □ □	1110	1101
15	□ □ □ □ □ □ □ □ □	1111	1110

Figure 10. Example of a 16-Line Format

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □	0000	1001
1	□ □ □ ■ □ □ □	0001	0000
2	□ □ ■ □ ■ □ □	0010	0001
3	□ ■ □ □ □ ■ □	0011	0010
4	□ ■ □ □ □ ■ □	0100	0011
5	□ ■ ■ ■ ■ ■ □	0101	0100
6	□ ■ □ □ □ ■ □	0110	0101
7	□ ■ □ □ □ ■ □	0111	0110
8	□ □ □ □ □ □ □	1000	0111
9	□ □ □ □ □ □ □	1001	1000

Figure 11. Example of a 10-Line Format

Mode 0 is useful for character generators that leave address zero blank and start at address 1. Mode 1 is useful for character generators which start at address zero.

Underline placement is also programmable (from line *number* 0 to 15). This is independent of the line *counter* mode.

If the line *number* of the underline is greater than 7 (line *number* MSB = 1), then the top and bottom lines will be blanked.

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □ □	0000	1011
1	□ □ □ □ ■ □ □ □	0001	0000
2	□ □ □ ■ □ ■ □ □	0010	0001
3	□ □ ■ □ □ □ ■ □	0011	0010
4	□ ■ □ □ □ □ ■ □	0100	0011
5	□ ■ □ □ □ □ ■ □	0101	0100
6	□ ■ ■ ■ ■ ■ ■ □	0110	0101
7	□ ■ □ □ □ □ ■ □	0111	0110
8	□ ■ □ □ □ □ ■ □	1000	0111
9	□ ■ □ □ □ □ ■ □	1001	1000
10	■ ■ ■ ■ ■ ■ ■ ■	1010	1001
11	□ □ □ □ □ □ □ □	1011	1010

Top and Bottom Lines are Blanked

Figure 12. Underline in Line Number 10

If the line *number* of the underline is less than or equal to 7 (line *number* MSB = 0), then the top and bottom lines will *not* be blanked.

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ ■ □ □ □	0000	0111
1	□ □ ■ □ ■ □ □	0001	0000
2	□ ■ □ □ □ ■ □	0010	0001
3	□ ■ □ □ □ ■ □	0011	0010
4	□ ■ ■ ■ ■ ■ □	0100	0011
5	□ ■ □ □ □ ■ □	0101	0100
6	□ ■ □ □ □ ■ □	0110	0101
7	■ ■ ■ ■ ■ ■ ■	0111	0110

Top and Bottom Lines are not Blanked

Figure 13. Underline in Line Number 7

If the line *number* of the underline is greater than the maximum number of lines, the underline will not appear.

Blanking is accomplished by the VSP (Video Suppression) signal. Underline is accomplished by the LTEN (Light Enable) signal.

Dot Format

Dot width and character width are dependent upon the external timing and control circuitry.

Dot level timing circuitry should be designed to accept the parallel output of the character generator and shift it out serially at the rate required by the CRT display.

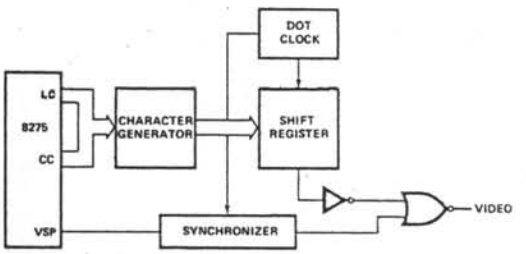


Figure 14. Typical Dot Level Block Diagram

Dot width is a function of dot clock frequency.

Character width is a function of the character generator width.

Horizontal character spacing is a function of the shift register length.

Note: Video control and timing signals must be synchronized with the video signal due to the character generator access delay.

Raster Timing

The character counter is driven by the character clock input (CCLK). It counts out the characters being displayed (programmable from 1 to 80). It then causes the line counter to increment, and it starts counting out the horizontal retrace interval (programmable from 2 to 32). This is constantly repeated.

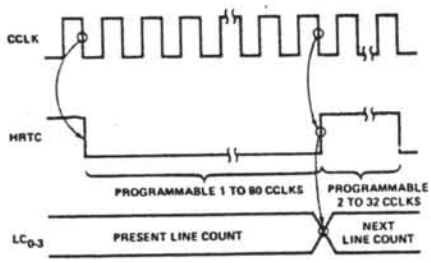


Figure 15. Line Timing

The line counter is driven by the character counter. It is used to generate the line address outputs (LC_{0-3}) for the character generator. After it counts all of the lines in a character row (programmable from 1 to 16), it increments the row counter, and starts over again. (See Character Format Section for detailed description of Line Counter functions.)

The row counter is an internal counter driven by the line counter. It controls the functions of the row buffers and counts the number of character rows displayed.

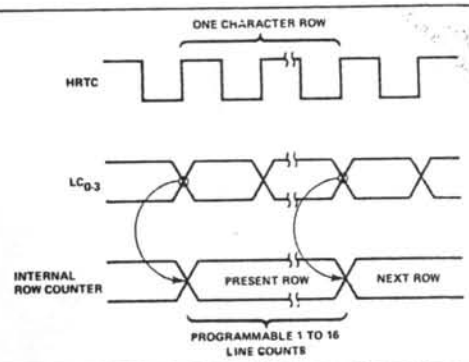


Figure 16. Row Timing

After the row counter counts all of the rows in a frame (programmable from 1 to 64), it starts counting out the vertical retrace interval (programmable from 1 to 4).

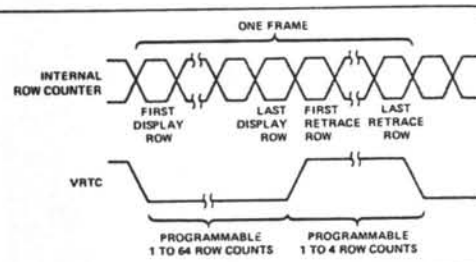


Figure 17. Frame Timing

The Video Suppression Output (VSP) is active during horizontal and vertical retrace intervals.

Dot level timing circuitry must synchronize these outputs with the video signal to the CRT Display.

DMA Timing

The 8275 can be programmed to request burst DMA transfers of 1 to 8 characters. The interval between bursts is also programmable (from 0 to 55 character clock periods ±1). This allows the user to tailor his DMA overhead to fit his system needs.

The first DMA request of the frame occurs one *row time* before the end of vertical retrace. DMA requests continue as programmed, until the row buffer is filled. If the row buffer is filled in the middle of a burst, the 8275 terminates the burst and resets the burst counter. No more DMA requests will occur until the *beginning* of the *next* row. At that time, DMA requests are activated as programmed until the other buffer is filled.

If, for any reason, there is a DMA underrun, a flag in the status word will be set.

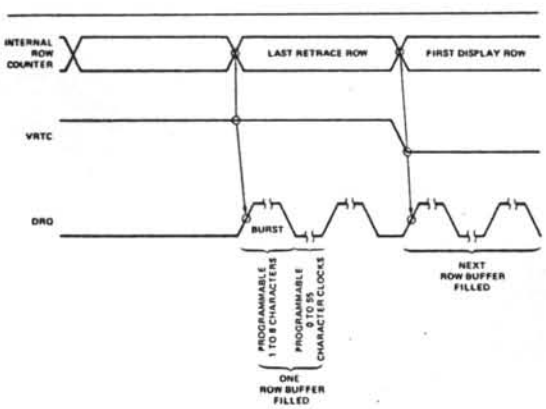


Figure 18. DMA Timing

The DMA controller is typically initialized for the next frame at the end of the current frame.

Interrupt Timing

The 8275 can be programmed to generate an interrupt request at the end of each frame. This can be used to reinitialize the DMA controller. If the 8275 interrupt enable flag is set, an interrupt request will occur at the *beginning* of the *last display row*.

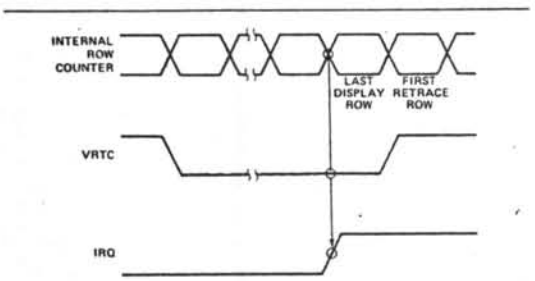


Figure 19. Beginning of Interrupt Request

IRQ will go inactive after the status register is read.

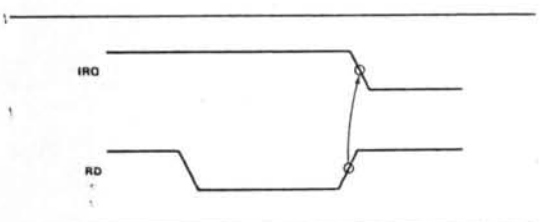


Figure 20. End of Interrupt Request

A reset command will also cause IRQ to go inactive, but this is not recommended during normal service.

Another method of reinitializing the DMA controller is to have the DMA controller itself interrupt on terminal count. With this method, the 8275 interrupt enable flag should not be set.

Note: Upon power-up, the 8275 Interrupt Enable Flag may be set. As a result, the user's cold start routine should write a reset command to the 8275 before system interrupts are enabled.

VISUAL ATTRIBUTES AND SPECIAL CODES

The characters processed by the 8275 are 8-bit quantities. The character code outputs provide the character generator with 7 bits of address. The Most Significant Bit is the extra bit and it is used to determine if it is a normal display character (MSB = 0), or if it is a Visual Attribute or Special Code (MSB = 1).

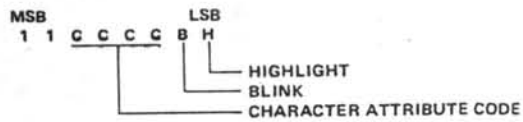
There are two types of Visual Attribute Codes. They are Character Attributes and Field Attributes.

Character Attribute Codes

Character attribute codes are codes that can be used to generate graphics symbols without the use of a character generator. This is accomplished by selectively activating the Line Attribute outputs (LA_{0-1}), the Video Suppression output (VSP), and the Light Enable output. The dot level timing circuitry can use these signals to generate the proper symbols.

Character attributes can be programmed to blink or be highlighted individually. Blinking is accomplished with the Video Suppression output (VSP). Blink frequency is equal to the screen refresh frequency divided by 32. Highlighting is accomplished by activating the Highlight output (HGLT).

Character Attributes



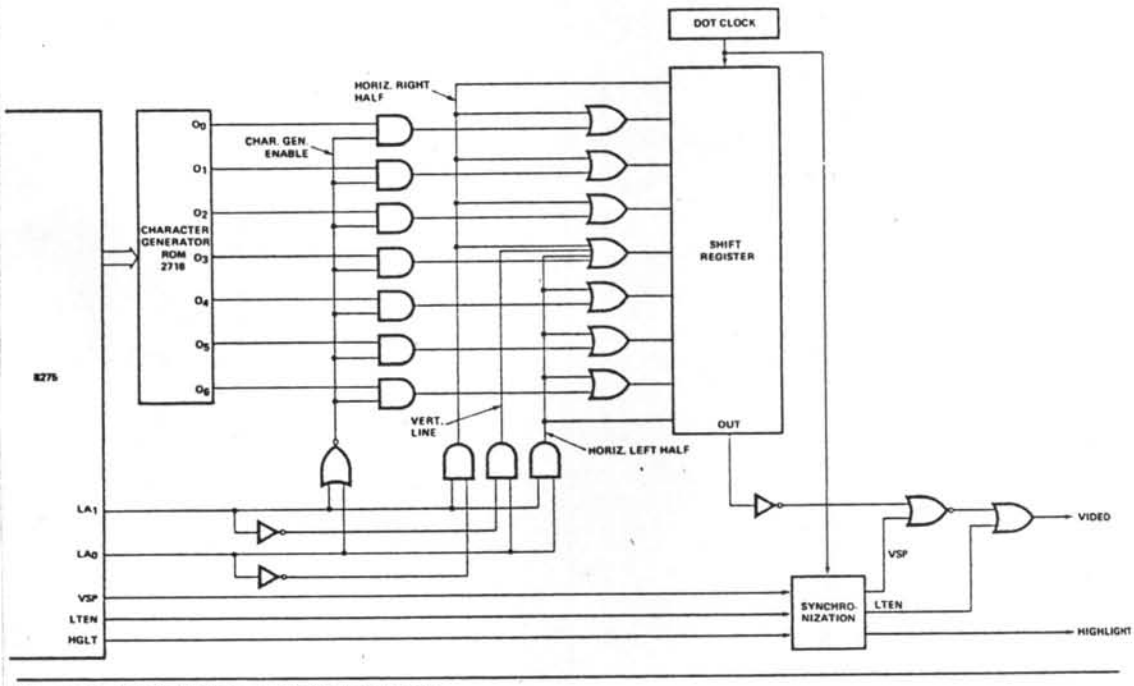


Figure 21. Typical Character Attribute Logic

Character attributes were designed to produce the following graphics:

CHARACTER ATTRIBUTE CODE "CCCC"		OUTPUTS LA_1	LA_0	VSP	LTEN	SYMBOL	DESCRIPTION
0000	Above Underline	0	0	1	0		Top Left Corner
	Underline	1	0	0	0		
	Below Underline	0	1	0	0		
0001	Above Underline	0	0	1	0		Top Right Corner
	Underline	1	1	0	0		
	Below Underline	0	1	0	0		
0010	Above Underline	0	1	0	0		Bottom Left Corner
	Underline	1	0	0	0		
	Below Underline	0	0	1	0		
0011	Above Underline	0	1	0	0		Bottom Right Corner
	Underline	1	1	0	0		
	Below Underline	0	0	1	0		
0100	Above Underline	0	0	1	0		Top Intersect
	Underline	0	0	0	1		
	Below Underline	0	1	0	0		
0101	Above Underline	0	1	0	0		Right Intersect
	Underline	1	1	0	0		
	Below Underline	0	1	0	0		
0110	Above Underline	0	1	0	0		Left Intersect
	Underline	1	0	0	0		
	Below Underline	0	1	0	0		
0111	Above Underline	0	1	0	0		Bottom Intersect
	Underline	0	0	0	1		
	Below Underline	0	0	1	0		
1000	Above Underline	0	0	1	0		Horizontal Line
	Underline	0	0	0	1		
	Below Underline	0	0	1	0		
1001	Above Underline	0	1	0	0		Vertical Line
	Underline	0	1	0	0		
	Below Underline	0	1	0	0		
1010	Above Underline	0	1	0	0		Crossed Lines
	Underline	0	0	0	1		
	Below Underline	0	1	0	0		
1011	Above Underline	0	0	0	0		Not Recommended *
	Underline	0	0	0	0		
	Below Underline	0	0	0	0		
1100	Above Underline	0	0	1	0		Special Codes
	Underline	0	0	1	0		
	Below Underline	0	0	1	0		
1101	Above Underline						Illegal
	Underline		Undefined				
	Below Underline						
1110	Above Underline						Illegal
	Underline		Undefined				
	Below Underline						
1111	Above Underline						Illegal
	Underline		Undefined				
	Below Underline						

*Character Attribute Code 1011 is not recommended for normal operation. Since none of the attribute outputs are active, the character Generator will not be disabled, and an indeterminate character will be generated.

Character Attribute Codes 1101, 1110, and 1111 are illegal.

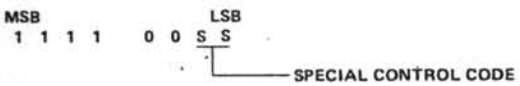
Blinking is active when B = 1.

Highlight is active when H = 1.

Special Codes

Four special codes are available to help reduce memory, software, or DMA overhead.

Special Control Character



S S	FUNCTION
0 0	End of Row
0 1	End of Row-Stop DMA
1 0	End of Screen
1 1	End of Screen-Stop DMA

The End of Row Code (00) activates VSP and holds it to the end of the line.

The End of Row-Stop DMA Code (01) causes the DMA Control Logic to stop DMA for the rest of the row when it is written into the Row Buffer. It affects the display in the same way as the End of Row Code (00).

The End of Screen Code (10) activates VSP and holds it to the end of the frame.

The End of Screen-Stop DMA Code (11) causes the DMA Control Logic to stop DMA for the rest of the frame when it is written into the Row Buffer. It affects the display in the same way as the End of Screen Code (10).

If the Stop DMA feature is not used, all characters after an End of Row character are ignored, except for the End of Screen character, which operates normally. All characters after an End of Screen character are ignored.

Note: If a Stop DMA character is not the last character in a burst or row, DMA is not stopped until after the next character is read. In this situation, a dummy character must be placed in memory after the Stop DMA character.

Field Attributes

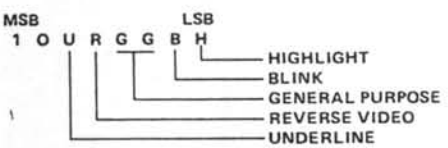
The field attributes are control codes which affect the visual characteristics for a field of characters, starting-at the character following the code up to, and including, the character which precedes the *next* field attribute code, or up to the end of the frame. The field attributes are reset during the vertical retrace interval.

There are six field attributes:

1. *Blink* – Characters following the code are caused to blink by activating the Video Suppression output (VSP). The blink frequency is equal to the screen refresh frequency divided by 32.
2. *Highlight* – Characters following the code are caused to be highlighted by activating the Highlight output (HGLT).
3. *Reverse Video* – Characters following the code are caused to appear with reverse video by activating the Reverse Video output (RVV).
4. *Underline* – Characters following the code are caused to be underlined by activating the Light Enable output (LTEN).

5,6. *General Purpose* – There are two additional 8275 outputs which act as general purpose, independently programmable field attributes. GPA_{0-1} are active high outputs.

Field Attribute Code



H = 1 FOR HIGHLIGHTING
B = 1 FOR BLINKING
R = 1 FOR REVERSE VIDEO
U = 1 FOR UNDERLINE
GG = GPA_1, GPA_0

The 8275 can be programmed to provide visible or invisible field attribute characters.

If the 8275 is programmed in the visible field attribute mode, all field attributes will occupy a position on the screen. They will appear as blanks caused by activation of the Video Suppression output (VSP). The chosen visual attributes are activated after this blanked character.

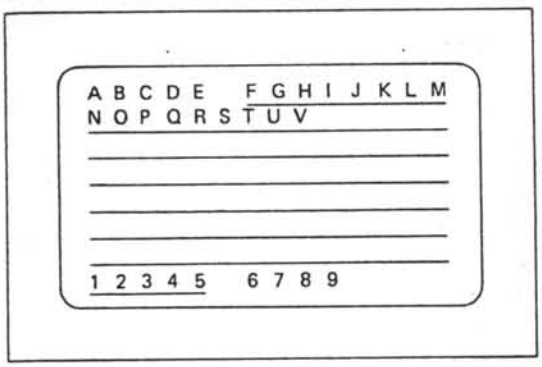


Figure 22. Example of the Visible Field Attribute Mode (Underline Attribute)

If the 8275 is programmed in the invisible field attribute mode, the 8275 FIFO is activated.

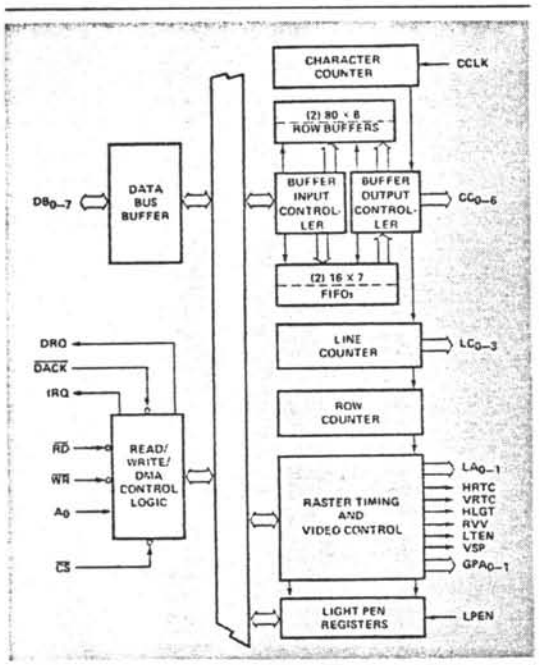


Figure 23. Block Diagram Showing FIFO Activation

Each row buffer has a corresponding FIFO. These FIFOs are 16 characters by 7 bits in size.

When a field attribute is placed in the row buffer during DMA, the buffer input controller recognizes it and places the *next* character in the proper FIFO.

When a field attribute is placed in the Buffer Output Controller during display, it causes the controller to immediately put a character from the FIFO on the Character Code outputs (CC_{0-6}). The chosen Visual Attributes are also activated.

Since the FIFO is 16 characters long, no more than 16 field attribute characters may be used per line in this mode. If more are used, a bit in the status word is set and the first characters in the FIFO are written over and lost.

Note: Since the FIFO is 7 bits wide, the MSB of any characters put in it are stripped off. Therefore, a Visual Attribute or Special Code must *not* immediately follow a field attribute code. If this situation does occur, the Visual Attribute or Special Code will be treated as a normal display character.

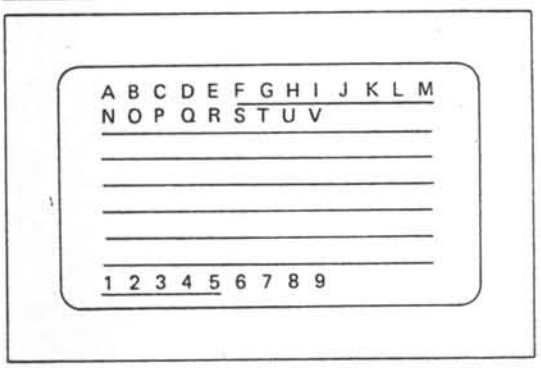


Figure 24. Example of the Invisible Field Attribute Mode (Underline Attribute)

Field and Character Attribute Interaction

Character Attribute Symbols are affected by the Reverse Video (RRV) and General Purpose (GPA_{0-1}) field attributes. They are not affected by Underline, Blink or Highlight field attributes; however, these characteristics can be programmed *individually* for Character Attribute Symbols.

Cursor Timing

The cursor location is determined by a cursor row register and a character position register which are loaded by command to the controller. The cursor can be programmed to appear on the display as:

1. a blinking underline
2. a blinking reverse video block
3. a non-blinking underline
4. a non-blinking reverse video block

The cursor blinking frequency is equal to the screen refresh frequency divided by 16.

If a non-blinking reverse video *cursor* appears in a non-blinking reverse video *field*, the cursor will appear as a normal video block.

If a non-blinking underline *cursor* appears in a non-blinking underline *field*, the cursor will not be visible.

Light Pen Detection

A light pen consists of a micro switch and a tiny light sensor. When the light pen is pressed against the CRT screen, the micro switch enables the light sensor. When the raster sweep reaches the light sensor, it triggers the light pen output.

If the output of the light pen is presented to the 8275 LPEN input, the row and character position coordinates are stored in a pair of registers. These registers can be read on command. A bit in the status word is set, indicating that the light pen signal was detected. The LPEN input must be a 0 to 1 transition for proper operation.

Note: Due to internal and external delays, the character position coordinate will be off by at least three character positions. This has to be corrected in software.

Device Programming

The 8275 has two programming registers, the Command Register (CREG) and the Parameter Register (PREG). It also has a Status Register (SREG). The Command Register can only be written into and the Status Registers can only be read from. They are addressed as follows:

A_0	OPERATION	REGISTER
0	Read	PREG
0	Write	PREG
1	Read	SREG
1	Write	CREG

The 8275 expects to receive a command and a sequence of 0 to 4 parameters, depending on the command. If the proper number of parameter bytes are not received before another command is given, a status flag is set, indicating an improper command.

Instruction Set

The 8275 instruction set consists of 8 commands.

COMMAND	NO. OF PARAMETER BYTES
Reset	4
Start Display	0
Stop Display	0
Read Light Pen	2
Load Cursor	2
Enable Interrupt	0
Disable Interrupt	0
Preset Counters	0

In addition, the status of the 8275 (SREG) can be read by the CPU at any time.

1. Reset Command:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Reset Command	0	0	0	0	0	0	0	0
Parameters	Write	0	Screen Comp Byte 1	S	H	H	H	H	H	H	H
	Write	0	Screen Comp Byte 2	V	V	R	R	R	R	R	R
	Write	0	Screen Comp Byte 3	U	U	U	U	L	L	L	L
	Write	0	Screen Comp Byte 4	M	F	C	C	Z	Z	Z	Z

Action – After the reset command is written, DMA requests stop, 8275 interrupts are disabled, and the VSP output is used to blank the screen. HRTC and VRTC continue to run. HRTC and VRTC timing are random on power-up.

As parameters are written, the screen composition is defined.

Parameter – S Spaced Rows

S	FUNCTIONS
0	Normal Rows
1	Spaced Rows

Parameter – HHHHHHH Horizontal Characters/Row

H H H H H H H	NO. OF CHARACTERS PER ROW
0 0 0 0 0 0 0	1
0 0 0 0 0 0 1	2
0 0 0 0 0 1 0	3
.	.
.	.
.	.
1 0 0 1 1 1 1	80
1 0 1 0 0 0 0	Undefined
.	.
.	.
.	.
1 1 1 1 1 1 1	Undefined

Parameter – VV Vertical Retrace Row Count

V V	NO. OF ROW COUNTS PER VRTC
0 0	1
0 1	2
1 0	3
1 1	4

Parameter – RRRRRR Vertical Rows/Frame

R R R R R R	NO. OF ROWS/FRAME
0 0 0 0 0 0	1
0 0 0 0 0 1	2
0 0 0 0 1 0	3
.	.
.	.
.	.
1 1 1 1 1 1	64

Parameter – UUUU Underline Placement

U U U U	LINE NUMBER OF UNDERLINE
0 0 0 0	1
0 0 0 1	2
0 0 1 0	3
.	.
.	.
.	.
1 1 1 1	16

Parameter – LLLL Number of Lines per Character Row

L L L L	NO. OF LINES/ROW
0 0 0 0	1
0 0 0 1	2
0 0 1 0	3
.	.
.	.
.	.
1 1 1 1	16

Parameter – M Line Counter Mode

M	LINE COUNTER MODE
0	Mode 0 (Non-Offset)
1	Mode 1 (Offset by 1 Count)

Parameter – F Field Attribute Mode

F	FIELD ATTRIBUTE MODE
0	Transparent
1	Non-Transparent

Parameter – CC Cursor Format

C C	CURSOR FORMAT
0 0	Blinking reverse video block
0 1	Blinking underline
1 0	Nonblinking reverse video block
1 1	Nonblinking underling

Parameter – ZZZZ Horizontal Retrace Count

Z Z Z Z	NO. OF CHARACTER COUNTS PER HRTC
0 0 0 0	2
0 0 0 1	4
0 0 1 0	6
.	.
.	.
.	.
1 1 1 1	32

Note: uuuu MSB determines blanking of top and bottom lines (1 = blanked, 0 = not blanked).

2. Start Display Command:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Start Display	0	0	1	S	S	S	B	B
No parameters											

S S S BURST SPACE CODE

S S S	NO. OF CHARACTER CLOCKS BETWEEN DMA REQUESTS
0 0 0	0
0 0 1	7
0 1 0	15
0 1 1	23
1 0 0	31
1 0 1	39
1 1 0	47
1 1 1	55

B B BURST COUNT CODE

B B	NO. OF DMA CYCLES PER BURST
0 0	1
0 1	2
1 0	4
1 1	8

Action – 8275 interrupts are enabled, DMA requests begin, video is enabled, Interrupt Enable and Video Enable status flags are set.

3. Stop Display Command:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Stop Display	0	1	0	0	0	0	0	0
No parameters											

Action – Disables video, interrupts remain enabled, HRTC and VRTC continue to run, Video Enable status flag is reset, and the "Start Display" command must be given to re-enable the display.

4. Read Light Pen Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Read Light Pen	0	1	1	0	0	0	0	0
Parameters	Read	0	Char. Number	(Char. Position in Row)							
	Read	0	Row Number	(Row Number)							

Action – The 8275 is conditioned to supply the contents of the light pen position registers in the next two read cycles of the parameter register. Status flags are not affected.

Note: Software correction of light pen position is required.

5. Load Cursor Position:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Load Cursor	1	0	0	0	0	0	0	0
Parameters	Write	0	Char. Number	(Char. Position in Row)							
	Write	0	Row Number	(Row Number)							

Action – The 8275 is conditioned to place the next two parameter bytes into the cursor position registers. Status flags not affected.

6. Enable Interrupt Command:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Enable Interrupt	1	0	1	0	0	0	0	0
No parameters											

Action – The interrupt enable status flag is set and interrupts are enabled.

7. Disable Interrupt Command:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Disable Interrupt	1	1	0	0	0	0	0	0
No parameters											

Action – Interrupts are disabled and the interrupt enable status flag is reset.

8. Preset Counters Command:

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB							LSB
Command	Write	1	Preset Counters	1	1	1	0	0	0	0	0
No parameters											

Action – The internal timing counters are preset, corresponding to a screen display position at the top left corner. Two character clocks are required for this operation. The counters will remain in this state until any other command is given.

This command is useful for system debug and synchronization of clustered CRT displays on a single CPU.

Status Flags

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Read	1	Status Word	0 IE IR LP IC VE OU F0

IE – (Interrupt Enable) Set or reset by command. It enables vertical retrace interrupt. It is automatically set by a "Start Display" command and reset with the "Reset" command.

IR – (Interrupt Request) This flag is set at the beginning of display of the last row of the frame if the interrupt enable flag is set. It is reset after a status read operation.

LP – This flag is set when the light pen input (LPEN) is activated and the light pen registers have been loaded. This flag is automatically reset after a status read.

IC – (Improper Command) This flag is set when a command parameter string is too long or too short. The flag is automatically reset after a status read.

VE – (Video Enable) This flag indicates that video operation of the CRT is enabled. This flag is set on a "Start Display" command, and reset on a "Stop Display" or "Reset" command.

DU – (DMA Underrun) This flag is set whenever a data underrun occurs during DMA transfers. Upon detection of DU, the DMA operation is stopped and the screen is blanked until after the vertical retrace interval. This flag is reset after a status read.

FO – (FIFO Overrun) This flag is set whenever the FIFO is overrun. It is reset on a status read.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage On Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. CHARACTERISTICS

$T_A = 0°C$ to $70°C$; $V_{CC} = 5V \pm 5\%$

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	$I_{OL} = 2.2$ mA
V_{OH}	Output High Voltage	2.4		V	$I_{OH} = -400\ \mu A$
I_{IL}	Input Load Current		±10	μA	$V_{IN} = V_{CC}$ to 0V
I_{OFL}	Output Float Leakage		±10	μA	$V_{OUT} = V_{CC}$ to 0V
I_{CC}	V_{CC} Supply Current		160	mA	

CAPACITANCE

$T_A = 25°C$; $V_{CC} = GND = 0V$

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance		10	pF	$f_c = 1$ MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to V_{SS}

A.C. CHARACTERISTICS

T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V

Bus Parameters (Note 1)

Read Cycle:

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{AR}	Address Stable Before READ	0		ns	
t_{RA}	Address Hold Time for READ	0		ns	
t_{RR}	READ Pulse Width	250		ns	
t_{RD}	Data Delay from READ		200	ns	C_L = 150 pF
t_{DF}	READ to Data Floating	20	100	ns	

Write Cycle:

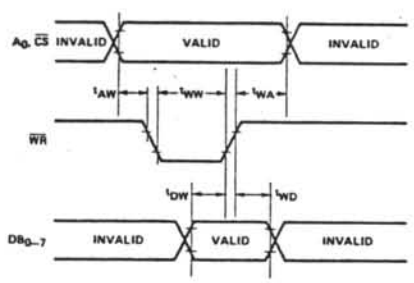
SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{AW}	Address Stable Before WRITE	0		ns	
t_{WA}	Address Hold Time for WRITE	0		ns	
t_{WW}	WRITE Pulse Width	250		ns	
t_{DW}	Data Setup Time for WRITE	150		ns	
t_{WD}	Data Hold Time for WRITE	0		ns	

Clock Timing:

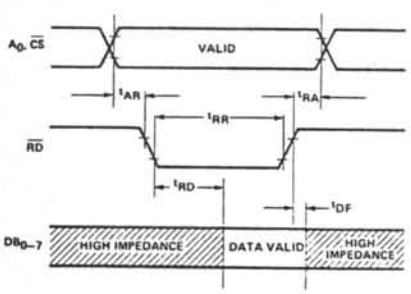
SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{CLK}	Clock Period	320		ns	
t_{KH}	Clock High	120		ns	
t_{KL}	Clock Low	120		ns	
t_{KR}	Clock Rise	5	30	ns	
t_{KF}	Clock Fall	5	30	ns	

Note 1: AC timings measured at V_{OH} = 2.0, V_{OL} = 0.8

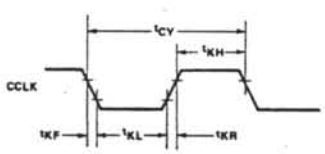
Write Timing



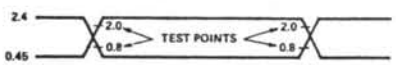
Read Timing



Clock Timing



Input Waveforms (For A.C. Tests)



Other Timing:

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{CC}	Character Code Output Delay		150	ns	C_L = 50 pF
t_{HR}	Horizontal Retrace Output Delay		150	ns	C_L = 50 pF
t_{LC}	Line Count Output Delay		250	ns	C_L = 50 pF
t_{AT}	Control/Attribute Output Delay		250	ns	C_L = 50 pF
t_{VR}	Vertical Retrace Output Delay		250	ns	C_L = 50 pF
t_{IR}	IRQ↑ from CCLK↓		250	ns	C_L = 50 pF
t_{RI}	IRQ↓ from Rd↑		250	ns	C_L = 50 pF
t_{KQ}	DRQ↑ from CCLK↓		250	ns	C_L = 50 pF
t_{WQ}	DRQ↑ from WR↑		250	ns	C_L = 50 pF
t_{RQ}	DRQ↓ from WR↓		250	ns	C_L = 50 pF
t_{LR}	DACK↓ to WR↓	0		ns	
t_{RL}	WR↑ to DACK↑	0		ns	
t_{PR}	LPEN Rise		50	ns	
t_{PH}	LPEN Hold	100		ns	

Note: Timing measurements are made at the following reference voltages: Output "1" = 2.0V, "0" = 0.8V.

WAVEFORMS

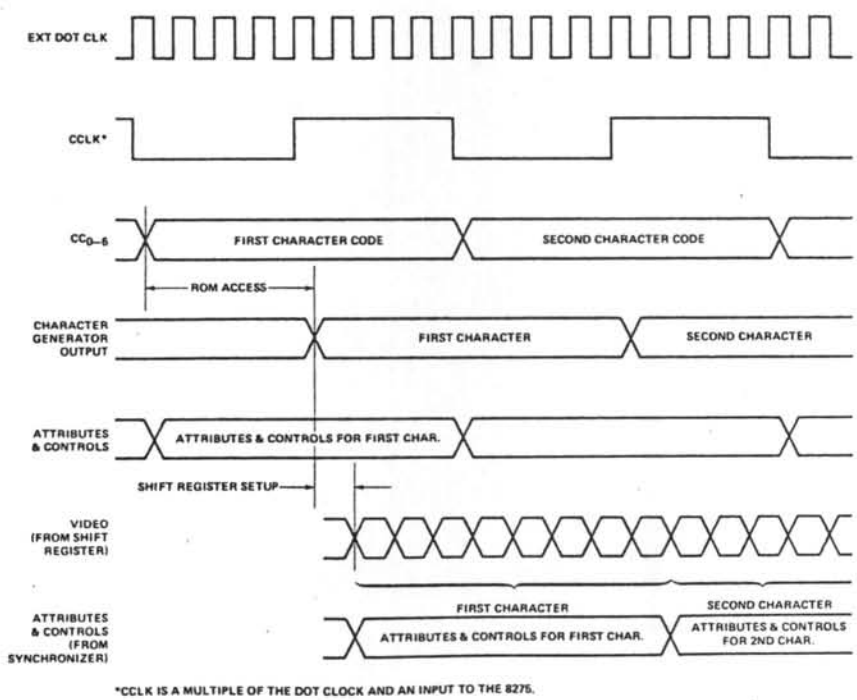


Figure 25. Typical Dot Level Timing

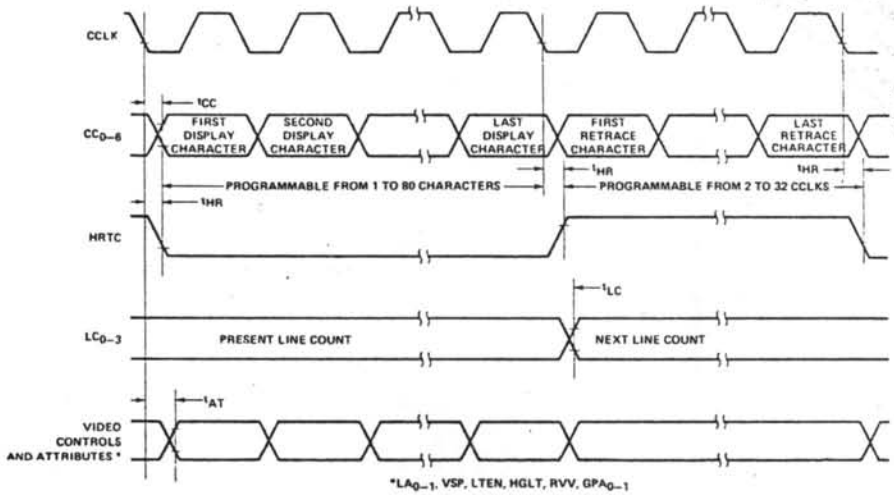


Figure 26. Line Timing

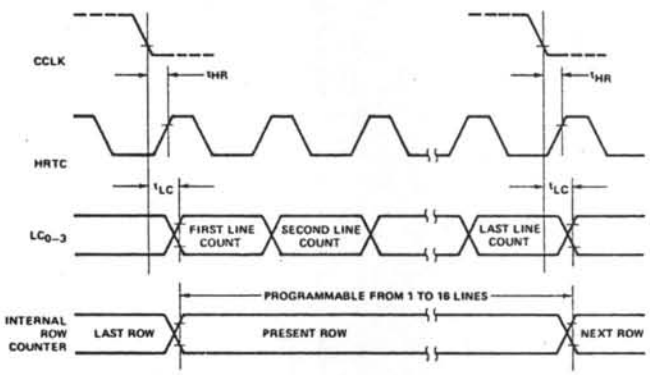


Figure 27. Row Timing

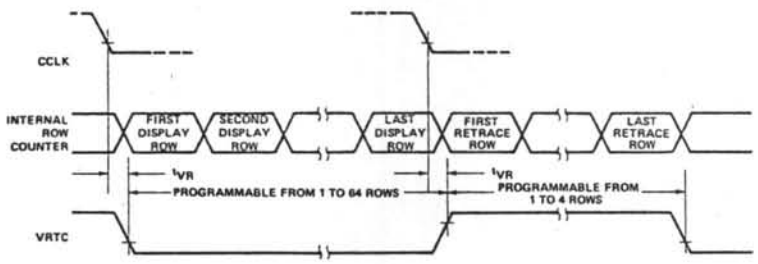


Figure 28. Frame Timing

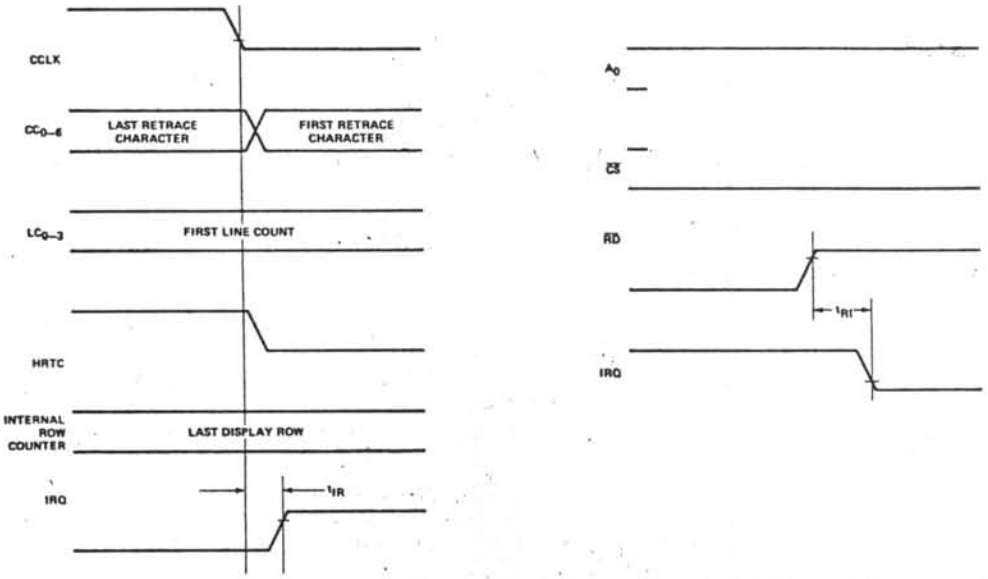


Figure 29. Interrupt Timing

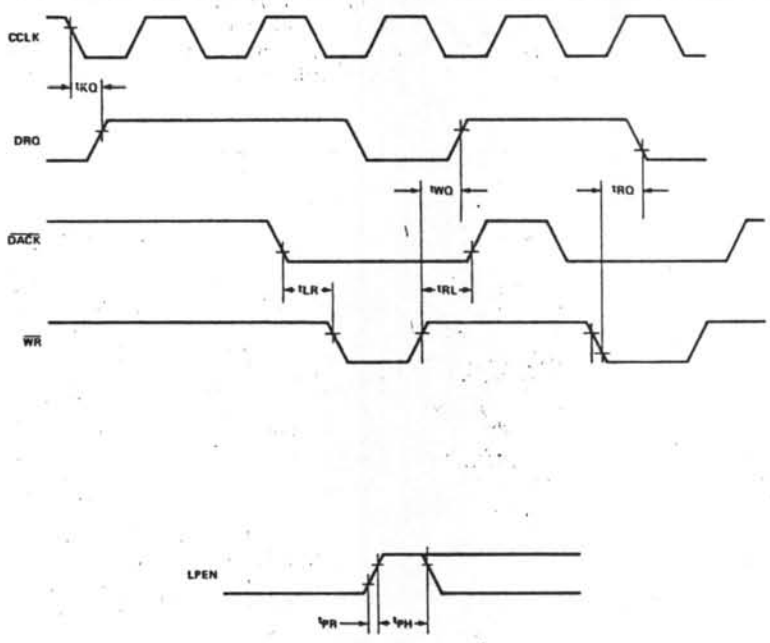


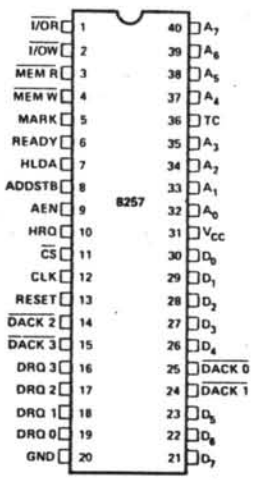
Figure 30. DMA Timing

8257/8257-5
PROGRAMMABLE DMA CONTROLLER

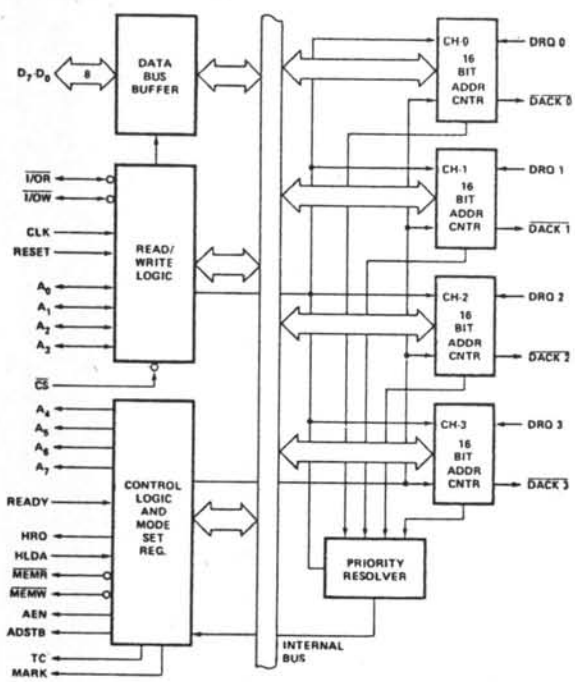
- MCS-85™ Compatible 8257-5
- 4-Channel DMA Controller
- Priority DMA Request Logic
- Channel Inhibit Logic
- Terminal Count and Modulo 128 Outputs
- Auto Load Mode
- Single TTL Clock
- Single +5V Supply
- Expandable
- 40-Pin Dual In-Line Package

The Intel® 8257 is a 4-channel direct memory access (DMA) controller. It is specifically designed to simplify the transfer of data at high speeds for the Intel® microcomputer systems. Its primary function is to generate, upon a peripheral request, a sequential memory address which will allow the peripheral to read or write data directly to or from memory. Acquisition of the system bus in accomplished via the CPU's hold function. The 8257 has priority logic that resolves the peripherals requests and issues a composite hold request to the CPU. It maintains the DMA cycle count for each channel and outputs a control signal to notify the peripheral that the programmed number of DMA cycles is complete. Other output control signals simplify sectored data transfers and expansion to other 8257 devices for systems that require more than 4 channels of DMA controlled transfer. The 8257 represents a significant savings in component count for DMA-based microcomputer systems and greatly simplifies the transfer of data at high speed between peripherals and memories.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

D_7-D_0	DATA BUS
A_7-A_0	ADDRESS BUS
$\overline{I/OR}$	I/O READ
$\overline{I/OW}$	I/O WRITE
$\overline{MEMR}$	MEMORY READ
$\overline{MEMW}$	MEMORY WRITE
CLK	CLOCK INPUT
RESET	RESET INPUT
READY	READY
HRQ	HOLD REQUEST (TO 8080A)
HLDA	HOLD ACKNOWLEDGE (FROM 8080A)

AEN	ADDRESS ENABLE
ADSTB	ADDRESS STROBE
TC	TERMINAL COUNT
MARK	MODULO 128 MARK
DRQ_3-DRQ_0	DMA REQUEST INPUT
$\overline{DACK_3}$-$\overline{DACK_0}$	DMA ACKNOWLEDGE OUT
$\overline{CS}$	CHIP SELECT
V_{CC}	+5 VOLTS
GND	GROUND

FUNCTIONAL DESCRIPTION

General

The 8257 is a programmable, Direct Memory Access (DMA) device which, when coupled with a single Intel® 8212 I/O port device, provides a complete four-channel DMA controller for use in Intel® microcomputer systems. After being initialized by software, the 8257 can transfer a block of data, containing up to 16,384 bytes, between memory and a peripheral device directly, without further intervention required of the CPU. Upon receiving a DMA transfer request from an enabled peripheral, the 8257:

- Acquires control of the system bus.
- Acknowledges that requesting peripheral which is connected to the highest priority channel.
- Outputs the least significant eight bits of the memory address onto system address lines A_0-A_7, outputs the most significant eight bits of the memory address to the 8212 I/O port via the data bus (the 8212 places these address bits on lines A_8-A_{15}), and
- Generates the appropriate memory and I/O read/write control signals that cause the peripheral to receive or deposit a data byte directly from or to the addressed location in memory.

The 8257 will retain control of the system bus and repeat the transfer sequence, as long as a peripheral maintains its DMA request. Thus, the 8257 can transfer a block of data to/from a high speed peripheral (e.g., a sector of data on a floppy disk) in a single "burst". When the specified number of data bytes have been transferred, the 8257 activates its Terminal Count (TC) output, informing the CPU that the operation is complete.

The 8257 offers three different modes of operation: (1) DMA read, which causes data to be transferred from memory to a peripheral; (2) DMA write, which causes data to be transferred from a peripheral to memory; and (3) DMA verify, which does not actually involve the transfer of data. When an 8257 channel is in the DMA verify mode, it will respond the same as described for transfer operations, except that no memory or I/O read/write control signals will be generated, thus preventing the transfer of data. The 8257, however, will gain control of the system bus and will acknowledge the peripheral's DMA request for each DMA cycle. The peripheral can use these acknowledge signals to enable an internal access of each byte of a data block in order to execute some verification procedure, such as the accumulation of a CRC (Cyclic Redundancy Code) checkword. For example, a block of DMA verify cycles might follow a block of DMA read cycles (memory to peripheral) to allow the peripheral to verify its newly acquired data.

Block Diagram Description

1. DMA Channels

The 8257 provides four separate DMA channels (labeled CH-0 to CH-3). Each channel includes two sixteen-bit registers: (1) a DMA address register, and (2) a terminal count register. Both registers must be initialized before a channel is enabled. The DMA address register is loaded with the address of the first memory location to be accessed. The value loaded into the low-order 14-bits of the terminal count register specifies the number of DMA cycles minus one before the Terminal Count (TC) output is activated. For instance, a terminal count of 0 would cause the TC output to be active in the first DMA cycle for that channel. In general, if N = the number of desired DMA cycles, load the value N-1 into the low-order 14-bits of the terminal count register. The most significant two bits of the terminal count register specify the type of DMA operation for that channel:

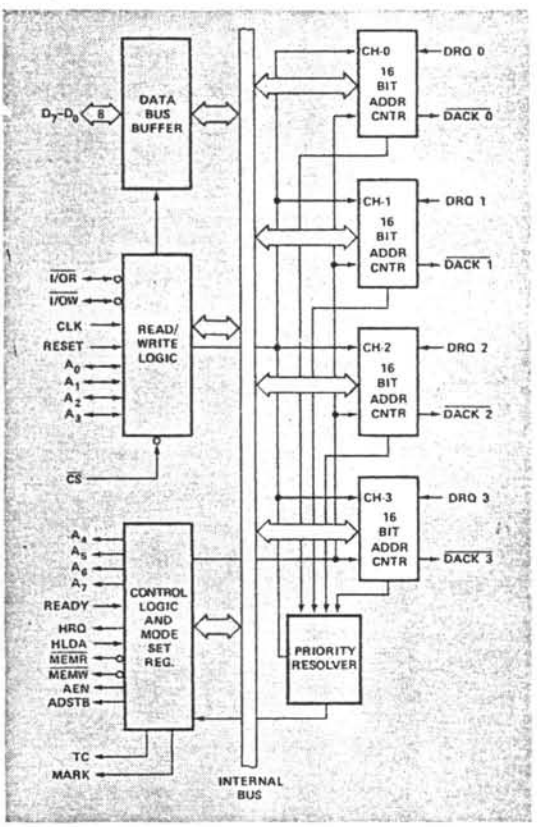


Figure 1. 8257 Block Diagram Showing DMA Channels

These two bits are not modified during a DMA cycle, but can be changed between DMA blocks.

Each channel accepts a DMA Request (DRQn) input and provides a DMA Acknowledge (DACKn) output:

BIT 15	BIT 14	TYPE OF DMA OPERATION
0	0	Verify DMA Cycle
0	1	Write DMA Cycle
1	0	Read DMA Cycle
1	1	(Illegal)

(DRQ 0-DRQ 3)

DMA Request: These are individual asynchronous channel request inputs used by the peripherals to obtain a DMA cycle. If not in the rotating priority mode then DRQ 0 has the highest priority and DRQ 3 has the lowest. A request can be generated by raising the request line and holding it high until DMA acknowledge. For multiple DMA cycles (Burst Mode) the request line is held high until the DMA acknowledge of the last cycle arrives.

$\overline{\text{(DACK 0 - DACK 3)}}$

DMA Acknowledge: An active low level on the acknowledge output informs the peripheral connected to that channel that it has been selected for a DMA cycle.

2. Data Bus Buffer

This three-state, bi-directional, eight bit buffer interfaces the 8257 to the system data bus:

(D_0-D_7)

Data Bus Lines: These are bi-directional three-state lines. When the 8257 is being programmed by the CPU, eight-bits of data for a DMA address register, a terminal count register or the Mode Set register are received on the data bus. When the CPU reads a DMA address register, a terminal count register or the Status register, the data is sent to the CPU over the data bus. During DMA cycles (when the 8257 is the bus master), the 8257 will output the most significant eight-bits of the memory address (from one of the DMA address registers) to the 8212 latch via the data bus. These address bits will be transferred at the beginning of the DMA cycle; the bus will then be released to handle the memory data transfer during the balance of the DMA cycle.

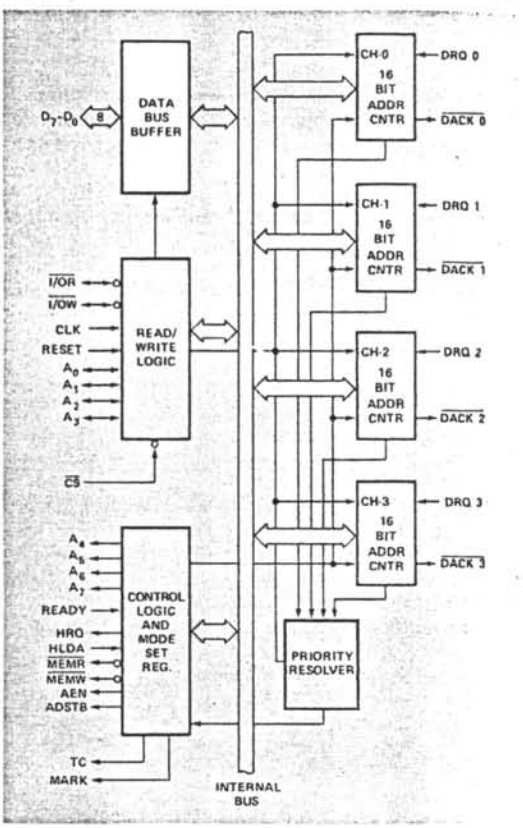


Figure 2. 8257 Block Diagram Showing Data Bus Buffer

3. Read/Write Logic

When the CPU is programming or reading one of the 8257's register (i.e., when the 8257 is a "slave" device on the system bus), the Read/Write Logic accepts the I/O Read ($\overline{I/OR}$) or I/O Write ($\overline{I/OW}$) signal, decodes the least significant four address bits, (A_0-A_3), and either writes the contents of the data bus into the addressed register (if $\overline{I/OW}$ is true) or places the contents of the addressed register onto the data bus (if $\overline{I/OR}$ is true).

During DMA cycles (i.e., when the 8257 is the bus "master"), the Read/Write Logic generates the I/O read and memory write (DMA write cycle) or I/O Write and memory read (DMA read cycle) signals which control the data link with the peripheral that has been granted the DMA cycle.

Note that during DMA transfers Non-DMA I/O devices should be de-selected (disabled) using "AEN" signal to inhibit I/O device decoding of the memory address as an erroneous device address.

($\overline{I/OR}$)

I/O Read: An active-low, bi-directional three-state line. In the "slave" mode, it is an input which allows the 8-bit status register or the upper/lower byte of a 16-bit DMA address register or terminal count register to be read. In the "master" mode, $\overline{I/OR}$ is a control output which is used to access data from a peripheral during the DMA write cycle.

($\overline{I/OW}$)

I/O Write: An active-low, bi-directional three-state line. In the "slave" mode, it is an input which allows the contents of the data bus to be loaded into the 8-bit mode set register or the upper/lower byte of a 16-bit DMA address register or terminal count register. In the "master" mode, $\overline{I/OW}$ is a control output which allows data to be output to a peripheral during a DMA read cycle.

(CLK)

Clock Input: Generally from an Intel® 8224 Clock Generator device. (ϕ2 TTL)

(RESET)

Reset: An asynchronous input (generally from an 8224 device) which clears all control lines and disables all DMA channels by clearing the mode register.

(A_0-A_3)

Address Lines: These least significant four address lines are bi-directional. In the "slave" mode they are inputs which select one of the registers to be read or programmed. In the "master" mode, they are outputs which constitute the least significant four bits of the 16-bit memory address generated by the 8257.

($\overline{CS}$)

Chip Select: An active-low input which enables the I/O Read or I/O Write input when the 8257 is being read or programmed in the "slave" mode. In the "master" mode, $\overline{CS}$ is automatically disabled to prevent the chip from selecting itself while performing the DMA function.

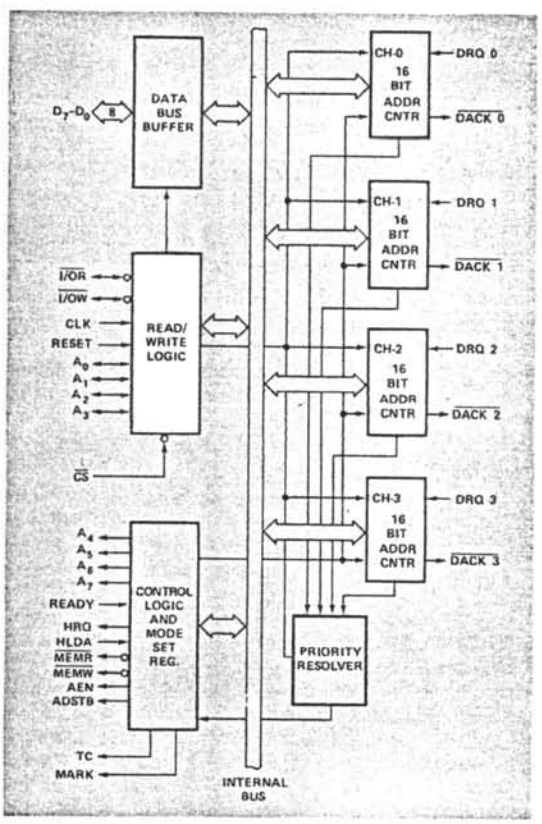


Figure 3. 8257 Block Diagram Showing Read/Write Logic Function

4. Control Logic

This block controls the sequence of operations during all DMA cycles by generating the appropriate control signals and the 16-bit address that specifies the memory location to be accessed.

(A_4-A_7)

Address Lines: These four address lines are three-state outputs which constitute bits 4 through 7 of the 16-bit memory address generated by the 8257 during all DMA cycles.

(READY)

Ready: This asynchronous input is used to elongate the memory read and write cycles in the 8257 with wait states if the selected memory requires longer cycles.

(HRQ)

Hold Request: This output requests control of the system bus. In systems with only one 8257, HRQ will normally be applied to the HOLD input on the CPU.

(HLDA)

Hold Acknowledge: This input from the CPU indicates that the 8257 has acquired control of the system bus.

($\overline{\text{MEMR}}$)

Memory Read: This active-low three-state output is used to read data from the addressed memory location during DMA Read cycles.

($\overline{\text{MEMW}}$)

Memory Write: This active-low three-state output is used to write data into the addressed memory location during DMA Write cycles.

(ADSTB)

Address Strobe: This output strobes the most significant byte of the memory address into the 8212 device from the data bus.

(AEN)

Address Enable: This output is used to disable (float) the System Data Bus and the System Control Bus. It may also be used to disable (float) the System Address Bus by use of an enable on the Address Bus drivers in systems to inhibit non-DMA devices from responding during DMA cycles. It may be further used to isolate the 8257 data bus from the System Data Bus to facilitate the transfer of the 8 most significant DMA address bits over the 8257 data I/O pins without subjecting the System Data Bus to any timing constraints for the transfer. When the 8257 is used in an I/O device structure (as opposed to memory mapped), this AEN output should be used to disable the selection of an I/O device when the DMA address is on the address bus. The I/O device selection should be determined by the DMA acknowledge outputs for the 4 channels.

(TC)

Terminal Count: This output notifies the currently selected peripheral that the present DMA cycle should be the last cycle for this data block. If the TC STOP bit in the Mode Set register is set, the selected channel will be automatically disabled at the end of that DMA cycle. TC is activated when the 14-bit value in the selected channel's terminal count register equals zero. Recall that the low-order 14-bits of the terminal count register should be loaded with the values (n-1), where n = the desired number of the DMA cycles.

(MARK)

Modulo 128 Mark: This output notifies the selected peripheral that the current DMA cycle is the 128th cycle since the previous MARK output. MARK always occurs at 128 (and all multiples of 128) cycles from the end of the data block. Only if the total number of DMA cycles (n) is evenly divisable by 128 (and the terminal count register was loaded with n-1), will MARK occur at 128 (and each succeeding multiple of 128) cycles from the beginning of the data block.

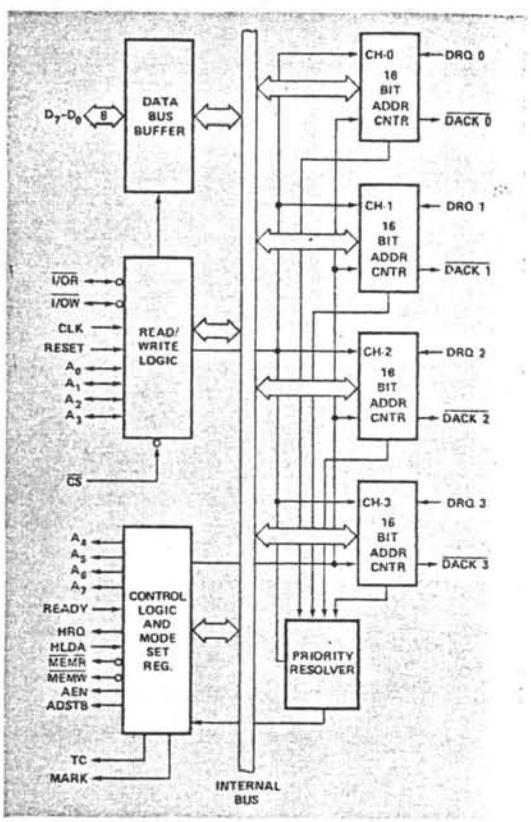
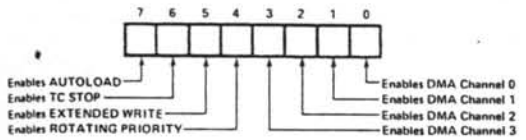


Figure 4. 8257 Block Diagram Showing Control Logic and Mode Set Register

5. Mode Set Register

When set, the various bits in the Mode Set register enable each of the four DMA channels, and allow four different options for the 8257:

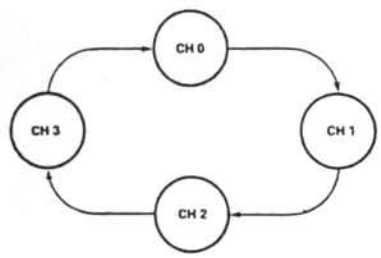


The Mode Set register is normally programmed by the CPU after the DMA address register(s) and terminal count register(s) are initialized. The Mode Set Register is cleared by the RESET input, thus disabling all options, inhibiting all channels, and preventing bus conflicts on power-up. A channel should not be left enabled unless its DMA address and terminal count registers contain valid values; otherwise, an inadvertent DMA request (DRQn) from a peripheral could initiate a DMA cycle that would destroy memory data.

The various options which can be enabled by bits in the Mode Set register are explained below:

Rotating Priority Bit 4

In the Rotating Priority Mode, the priority of the channels has a circular sequence. After each DMA cycle, the priority of each channel changes. The channel which had just been serviced will have the lowest priority.



If the ROTATING PRIORITY bit is not set (set to a zero), each DMA channel has a fixed priority. In the fixed priority mode, Channel 0 has the highest priority and Channel 3 has the lowest priority. If the ROTATING PRIORITY bit is set to a one, the priority of each channel changes after each DMA cycle (not each DMA request). Each channel moves up to the next highest priority assignment, while the channel which has just been serviced moves to the lowest priority assignment:

	CHANNEL→ JUST SERVICED	CH-0	CH-1	CH-2	CH-3
Priority → Assignments	Highest	CH-1	CH-2	CH-3	CH-0
	↑ ↓	CH-2	CH-3	CH-0	CH-1
		CH-3	CH-0	CH-1	CH-2
	Lowest	CH-0	CH-1	CH-2	CH-3

Note that rotating priority will prevent any one channel from monopolizing the DMA mode; consecutive DMA cycles will service different channels if more than one channel is enabled and requesting service. All DMA operations began with Channel 0 initially assigned to the highest priority for the first DMA cycle.

Extended Write Bit 5

If the EXTENDED WRITE bit is set, the duration of both the $\overline{\text{MEMW}}$ and $\overline{\text{I/OW}}$ signals is extended by activating them earlier in the DMA cycle. Data transfers within microcomputer systems proceed asynchronously to allow use of various types of memory and I/O devices with different access times. If a device cannot be accessed within a specific amount of time it returns a "not ready" indication to the 8257 that causes the 8257 to insert one or more wait states in its internal sequencing. Some devices are fast enough to be accessed without the use of wait states, but if they generate their READY response with the leading edge of the $\overline{\text{I/OW}}$ or $\overline{\text{MEMW}}$ signal (which generally occurs late in the transfer sequence), they would normally cause the 8257 to enter a wait state because it does not receive READY in time. For systems with these types of devices, the Extended Write option provides alternative timing for the I/O and memory write signals which allows the devices to return an early READY and prevents the unnecessary occurrence of wait states in the 8257, thus increasing system throughput.

TC Stop Bit 6

If the TC STOP bit is set, a channel is disabled (i.e., its enable bit is reset) after the Terminal Count (TC) output goes true, thus automatically preventing further DMA operation on that channel. The enable bit for that channel must be re-programmed to continue or begin another DMA operation. If the TC STOP bit is not set, the occurrence of the TC output has no effect on the channel enable bits. In this case, it is generally the responsibility of the peripheral to cease DMA requests in order to terminate a DMA operation.

Auto Load Bit 7

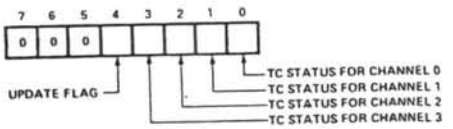
The Auto Load mode permits Channel 2 to be used for repeat block or block chaining operations, without immediate software intervention between blocks. Channel 2 registers are initialized as usual for the first data block; Channel 3 registers, however, are used to store the block re-initialization parameters (DMA starting address, terminal count and DMA transfer mode). After the first block of DMA cycles is executed by Channel 2 (i.e., after the TC output goes true), the parameters stored in the Channel 3 registers are transferred to Channel 2 during an "update" cycle. Note that the TC STOP feature, described above, has no effect on Channel 2 when the Auto Load bit is set.

If the Auto Load bit is set, the initial parameters for Channel 2 are automatically duplicated in the Channel 3 registers when Channel 2 is programmed. This permits repeat block operations to be set up with the programming of a single channel. Repeat block operations can be used in applications such as CRT refreshing. Channels 2 and 3 can still be loaded with separate values if Channel 2 is loaded before loading Channel 3. Note that in the Auto Load mode, Channel 3 is still available to the user if the Channel 3 enable bit is set, but use of this channel will change the values to be auto loaded into Channel 2 at update time. All that is necessary to use the Auto Load feature for chaining operations is to reload Channel 3 registers at the conclusion of each update cycle with the new parameters for the next data block transfer.

Each time that the 8257 enters an update cycle, the update flag in the status register is set and parameters in Channel 3 are transferred to Channel 2, non-destructively for Channel 3. The actual re-initialization of Channel 2 occurs at the beginning of the next channel 2 DMA cycle after the TC cycle. This will be the first DMA cycle of the new data block for Channel 2. The update flag is cleared at the conclusion of this DMA cycle. For chaining operations, the update flag in the status register can be monitored by the CPU to determine when the re-initialization process has been completed so that the next block parameters can be safely loaded into Channel 3.

6. Status Register

The eight-bit status register indicates which channels have reached a terminal count condition and includes the update flag described previously.



The TC status bits are set when the Terminal Count (TC) output is activated for that channel. These bits remain set until the status register is read or the 8257 is reset. The UPDATE FLAG, however, is not affected by a status register read operation. The UPDATE FLAG can be cleared by resetting the 8257, by changing to the non-auto load mode (i.e., by resetting the AUTO LOAD bit in the Mode Set register) or it can be left to clear itself at the completion of the update cycle. The purpose of the UPDATE FLAG is to prevent the CPU from inadvertently skipping a data block by overwriting a starting address or terminal count in the Channel 3 registers before those parameters are properly auto-loaded into Channel 2.

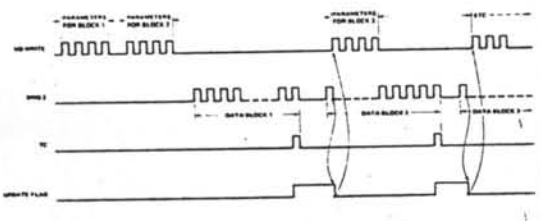


Figure 5. Autoload Timing

8257 Register Selection

REGISTER	BYTE	ADDRESS INPUTS					BI-DIRECTIONAL DATA BUS							
		A_3	A_2	A_1	A_0	F/L	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
CH-0 DMA Address	LSB	0	0	0	0	0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
	MSB	0	0	0	0	1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8
CH-0 Terminal Count	LSB	0	0	0	1	0	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0
	MSB	0	0	0	1	1	R/$\overline{W}$	C_{14}	C_{13}	C_{12}	C_{11}	C_{10}	C_9	C_8
CH-1 DMA Address	LSB	0	0	1	0	0	Same as Channel 0							
	MSB	0	0	1	0	1								
CH-1 Terminal Count	LSB	0	0	1	1	0								
	MSB	0	0	1	1	1								
CH-2 DMA Address	LSB	0	1	0	0	0	Same as Channel 0							
	MSB	0	1	0	0	1								
CH-2 Terminal Count	LSB	0	1	0	1	0								
	MSB	0	1	0	1	1								
CH-3 DMA Address	LSB	0	1	1	0	0	Same as Channel 0							
	MSB	0	1	1	0	1								
CH-3 Terminal Count	LSB	0	1	1	1	0								
	MSB	0	1	1	1	1								
MODE SET (Program only)	—	1	0	0	0	0	AL	TCS	EW	RP	EN3	EN2	EN1	EN0
STATUS (Read only)	—	1	0	0	0	0	0	0	0	UP	TC3	TC2	TC1	TC0

*A_0-A_{15}: DMA Starting Address; C_0-C_{15}: Terminal Count value (R/$\overline{W}$: Read and Write; DMA Verify (00); Write (01) or Read (10) cycle selection; AL: Auto-Load; TCS: TC STOP; EW: EXTENDED WRITE; RP: ROTATING PRIORITY; EN3-EN0: CHANNEL ENABLE MASK; UP: UPDATE FLAG; TC3-TC0: TERMINAL COUNT STATUS BITS

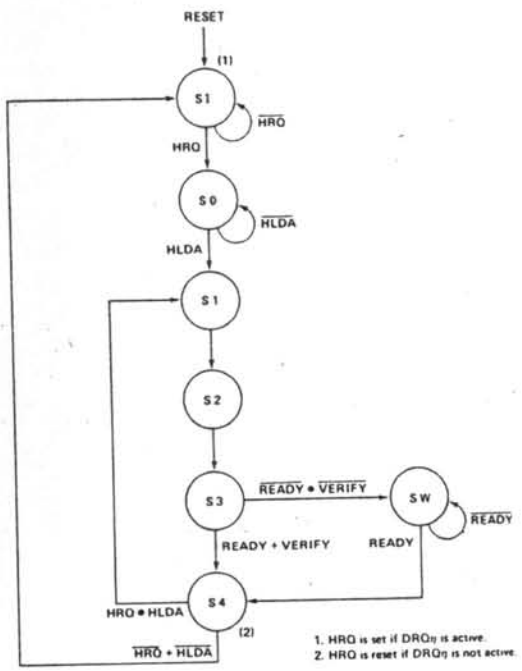


Figure 6. DMA Operation State Diagram

Programming and Reading the 8257 Registers

There are four pairs of "channel registers": each pair consisting of a 16-bit DMA address register and a 16-bit terminal count register (one pair for each channel). The 8257 also includes two "general registers": one 8-bit Mode Set register and one 8-bit Status register. The registers are loaded or read when the CPU executes a write or read instruction that addresses the 8257 device and the appropriate register within the 8257. The 8228 generates the appropriate read or write control signal (generally I/OR or I/OW while the CPU places a 16-bit address on the system address bus, and either outputs the data to be written onto the system data bus or accepts the data being read from the data bus. All or some of the most significant 12 address bits A_4-A_{15} (depending on the systems memory, I/O configuration) are usually decoded to produce the chip select ($\overline{CS}$) input to the 8257. An I/O Write input (or Memory Write in memory mapped I/O configurations, described below) specifies that the addressed register is to be programmed, while an I/O Read input (or Memory Read) specifies that the addressed register is to be read. Address bit 3 specifies whether a "channel register" (A_3 = 0) or the Mode Set (program only)/Status (read only) register (A_3 = 1) is to be accessed.

The least significant three address bits, A_0-A_2, indicate the specific register to be accessed. When accessing the Mode Set or Status register, A_0-A_2 are all zero. When accessing a channel register bit A_0 differentiates between the DMA address register (A_0 = 0) and the terminal count register (A_0 = 1), while bits A_1 and A_2 specify one of the

CONTROL INPUT	$\overline{CS}$	$\overline{I/OW}$	$\overline{I/OR}$	A_3
Program Half of a Channel Register	0	0	1	0
Read Half of a Channel Register	0	1	0	0
Program Mode Set Register	0	0	1	1
Read Status Register	0	1	0	1

four channels. Because the "channel registers" are 16-bits, two program instruction cycles are required to load or read an entire register. The 8257 contains a first/last (F/L) flip flop which toggles at the completion of each channel program or read operation. The F/L flip flop determines whether the upper or lower byte of the register is to be accessed. The F/L flip flop is reset by the RESET input and whenever the Mode Set register is loaded. To maintain proper synchronization when accessing the channel registers" all channel command instruction operations should occur in pairs, with the lower byte of a register always being accessed first. Do not allow $\overline{CS}$ to clock while either $\overline{I/OR}$ or $\overline{I/OW}$ is active, as this will cause an erroneous F/L flip flop state. In systems utilizing an interrupt structure, interrupts should be disabled prior to any paired programming operations to prevent an interrupt from splitting them. The result of such a split would leave the F/L F/F in the wrong state. This problem is particularly obvious when other DMA channels are programmed by an interrupt structure.

DMA Operation

Internal 8257 operations may proceed through seven different states. The duration of a state is defined by the clock input. When the 8257 is not executing a DMA cycle, it is in the idle state, S_I. A DMA cycle begins when one or more DMA Request (DRQn) lines become active. The 8257 then enters state S_0, sends a Hold Request (HRQ) to the CPU and waits for as many S_0 states as are necessary for the CPU to return a Hold Acknowledge (HLDA). For each S_0 state, the DMA Request lines are again sampled and DMA priority is resolved (according to the fixed or rotating priority scheme). When HLDA is received, the DMA Acknowledge ($\overline{DACKn}$) line for the highest priority requesting channel is activated, thus selecting that channel and its peripheral for the DMA cycle. The 8257 then proceeds to state S_1. Note that the DMA Request (DRQn) input should remain high until either $\overline{DACKn}$ is received for a single DMA cycle service, or until both the $\overline{DACKn}$ and TC outputs are received when transferring an entire data block in a "burst" mode. If the 8257 should lose control of the system bus (i.e., if HLDA goes false), the DMA Acknowledge will be removed after the current DMA cycle is completed and no more DMA cycles will occur until the 8257 again acquires control of the system bus.

Each DMA cycle will consist of at least four internal states: S_1, S_2, S_3, and S_4. If the access time for the memory or I/O devices involved is not fast enough to return the required READY response and complete a byte transfer within the specified amount of time, one or more wait states (SW) are inserted between states S_3 and S_4. Recall that in certain cases the Extended Write option can eliminate the need for a wait state. Note that a READY response is not required during DMA verify cycles. Specified minimum/maximum values for READY setup time (t_{RS}), write data setup time (t_{DW}), read data access time (t_{RD}) and HLDA setup time (t_{QS}) are listed under A.C. CHARACTERISTICS and are illustrated in the accompanying timing diagrams.

During DMA write cycles, the I/O Read ($\overline{I/OR}$) output is generated at the beginning of state S_2 and the Memory Write ($\overline{MEMW}$) output is generated at the beginning of S_3. During DMA read cycles, the Memory Read ($\overline{MEMR}$) output is generated at the beginning of state S_2 and the I/O Write (I/OW) output goes true at the beginning of of state S_3. Recall that no read or write control signals are generated during DMA verify cycles. Extended $\overline{WR}$ for MEM and I/O will be generated in S_2.

Memory Mapped I/O Configurations

The 8257 can be connected to the system bus as a memory device instead of as an I/O device for memory mapped I/O configurations by connecting the system memory control lines to the 8257's I/O control lines and the system I/O control lines to the 8257's memory control lines.

This configuration permits use of the 8080's considerably larger repertoire of memory instructions when reading or loading the 8257's registers. Note that with this connection, the programming of the Read (bit 15) and Write (bit 14) bits in the terminal count register will have a different meaning:

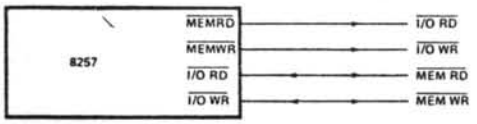


Figure 7. System Interface for Memory Mapped I/O

BIT 15 READ	BIT 14 WRITE	
0	0	DMA Verify Cycle
0	1	DMA Read Cycle
1	0	DMA Write Cycle
1	1	Illegal

Figure 8. TC Register for Memory Mapped I/O Only

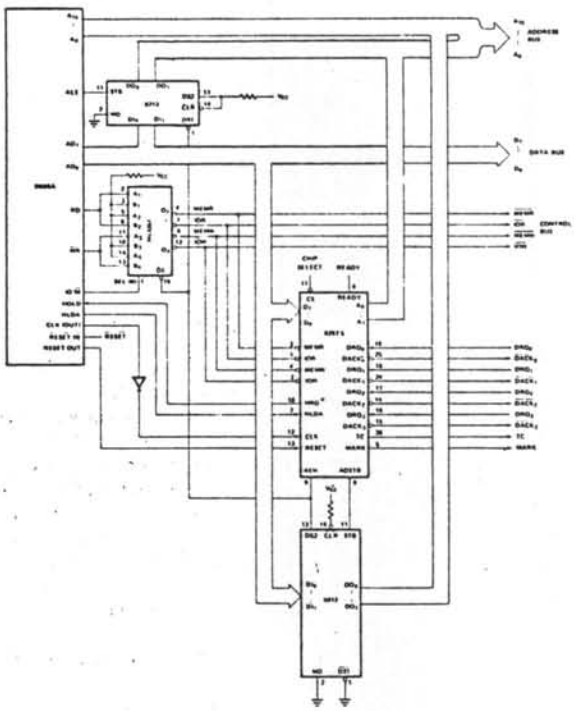


Figure 9. Detailed System Interface Schematic

SYSTEM APPLICATION EXAMPLES

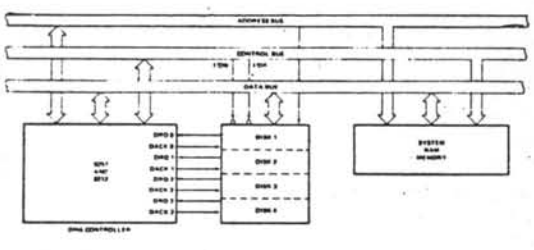


Figure 10. Floppy Disk Controller (4 Drives)

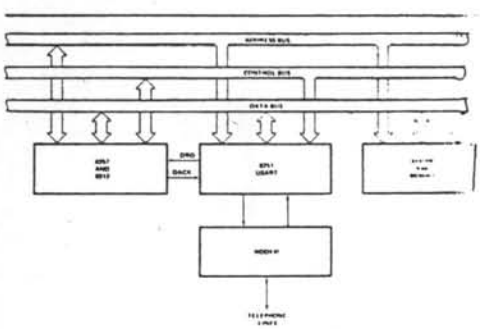


Figure 11. High-Speed Communication Controller

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . .–65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 1 Watt

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, GND = 0V

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	-0.5	0.8	Volts	
V_{IH}	Input High Voltage	2.0	V_{CC}+.5	Volts	
V_{OL}	Output Low Voltage		0.45	Volts	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4	V_{CC}	Volts	I_{OH}=-150μA for AB, DB and AEN I_{OH}=-80μA for others
V_{HH}	HRQ Output High Voltage	3.3	V_{CC}	Volts	I_{OH} = -80μA
I_{CC}	V_{CC} Current Drain		120	mA	
I_{IL}	Input Leakage		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Leakage During Float		±10	μA	V_{OUT} = V_{CC} to 0V

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

A.C. CHARACTERISTICS: PRIPHERAL (SLAVE) MODE

T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%; GND = 0V (Note 1).

8080 Bus Parameters

Read Cycle:

Symbol	Parameter	8257 Min.	8257 Max.	8257-5 Min.	8257-5 Max.	Unit	Test Conditions
T_{AR}	Adr or $\overline{CS}\downarrow$ Setup to $\overline{RD}\downarrow$	0		0		ns	
T_{RA}	Adr or $\overline{CS}\uparrow$ Hold from $\overline{RD}\uparrow$	0		0		ns	
T_{RD}	Data Access from $\overline{RD}\downarrow$	0	300	0	200	ns	(Note 2)
T_{DF}	DB→Float Delay from $\overline{RD}\uparrow$	20	150	20	100	ns	
T_{RR}	$\overline{RD}$ Width	250		250		ns	

Write Cycle:

Symbol	Parameter	8257 Min.	8257 Max.	8257-5 Min.	8257-5 Max.	Unit	Test Conditions
T_{AW}	Adr Setup to $\overline{WR}\downarrow$	20		20		ns	
T_{WA}	Adr Hold from $\overline{WR}\uparrow$	0		0		ns	
T_{DW}	Data Setup to $\overline{WR}\uparrow$	200		200		ns	
T_{WD}	Data Hold from $\overline{WR}\uparrow$	0		0		ns	
T_{WW}	$\overline{WR}$ Width	200		200		ns	

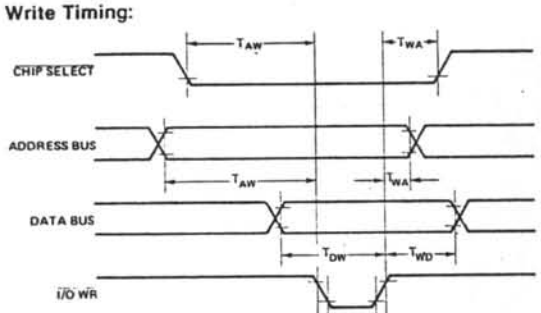
Other Timing:

Symbol	Parameter	8257 Min.	8257 Max.	8257-5 Min.	8257-5 Max.	Unit	Test Conditions
T_{RSTW}	Reset Pulse Width	300		300		ns	
T_{RSTD}	Power Supply↑ (V_{CC}) Setup to Reset↓	500		500		μs	
T_r	Signal Rise Time		20		20	ns	
T_f	Signal Fall Time		20		20	ns	
T_{RSTS}	Reset to First $\overline{IOWR}$	2		2		t_{CY}	

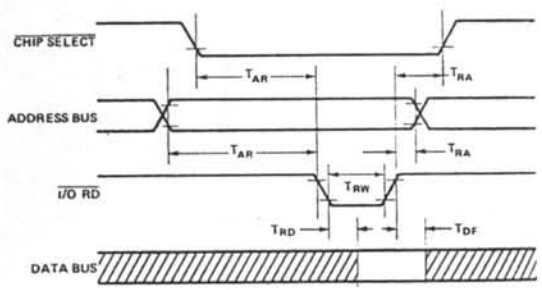
Notes: 1. All timing measurements are made at the following reference voltages unless specified otherwise: Input "1" at 2.0V, "0" at 0.8V
Output "1" at 2.0V, "0" at 0.8V
2. 8257: C_L = 100pF, 8257-5: C_L = 150pF.

8257 PERIPHERAL MODE TIMING DIAGRAMS

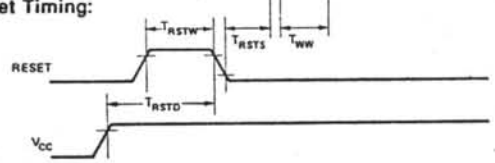
Write Timing:



Read Timing:



Reset Timing:



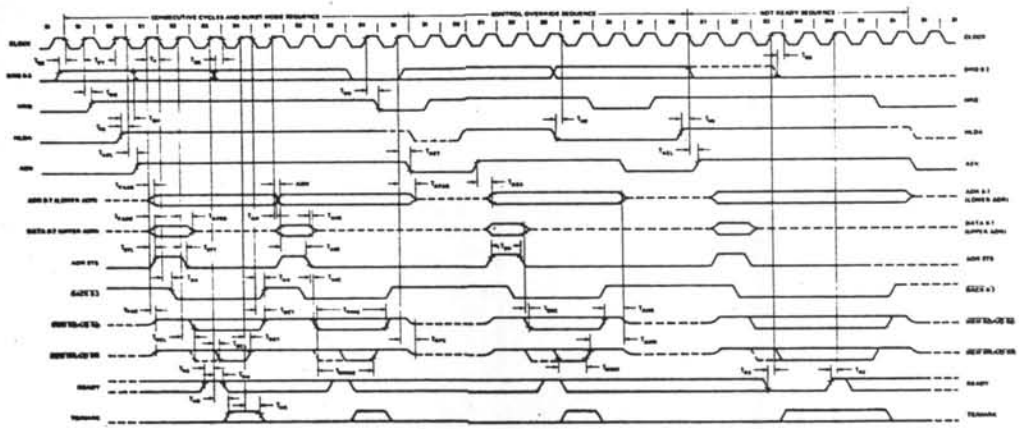
Input Waveform for A.C. Tests:

A.C. CHARACTERISTICS: DMA (MASTER) MODE $T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 5\%$, GND = 0V

SYMBOL	PARAMETER	8257		8257-5		UNIT
		MIN.	MAX.	MIN.	MAX.	
T_{CY}	Cycle Time (Period)	0.320	4	320	4	μs
$T\theta$	Clock Active (High)	120	$.8T_{CY}$	80	$.8T_{CY}$	ns
T_{QS}	DRQ↑ Setup to θ↓(SI,S4)	120		120		
T_{QH}	DRQ↓ Hold from HLDA↑[4]	0		0		
T_{DQ}	HRQ↑ or ↓Delay from θ↑(SI,S4) (measured at 2.0V)[1]		160		160	ns
T_{DQ1}	HRQ↑ or ↓Delay from θ↑(SI,S4) (measured at 3.3V)[3]		250		250	ns
T_{HS}	HLDA↑ or ↓Setup to θ↓(SI,S4)	100		100		ns
T_{AEL}	AEN↑ Delay from θ↓(S1)[1]		300		300	ns
T_{AET}	AEN↓ Delay from θ↑(SI)[1]		200		200	ns
T_{AEA}	Adr(AB)(Active) Delay from AEN↑(S1)[4]	20		20		ns
T_{FAAB}	Adr(AB)(Active) Delay from θ↑(S1)[2]		250		250	ns
T_{AFAB}	Adr(AB)(Float) Delay from θ↑(SI)[2]		150		150	ns
T_{ASM}	Adr(AB)(Stable) Delay from θ↑(S1)[2]		250		250	ns
T_{AH}	Adr(AB)(Stable) Hold from θ↑(S1)[2]	$T_{ASM}-50$		$T_{ASM}-50$		
T_{AHR}	Adr(AB)(Valid) Hold from $\overline{Rd}$↑(S1,SI)[4]	60		60		ns
T_{AHW}	Adr(AB)(Valid) Hold from $\overline{Wr}$↑(S1,SI)[4]	300		300		ns
T_{FADB}	Adr(DB)(Active) Delay from θ↑(S1)[2]		300		300	ns
T_{AFDB}	Adr(DB)(Float) Delay from θ↑(S2)[2]	$T_{STT}+20$	250	$T_{STT}+20$	170	ns
T_{ASS}	Adr(DB) Setup to AdrStb↓(S1-S2)[4]	100		100		ns
T_{AHS}	Adr(DB)(Valid) Hold from AdrStb↓(S2)[4]	50		50		ns
T_{STL}	AdrStb↑ Delay from θ↑(S1)[1]		200		200	ns
T_{STT}	AdrStb↓ Delay from θ↑(S2)[1]		140		140	ns
T_{SW}	AdrStb Width (S1-S2)[4]	$T_{CY}-100$		$T_{CY}-100$		ns
T_{ASC}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from AdrStb↓(S2)[4]	70		70		ns
T_{DBC}	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from Adr(DB) (Float)(S2)[4]	20		20		ns
T_{AK}	DACK↑ or ↓Delay from θ↓(S2,S1) and TC/Mark↑ Delay from θ↑(S3) and TC/Mark↓ Delay from θ↑(S4)[1,5]		250		250	ns
T_{DCL}*	$\overline{Rd}$↓ or $\overline{Wr}$(Ext)↓ Delay from θ↑(S2) and $\overline{Wr}$↓ Delay from θ↑(S3)[2,6]		200		200	ns
T_{DCT}	$\overline{Rd}$↑ Delay from θ↓(S1,SI) and $\overline{Wr}$↑ Delay from θ↑(S4)[2,7]		200		200	ns
T_{FAC}	$\overline{Rd}$ or $\overline{Wr}$ (Active) from θ↑(S1)[2]		300		300	ns
T_{AFC}	$\overline{Rd}$ or $\overline{Wr}$ (Float) from θ↑(SI)[2]		150		150	ns
T_{RWM}	$\overline{Rd}$ Width (S2-S1 or SI)[4]	$2T_{CY}+T_\theta-50$		$2T_{CY}+T_\theta-50$		ns
T_{WWM}	$\overline{Wr}$ Width (S3-S4)[4]	$T_{CY}-50$		$T_{CY}-50$		ns
T_{WWME}	$\overline{Wr}$(Ext) Width (S2-S4)[4]	$2T_{CY}-50$		$2T_{CY}-50$		ns
T_{RS}	READY Set Up Time to θ↑ (S3, Sw)	30		30		ns
T_{RH}	READY Hold Time from θ↑ (S3, Sw)	20		20		ns

Notes: 1. Load = 1 TTL. 2. Load = 1 TTL + 50pF. 3. Load = 1 TTL + (R_L = 3.3K), V_{OH} = 3.3V. 4. Tracking Specification. 5. $\Delta T_{AK} < 50$ ns. 6. $\Delta T_{DCL} < 50$ ns. 7. $\Delta T_{DCT} < 50$ ns.

DMA MODE WAVEFORMS



8212/3212*
8-BIT INPUT/OUTPUT PORT

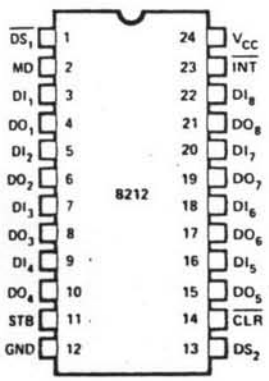
- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current — 0.25 mA Max
- 3-State Outputs
- Outputs Sink 15 mA
- 3.65V Output High Voltage for Direct Interface to 8080 CPU or 8008 CPU
- Asynchronous Register Clear
- Replaces Buffers, Latches, and Multiplexers in Microcomputer Systems
- Reduces System Package Count

The Intel® 8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

The device is multimode in nature. It can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

*Note: The specifications for the 3212 are identical with those for the 8212.

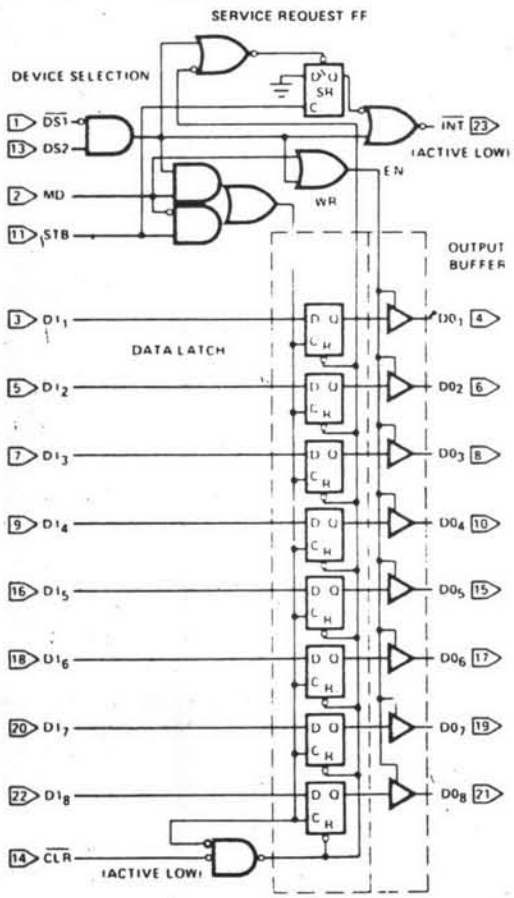
PIN CONFIGURATION



PIN NAMES

DI_1-DI_8	DATA IN
DO_1-DO_8	DATA OUT
$\overline{DS_1}$-DS_2	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

Data Latch

The 8 flip-flops that make up the data latch are of a "D" type design. The output (Q) of the flip-flop will follow the data input (D) while the clock input (C) is high. Latching will occur when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$). (Note: Clock (C) Overides Reset ($\overline{CLR}$).)

Output Buffer

The outputs of the data latch (Q) are connected to 3-state, non-inverting output buffers. These buffers have a common control line (EN); this control line either enables the buffer to transmit the data from the outputs of the data latch (Q) or disables the buffer, forcing the output into a high impedance state. (3-state)

This high-impedance state allows the designer to connect the 8212 directly onto the microprocessor bi-directional data bus.

Control Logic

The 8212 has control inputs $\overline{DS1}$, DS2, MD and STB. These inputs are used to control device selection, data latching, output buffer state and service request flip-flop.

DS1, DS2 (Device Select)

These 2 inputs are used for device selection. When $\overline{DS1}$ is low and DS2 is high ($\overline{DS1} \cdot DS2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

MD (Mode)

This input is used to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is high (output mode) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS1} \cdot DS2$).

When MD is low (input mode) the output buffer state is determined by the device selection logic ($\overline{DS1} \cdot DS2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

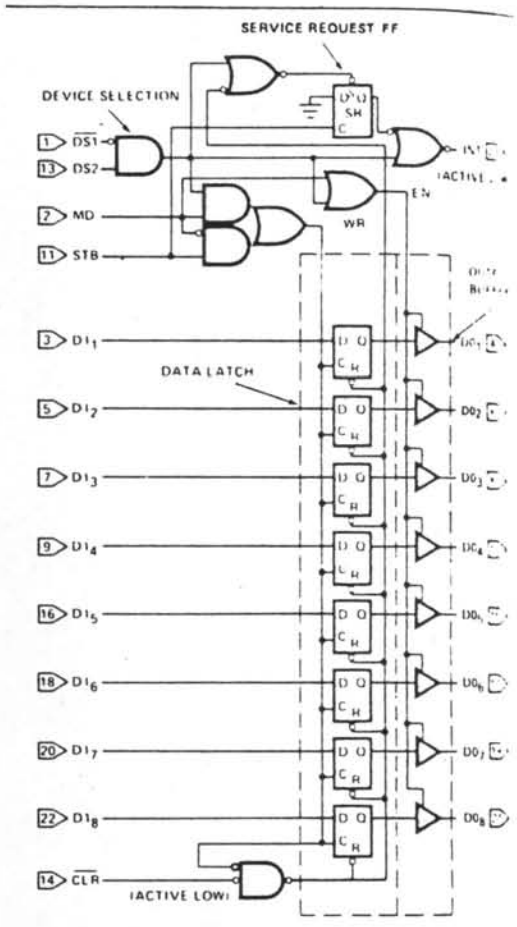
This input is used as the clock (C) to the data latch for the input mode (MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop is negative edge triggered.

Service Reqeust Flip-Flop

The (SR) flip-flop is used to generate and co... interrupts in microcomputer systems. It is as... chronously set by the $\overline{CLR}$ input (active low). W... the (SR) flip-flop is set it is in the non-interru... state.

The output of the (SR) flip-flop (Q) is connecte... an inverting input of a "NOR" gate. The other i... to the "NOR" gate is non-inverting and is conne... to the device selection logic ($\overline{DS1} \cdot DS2$). The ou... of the "NOR" gate ($\overline{INT}$) is active low (interru... state) for connection to active low input pric... generating circuits.



STB	MD	($DS_1 \cdot DS_2$)	DATA OUT EQUALS
0	0	0	3 STATE
1	0	0	3 STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

CLR	($\overline{DS_1} \cdot DS_2$)	STB	*SR
0	0	0	1
0	1	0	1
1	1	↓	0
1	1	0	1
1	0	0	1
1	1	↑	1

*INTERNAL SR FLIP FLOP

$\overline{CLR}$ – RESETS DATA LATCH
SETS SR FLIP FLOP
(NO EFFECT ON OUTPUT BUFFER)

Figure 1. Service Flip-Flop Function

APPLICATIONS OF THE 8212 — FOR MICROCOMPUTER SYSTEMS

- Basic schematic symbols
- Gated buffer
- Bidirectional bus driver
- Interrupting input port
- Interrupt instruction port
- Output port
- 8080A status latch
- 8085A address latch

Basic Schematic Symbols

Two examples of ways to draw the 8212 on system schematics—(1) the top being the detailed view showing pin numbers, and (2) the bottom being the symbolic view showing the system input or output as a system bus (bus containing 8 parallel lines). The output to the data bus is symbolic in referencing 8 parallel lines.

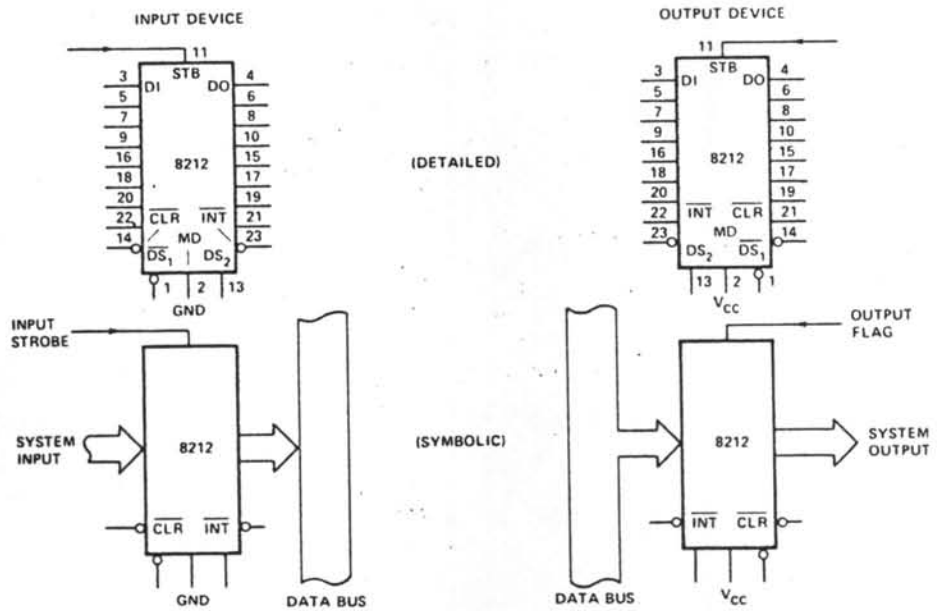


Figure 2. Basic Schematic Symbols

Gated Buffer (3-State)

The simplest use of the 8212 is that of a gated buffer. By tying the mode signal low and the strobe input high, the data latch is acting as a straight through gate. The output buffers are then enabled from the device selection logic $\overline{DS1}$ and DS2.

When the device selection logic is false, the outputs are 3-state.

When the device selection logic is true, the input data from the system is directly transferred to the output. The input data load is 250 micro amps. The output data can sink 15 milli amps. The minimum high output is 3.65 volts.

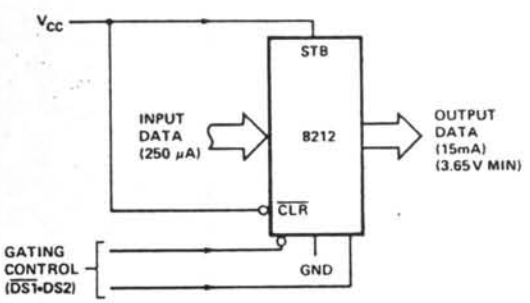


Figure 3. Gated Buffer (3-State)

Bidirectional Bus Driver

A pair of 8212's wired (back-to-back) can be used as a symmetrical drive, bi-directional bus driver. The devices are controlled by the data bus input control which is connected to $\overline{DS1}$ on the first 8212 and to DS2 on the second. One device is active, and acting as a straight through buffer the other is in 3-state mode. This is a very useful circuit in small system design.

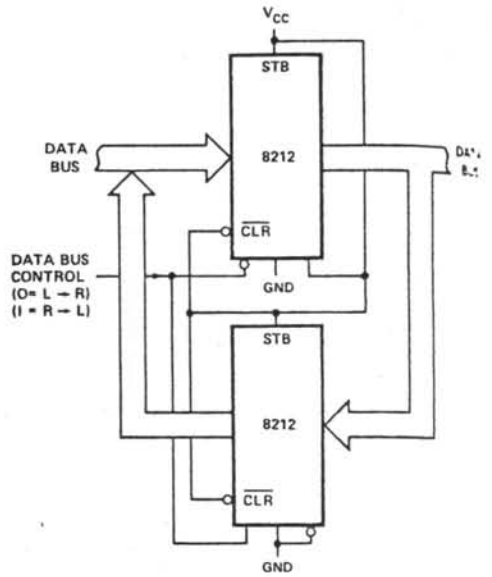


Figure 4. Bidirectional Bus Driver

Interrupting Input Port

This use of an 8212 is that of a system input port that accepts a strobe from the system input source, which in turn clears the service request flip-flop and interrupts the processor. The processor then goes through a service routine, identifies the port, and causes the device selection logic to go true — enabling the system input data onto the data bus.

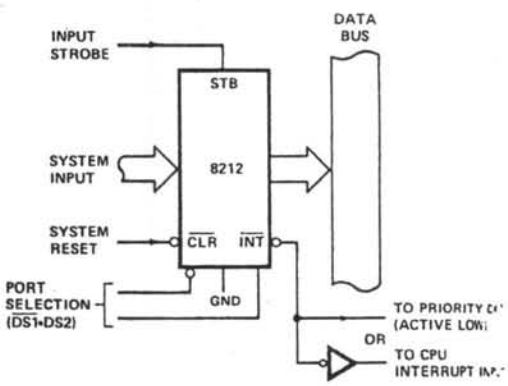


Figure 5. Interrupting Input Port

Interrupt Instruction Port

The 8212 can be used to gate the interrupt instruction, normally RESTART instructions, onto the data bus. The device is enabled from the interrupt acknowledge signal from the microprocessor and from a port selection signal. This signal is normally tied to ground. ($\overline{DS1}$ could be used to multiplex a variety of interrupt instruction ports onto a common bus).

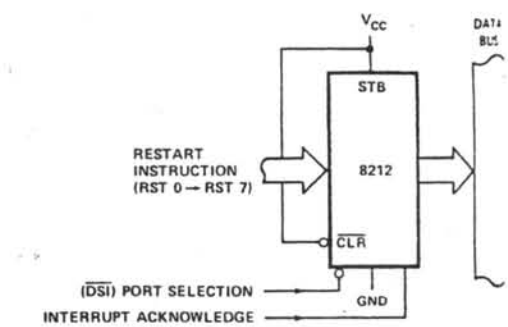


Figure 6. Interrupt Instruction Port

Output Port (With Handshaking)

The 8212 can be used to transmit data from the data bus to a system output. The output strobe could be a hand-shaking signal such as "reception of data" from the device that the system is outputting to. It in turn, can interrupt the system signifying the reception of data. The selection of the port comes from the device selection logic. ($\overline{DS1} \cdot DS2$)

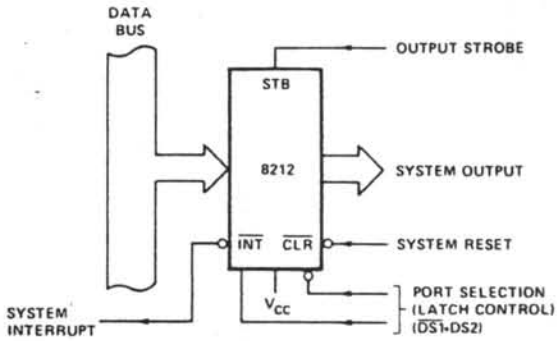


Figure 8. 8080 Status Latch

8080 Status Latch

Here the 8212 is used as the status latch for an 8080 microcomputer system. The input to the 8212 latch is directly from the 8080 data bus. Timing shows that when the SYNC signal is true, which is connected to the DS2 input and the phase 1 signal is true, which is a TTL level coming from the clock generator; then, the status data will be latched into the 8212.

Note: The mode signal is tied high so that the output on the latch is active and enabled all the time.

It is shown that the two areas of concern are the bidirectional data bus of the microprocessor and the control bus.

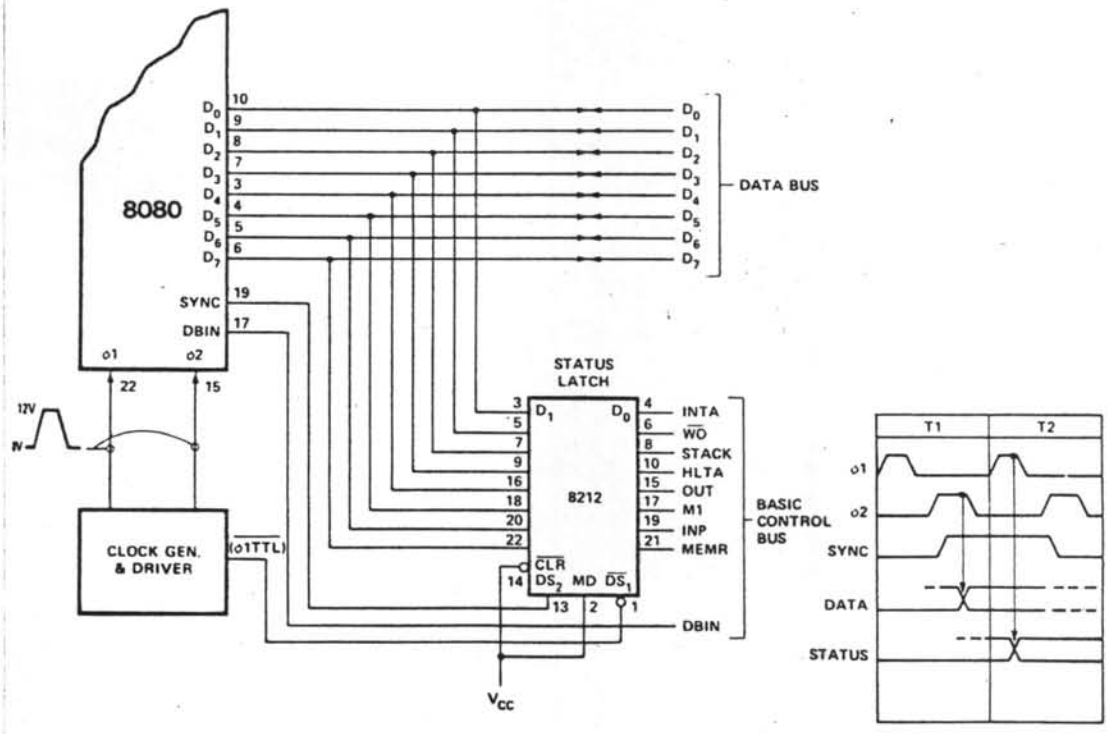


Figure 7. Output Port (With Handshaking)

ABSOLUTE MAXIMUM RATINGS*

Temperature under bias plastic.....0°C to 75°C
Storage temperature .....0°C to 75°C
All output or supply voltages.....−0.5V to +7V
All input voltages.....−1.0V to +5.5V
Output currents.....100 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

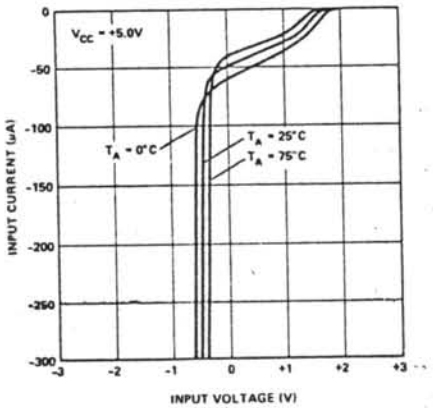
D.C. CHARACTERISTICS

T_A = 0°C to +75°C V_{CC} = +5V ±5%

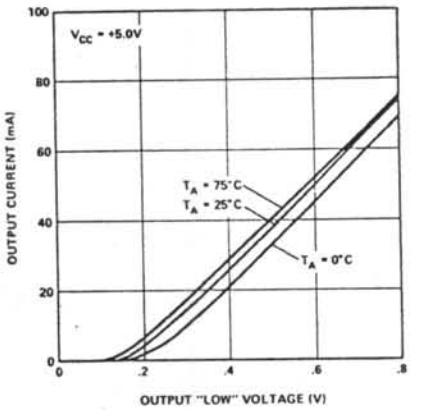
Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
I_F	Input Load Current ACK, DS_2, CR, DI_1-DI_8 Inputs			−.25	mA	V_F = .45V
I_F	Input Load Current MD Input			−.75	mA	V_F = .45V
I_F	Input Load Current DS_1 Input			−1.0	mA	V_F = .45V
I_R	Input Leakage Current ACK, DS, CR, DI_1-DI_8 Inputs			10	μA	$V_R \leq V_{CC}$
I_R	Input Leakage Current MO Input			30	μA	$V_R \leq V_{CC}$
I_R	Input Leakage Current DS_1 Input			40	μA	$V_R \leq V_{CC}$
V_C	Input Forward Voltage Clamp			−1	V	I_C = −5 mA
V_{IL}	Input "Low" Voltage			.85	V	
V_{IH}	Input "High" Voltage	2.0			V	
V_{OL}	Output "Low" Voltage			.45	V	I_{OL} = 15 mA
V_{OH}	Output "High" Voltage	3.65	4.0		V	I_{OH} = −1 mA
I_{SC}	Short Circuit Output Current	-15		-75	mA	V_O = 0V, V_{CC} = 5.0V
I_O	Output Leakage Current High Impedance State			20	μA	V_O = .45V/5.25V
I_{CC}	Power Supply Current		90	130	mA	

TYPICAL CHARACTERISTICS

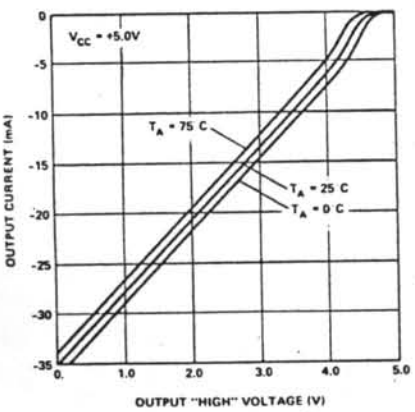
INPUT CURRENT VS. INPUT VOLTAGE



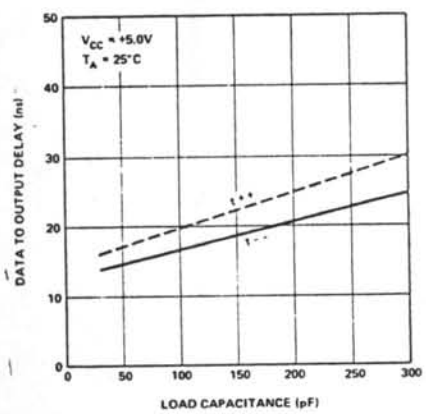
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



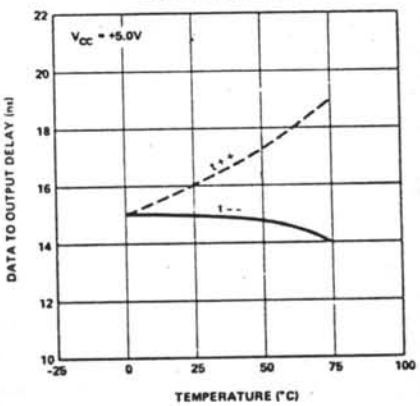
OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



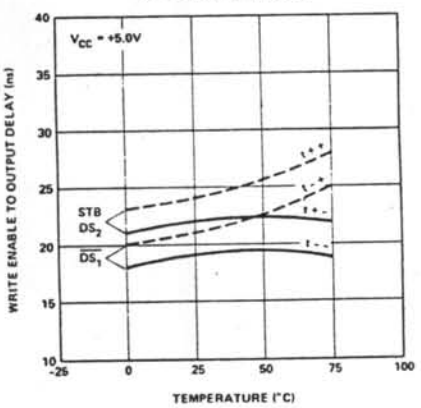
DATA TO OUTPUT DELAY VS. LOAD CAPACITANCE



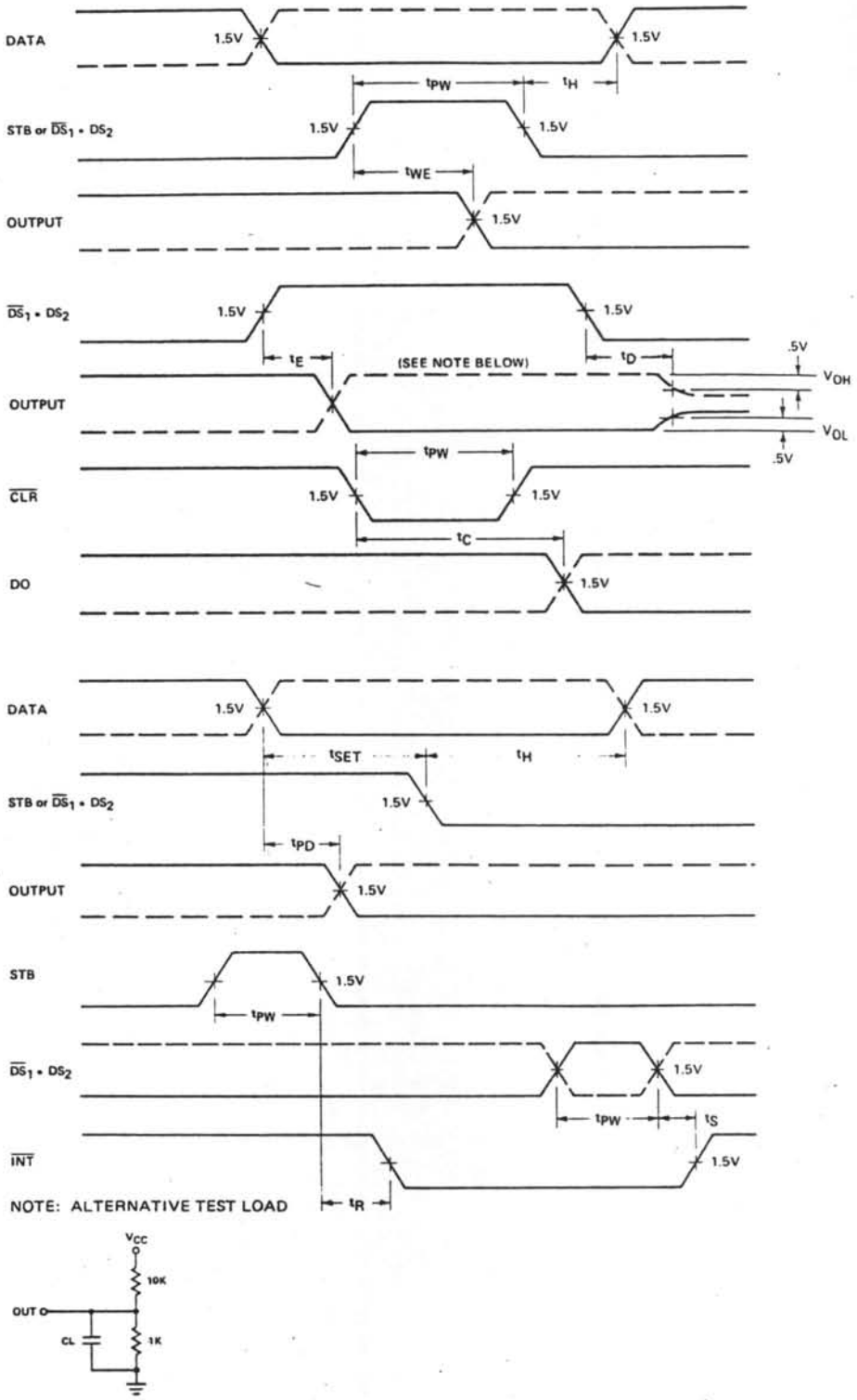
DATA TO OUTPUT DELAY VS. TEMPERATURE



WRITE ENABLE TO OUTPUT DELAY VS. TEMPERATURE



TIMING DIAGRAM



NOTE: ALTERNATIVE TEST LOAD

A.C. CHARACTERISTICS

T_A = 0°C to +75°C, V_{CC} = +5V ±5%

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.	Max.		
t_{pw}	Pulse Width	25			ns	
t_{pd}	Data To Output Delay			30	ns	
t_{we}	Write Enable To Output Delay			40	ns	
t_{ds}	Data Setup Time	15			ns	
t_{dh}	Data Hold Time	20			ns	
t_r	Reset To Output Delay			40	ns	
t_s	Set To Output Delay			30	ns	
t_{en}	Output Enable/Disable Time			45	ns	
t_c	Clear To Output Delay			55	ns	

CAPACITANCE*

F = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = +5V, T_A = 25°C

Symbol	Test	LIMITS	
		Typ.	Max.
C_{IN}	DS, MD Input Capacitance	9 pF	12 pF
C_{IN}	DS_2, CK, ACK, DI_1-DI_8 Input Capacitance	5 pF	9 pF
C_{OUT}	DO_1-DO_8 Output Capacitance	8 pF	12 pF

*This parameter is sampled and not 100% tested.

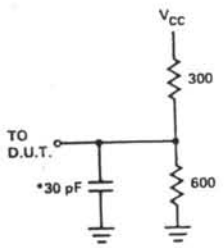
SWITCHING CHARACTERISTICS

Conditions of Test

Input Pulse Amplitude = 2.5 V
Input Rise and Fall Times 5 ns
Between 1V and 2V Measurements made at 1.5V
with 15 mA & 30 pF Test Load

Test Load

15mA & 30pF



* INCLUDING JIG & PROBE CAPACITANCE

2560-BIT STATIC CHARACTER GENERATOR (64x8x5) 2513

2513-NJ

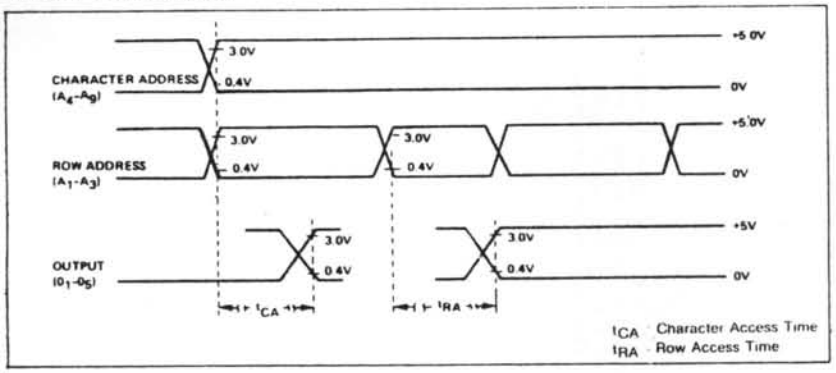
DESCRIPTION

The Signetics 2513 is a high speed 2560-bit Static ROM organized as 64x8x5. A standard 7x5 dot matrix fits well in the 2513. The product uses +5V, -5V and -12V power supplies, TTL level interface signals and Tri-State Outputs for direct, low cost interfacing with TTL, DTL, CMOS and 2500 Series MOS.

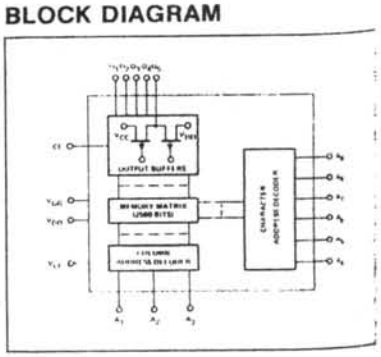
CE	OUTPUT
0	DATA
1	OPEN

PIN CONFIGURATION

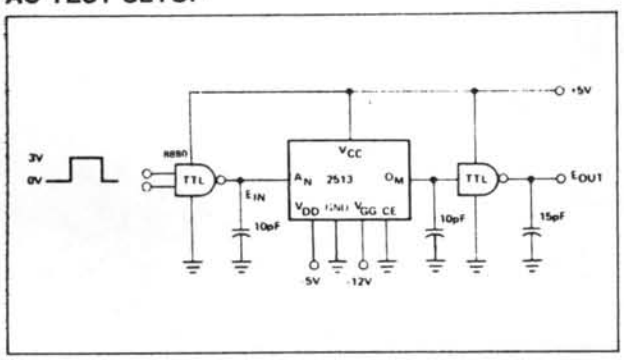
TIMING DIAGRAM



BLOCK DIAGRAM



AC TEST SETUP



AC CHARACTERISTICS

SYMBOL	TEST	MIN	TYP	MAX	UNIT
$t_{CA(CM2140)}$	Character Access Time			600	ns
t_{RA}	Row Access Time (A_1 - A_3)			500	ns
t_{CE}	Chip Enable to Output				ns

T_A = 0°C to +70°C; V_{CC} = 5V (Note 8); V_{DD} = -5V ± 5%; V_{GG} = -12V ± 5%; unless otherwise noted.

COMPANY_____
ADDRESS_____
CITY_____ STATE _____ ZIP_____
TELEPHONE_____
AUTHORIZED
SIGNATURE _____
DATE _____
CUSTOMER PRINT OR ID NO. _____
PURCHASE ORDER NUMBER _____
DEVICE TYPE _____ 2513 _____
CUSTOM PATTERN NUMBER (TO BE ENTERED BY SIGNETICS) _____

CHARACTER FORMAT

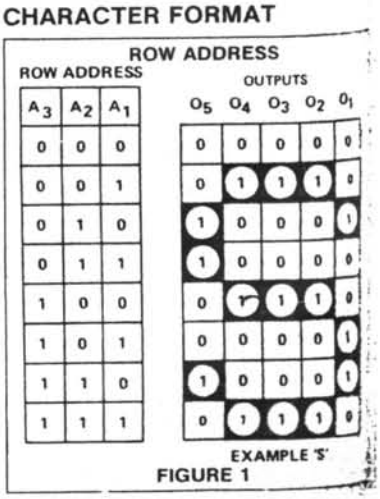


FIGURE 1

ORGANIZATION AS CHARACTER GENERATOR

A six-bit binary address (A4 through A9) selects 1-of-64 matrix characters arranged 5 dots horizontally and 8 dots vertically. A three bit binary address code (A1 through A3) selects 1 of 8 rows. Five outputs display a complete row of the character matrix. See Figure 1. The devices may also be used in pairs to provide 9 X 7 and 10 X 8 vertical scan formats.

2560-BIT STATIC CHARACTER GENERATOR (64x8x5) 2513

2513-N,I

CHARACTER ADDRESS

COLUMN ADDRESS

	A_4	A_5	A_6	A_7	A_8	A_9
ASCII CHARACTER	1	1	0	0	1	0

FIGURE 2

ORGANIZATION AS READ-ONLY MEMORY

For a straight 512 X 5 read-only memory, the five outputs will display any one of 512 5-bit stored words corresponding to a 9-bit address applied to A_1 through Ag.

CUSTOM DEVICES

For unique custom memory patterns, this form should be used to transmit coding instructions. The nomenclature for a custom device will consist of he basic product type followed by a unique CM number assigned by Signetics. For example, "2513N/CM2141".

■ PROGRAMMING WITH PUNCHED CARDS

For maximum accuracy and minimum cost and turn-around time, the truth table should be transmitted to Signetics in the form of punched cards according to the format indicated on the following pages.

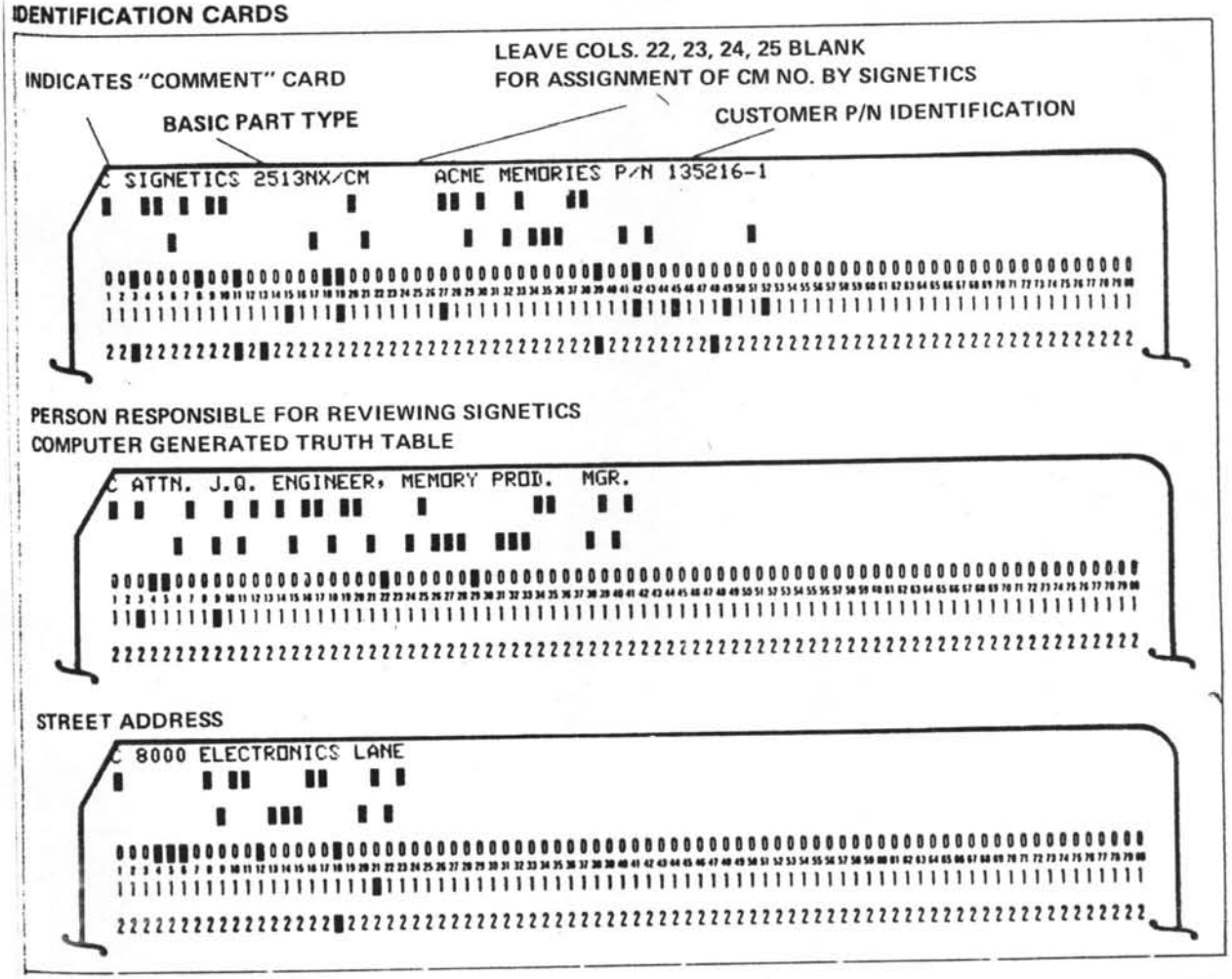
VERIFICATION

Upon receipt of either punched card or written truth table information, Signetics will prepare a computer tabulation of the instructions and return to the address indicated. If errors are detected, they should be transmitted to Signetics as quickly as possible.

LOGIC CONVENTION

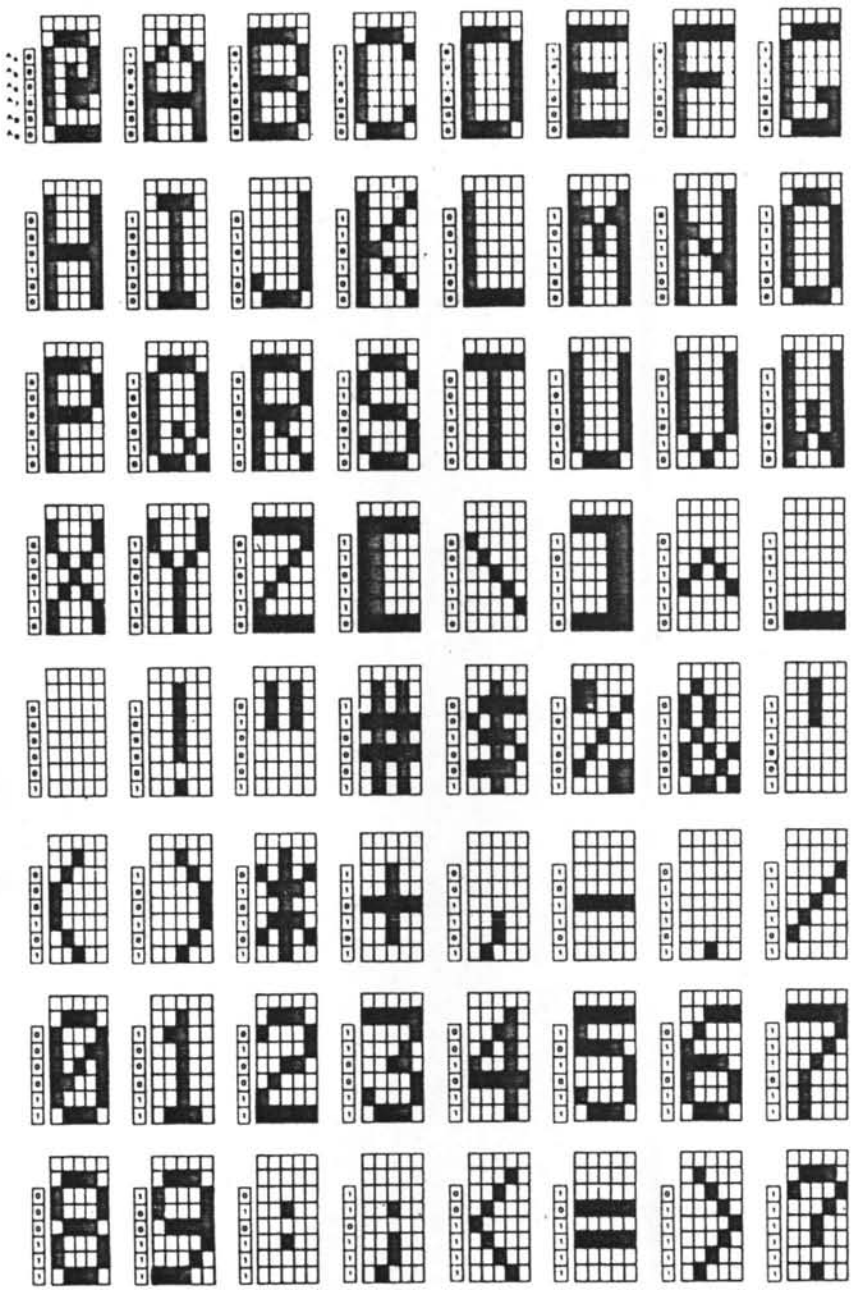
Logic "1"s or blackened squares in the truth table will result in "high" output from the indicated output terminal (i.e. 3.2V minimum). Similarly, a "1" address input level is interpreted as 3.2V minimum.

IDENTIFICATION CARDS



2560-BIT STATIC CHARACTER GENERATOR (64x8x5)

ASCII CHARACTER FONT CM2140 (Upper Case); For Lower Case Order CM3021



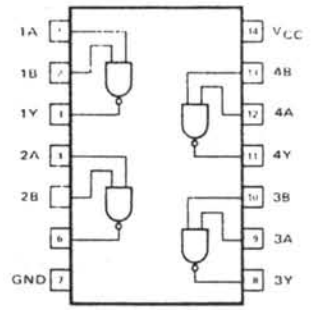
QUAD 2-INPUT NAND GATE — 54/7400

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

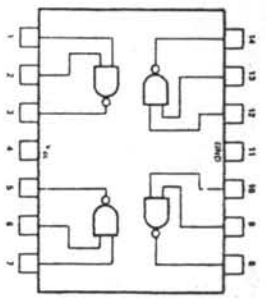
PIN CONFIGURATION

54/74, 54/74LS, 54S
A,F,W PACKAGE



Positive logic: $Y = \overline{AB}$

54/74H
W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time													
t_{PLH} Low-to-high		11	22		5.9	10		9	15	2	3	4.5	ns
											C_L=50pF		
											4.5		
t_{PHL} High-to-low		7	15		6.2	10		10	15	2	3	5	ns
											C_L=50pF		
											5		

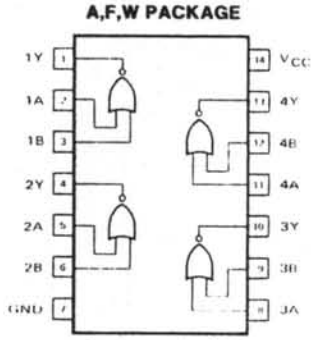
QUAD 2-INPUT NOR GATE — 54/7402

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

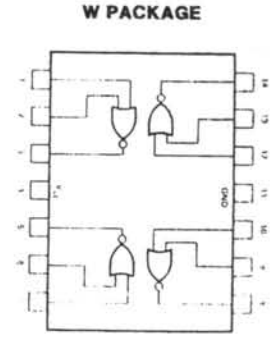
PIN CONFIGURATION

74,54/74LS, 54/74S
A,F,W PACKAGE



Positive logic: $Y = \overline{A+B}$

54
W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

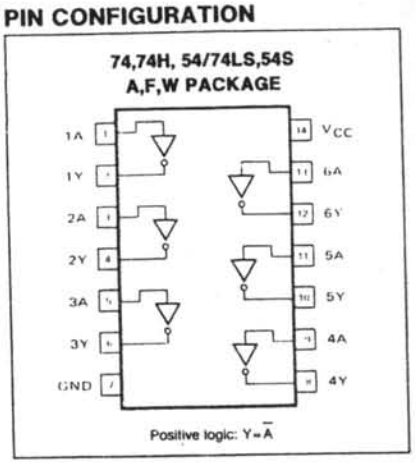
TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time										
t_{PLH} Low-to-high		12	22		8	15		3.5	5.5	ns
t_{PHL} High-to-low		8	15		8	15		3.5	5.5	ns

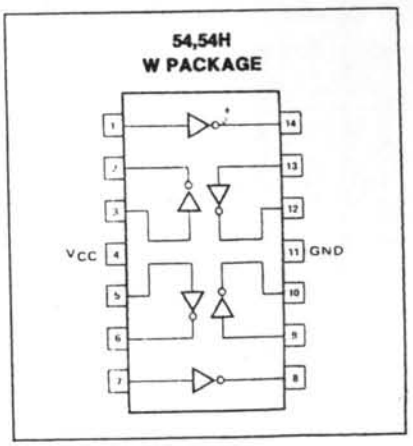
HEX INVERTER 54/7404

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

PIN CONFIGURATION





SWITCHING CHARACTERISTICS V_{CC}= 5V, T_A = 25°C

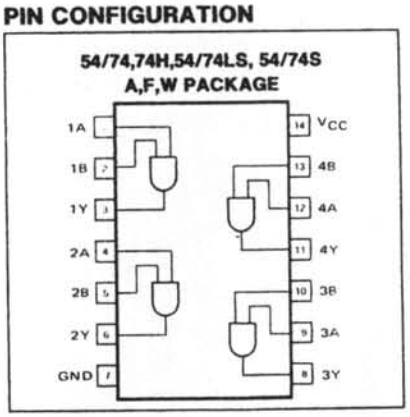
TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			UNIT
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation delay time t_{PLH} Low-to-high		12	22		6	10		5	15	2	3 / C_L=50pF 4.5	4.5	ns
t_{PHL} High-to-low		8	15		6.5	10		9	15	2	3 / C_L=50pF 5	5	ns

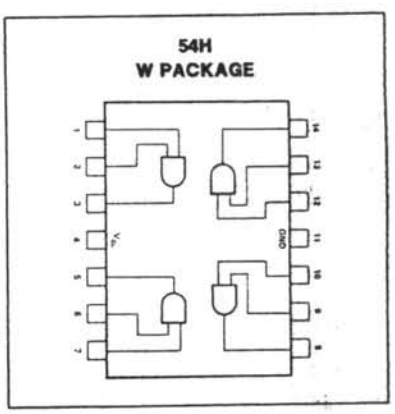
QUAD 2-INPUT AND GATE 54/7408

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

PIN CONFIGURATION





SWITCHING CHARACTERISTICS V_{CC}= 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L=15pF R_L=400Ω			54/74H C_L=25pF R_L=280Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			UNIT
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation delay time t_{PLH} Low-to-high		17.5	27		7.6	12		8.5	15		4.5 / C_L=50pF 6	7	ns
t_{PHL} High-to-low		12	19		8.8	12		8	20		5 / C_L=50pF 7.5	7.5	ns

HEX INVERTER/BUFFER 54/7416

SPEED/PACKAGE AVAILABILITY

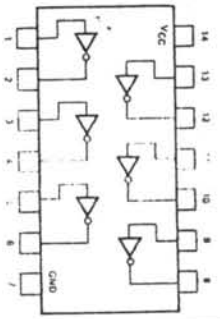
54 F,W 74 A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L = 15pF R_L = 110Ω			
PARAMETER	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		10	15	ns
t_{PHL} High-to-low		15	23	ns

PIN CONFIGURATION

A,F,W PACKAGE



QUAD 2-INPUT OR GATE 54/7432

SPEED/PACKAGE AVAILABILITY

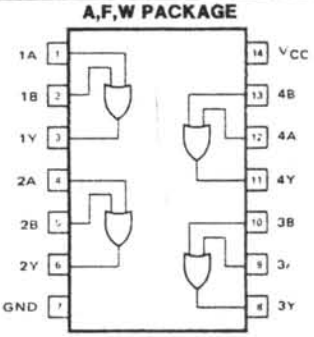
54 F,W 74 A,F
54LS F,W 74LS A,F

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L = 15pF R_L = 400Ω			54/74LS C_L = 15pF R_L = 2kΩ			
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time t_{PLH} Low-to-high		10	15		9	22	ns
t_{PHL} High-to-low		14	22		9	22	ns

PIN CONFIGURATION

A,F,W PACKAGE



Positive logic: y = A+B

BCD-TO-DECIMAL DECODER (1-of-10) 54/7442

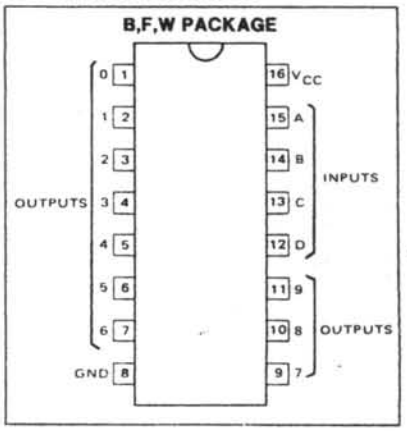
SPEED/PACKAGE AVAILABILITY

54 F,W 74 B,F
54LS F,W 74LS B,F

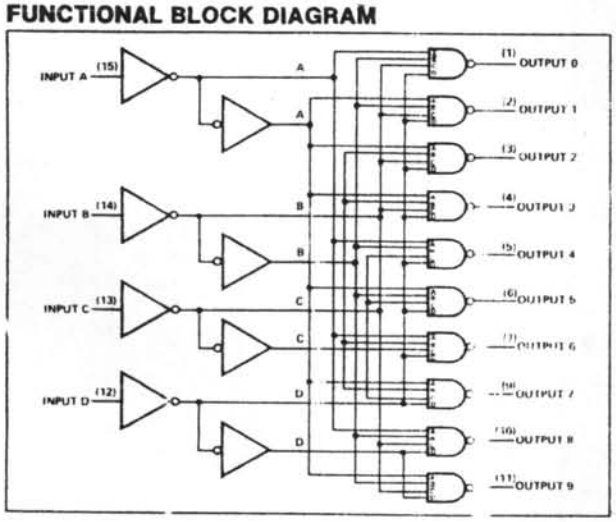
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2KΩ			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time									
t_{PLH} Low-to-high	A,B,C,D	through 2 logic		10	25		10	25	ns
t_{PHL} High-to-low		levels		14	25		14	25	
t_{PLH} Low-to-high	A,B,C,D	through 3 logic		17	30		17	30	ns
t_{PHL} High-to-low		levels		17	30		17	30	

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



FUNCTION TABLE

NO.	BCD INPUT				DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

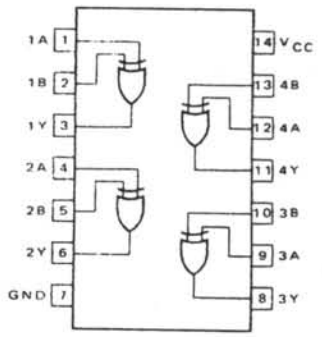
QUAD 2-INPUT EXCLUSIVE-OR GATE 54/7486

SPEED/PACKAGE AVAILABILITY

54	F,W	74	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

PIN CONFIGURATION

A,F,W PACKAGE



positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L = 15pF R_L = 400Ω			54/74LS C_L = 15pF R_L = 2k			54/74S C_L = 15pF R_L = 280			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Propagation delay time		A or B											
t_{PLH}	Low-to-high	Other input low			15	23		12	23		7	10.5	ns
t_{PHL}	High-to-low	A or B			11	17		10	17		6.5	10	
t_{PLH}	Low-to-high	Other input high			18	30		10	30		7	10.5	
t_{PHL}	High-to-low				13	22		18	22		6.5	10	

SN54LS165/SN74LS165
8-BIT PARALLEL-TO-SERIAL CONVERTER

DESCRIPTION—The 54LS/74LS165 is an 8-bit parallel load or serial-in register with complementary outputs available from the last stage. Parallel inputing occurs asynchronously when the Parallel Load ($\overline{PL}$) input is LOW. With $\overline{PL}$ HIGH, serial shifting occurs on the rising edge of the clock; new data enters via the Serial Data (DS) input. The 2-input OR clock can be used to combine two independent clock sources, or one input can act as an active LOW clock enable.

PIN NAMES

		LOADING (Note a) HIGH	LOW
CP_1, CP_2	Clock (LOW-to-HIGH Going Edge) Inputs	0.5 U.L.	0.25 U.L.
$\overline{DS}$	Serial Data Input	0.5 U.L.	0.25 U.L.
$\overline{PL}$	Asynchronous Parallel Load (Active LOW) Input	1.5 U.L.	0.75 U.L.
P_0-P_7	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_7	Serial Output from Last State (Note b)	10 U.L.	5 (2.5) U.L.
$\overline{Q}_7$	Complementary Output (Note b)	10 U.L.	5 (2.5) U.L.

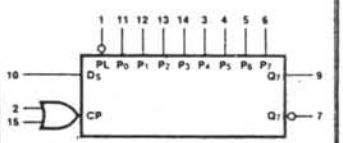
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

TRUTH TABLE

$\overline{PL}$	CP 1	CP 2	CONTENTS Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	$\overline{Q}_7$	RESPONSE
L	X	X	P_0	P_1	P_2	P_3	P_4	P_5	P_6	P_7	Parallel Entry
H	L	↓	D_S	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Right Shift
H	H	↓	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	No Change
H	↓	L	D_S	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Right Shift
H	↓	H	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	No Change

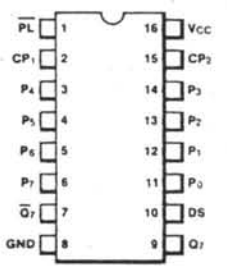
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC SYMBOL



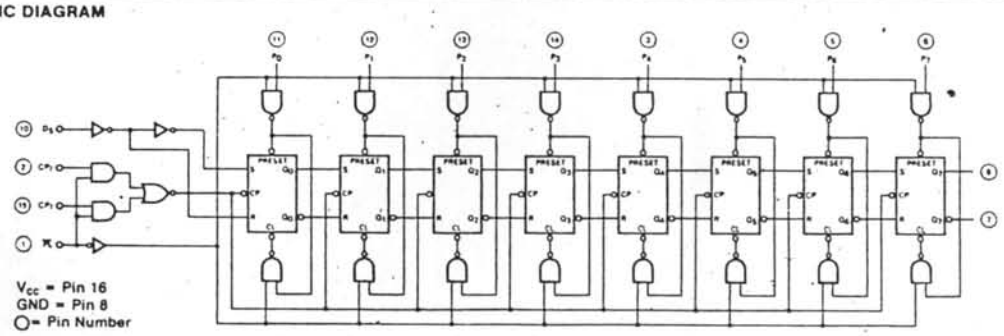
V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Number

FUNCTIONAL DESCRIPTION – The 54LS/74LS165 contains eight clocked master/slave RS flip-flops connected as a shift register, with auxiliary gating to provide overriding asynchronous parallel entry. Parallel data enters when the $\overline{PL}$ signal is LOW. The parallel data can change while $\overline{PL}$ is LOW, provided that the recommended set-up and hold times are observed.

For clock operation, $\overline{PL}$ must be HIGH. The two clock inputs perform identically; one can be used as a clock inhibit by applying a HIGH signal. To avoid double clocking, however, the inhibit signal should only go HIGH while the clock is HIGH. Otherwise, the rising inhibit signal will cause the same response as a rising clock edge. The flip-flops are edge-triggered for serial operations. The serial input data can change at any time, provided only that the recommended set-up and hold times are observed, with respect to the rising edge of the clock.

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS165X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS165X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5			V	I_{OH} = -400 μA V_{CC} = MIN
		74	2.7				V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4 mA; V_{CC} = MIN V_{IN} = V_{IH} or
		74		0.35	0.5		I_{OL} = 8 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current CP, DS, P_0-P_7				20	μA	V_{CC} = MAX
	$\overline{PL}$				60		V_{IN} = 2.7 V
	CP, DS, P_0-P_7				0.1	mA	V_{CC} = MAX
	$\overline{PL}$				0.3		V_{IN} = 10 V
I_{IL}	Input LOW Current CP, DS, P_0-P_7				−0.4	mA	V_{CC} = MAX
	$\overline{PL}$				−1.2		V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX V_{OUT} = 0 V
I_{CC}	Power Supply Current				36	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operations under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

SN54LS165/SN74LS165

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
f_{MAX}	Maximum Input Clock Frequency	30	45		MHz	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Clock to Output			30 30	ns	Fig. 1	
t_{PLH} t_{PHL}	Propagation Delay, $\overline{PL}$ to Output			30 30	ns	Fig. 2	

AC SET-UP REQUIREMENTS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS	
		MIN	TYP	MAX			
T_w	CP Pulse Width	20			ns	Fig. 1	V_{CC} = 5.0 V C_L = 15 pF
T_w	$\overline{PL}$ Pulse Width	15			ns	Fig. 2	
T_sL	Set-Up Time LOW, Data to $\overline{PL}$	10			ns	Fig. 3	
T_hL	Hold Time LOW, Data to $\overline{PL}$	5			ns	Fig. 3	
T_sH	Set-Up Time HIGH, Data to $\overline{PL}$	10			ns	Fig. 3	
T_hH	Hold Time HIGH, Data to $\overline{PL}$	5			ns	Fig. 3	
T_sL	Set-Up Time LOW, Data to Clock	10			ns	Fig. 3	
T_hL	Hold Time LOW, Data to Clock	5			ns	Fig. 3	
T_sH	Set-Up Time HIGH, Data to Clock	10			ns	Fig. 3	
T_hH	Hold Time HIGH, Data to Clock	5			ns	Fig. 3	
T_{rec}	Recovery Time, $\overline{PL}$ to CP	15			ns	Fig. 4	

DEFINITION OF TERMS:

SET-UP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative hold time indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW-to-HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

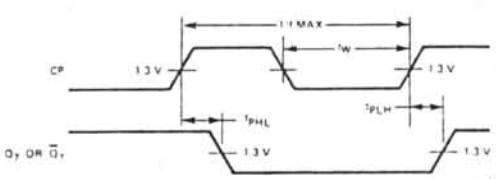


Fig.1

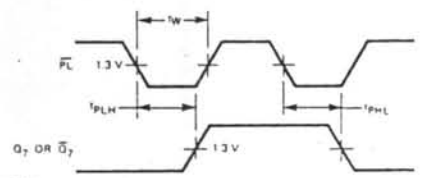


Fig. 2

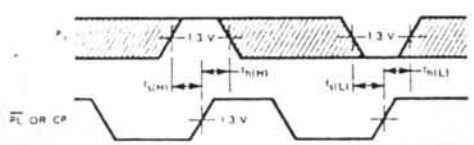


Fig. 3

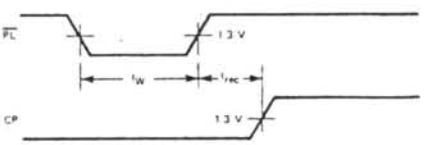


Fig. 4

SN54LS168/SN74LS168 • SN54LS169/SN74LS169

BCD DECADE — MODULO 16 BINARY SYNCHRONOUS BI-DIRECTIONAL COUNTERS

DESCRIPTION – The 54LS/74LS168 and 54LS/74LS169 are fully synchronous 4-stage up/down counters featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. The 54LS/74LS168 counts in a BCD decade (8, 4, 2, 1) sequence, while the 54LS/74LS169 operates in a Modulo 16 binary sequence. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

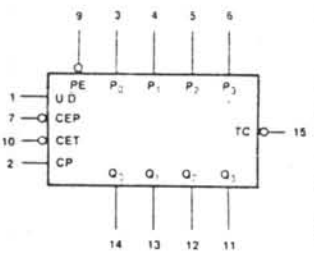
- LOW POWER DISSIPATION 100mW TYPICAL
- HIGH-SPEED COUNT FREQUENCY 30 MHz TYPICAL
- FULLY SYNCHRONOUS OPERATION
- FULL CARRY LOOKAHEAD FOR EASY CASCADING
- SINGLE UP/DOWN CONTROL INPUT
- POSITIVE EDGE-TRIGGER OPERATION
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{CEP}$	Count Enable Parallel (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{CET}$	Count Enable Trickle (Active LOW) Input	1.0 U.L.	0.5 U.L.
$\overline{CP}$	Clock Pulse (Active positive going edge) Input	0.5 U.L.	0.25 U.L.
$\overline{PE}$	Parallel Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
U/$\overline{D}$	Up-Down Count Control Input	0.5 U.L.	0.25 U.L.
P_0-P_3	Parallel Data Inputs	0.5 U.L.	0.25 U.L.
Q_0-Q_3	Flip-Flop Outputs	10 U.L.	5 (2.5) U.L.
$\overline{TC}$	Terminal Count (Active LOW) Output	10 U.L.	5 (2.5) U.L.

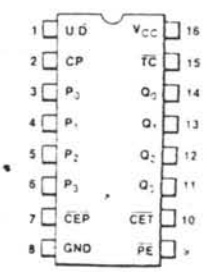
NOTES:
a. 1 TTL Unit Load (U.L.) = 40μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

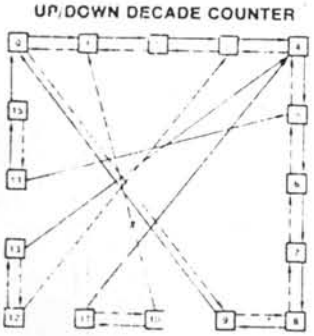
CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

STATE DIAGRAMS

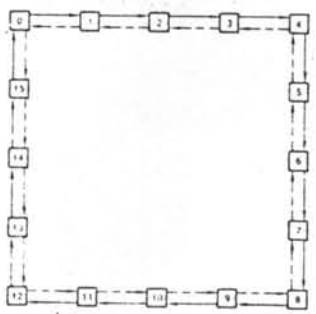
F54LS/74LS168
UP/DOWN DECADE COUNTER



54LS/74LS168
UP TC = $Q_0 \cdot Q_3 \cdot (U/\overline{D})$
DOWN TC = $\overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (U/\overline{D})$

——— Count Up
— — — Count Down

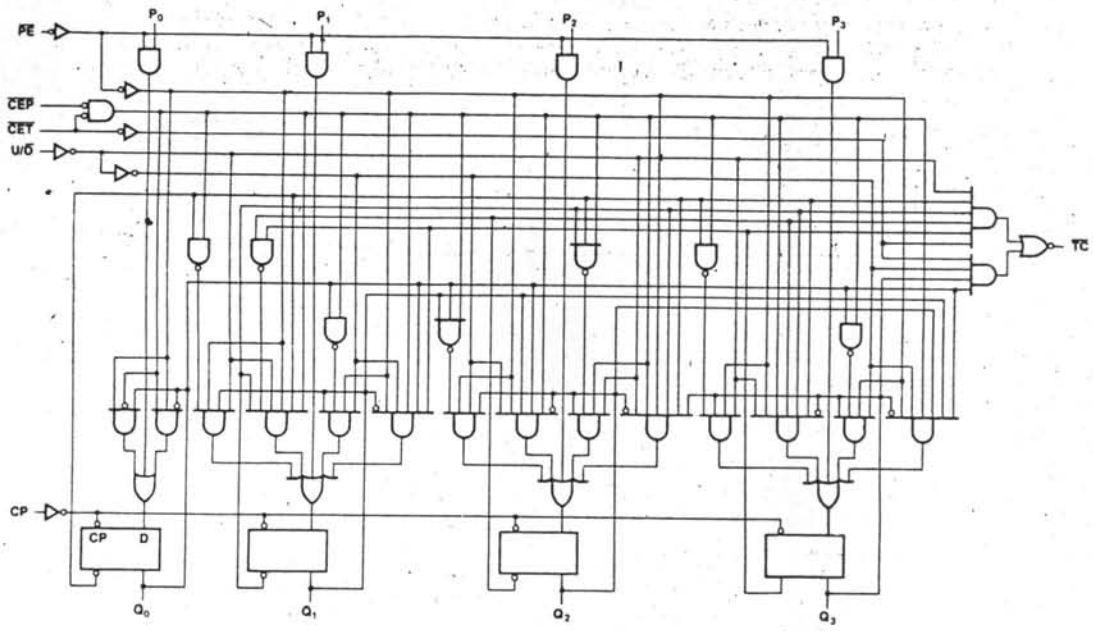
F54LS/74LS169



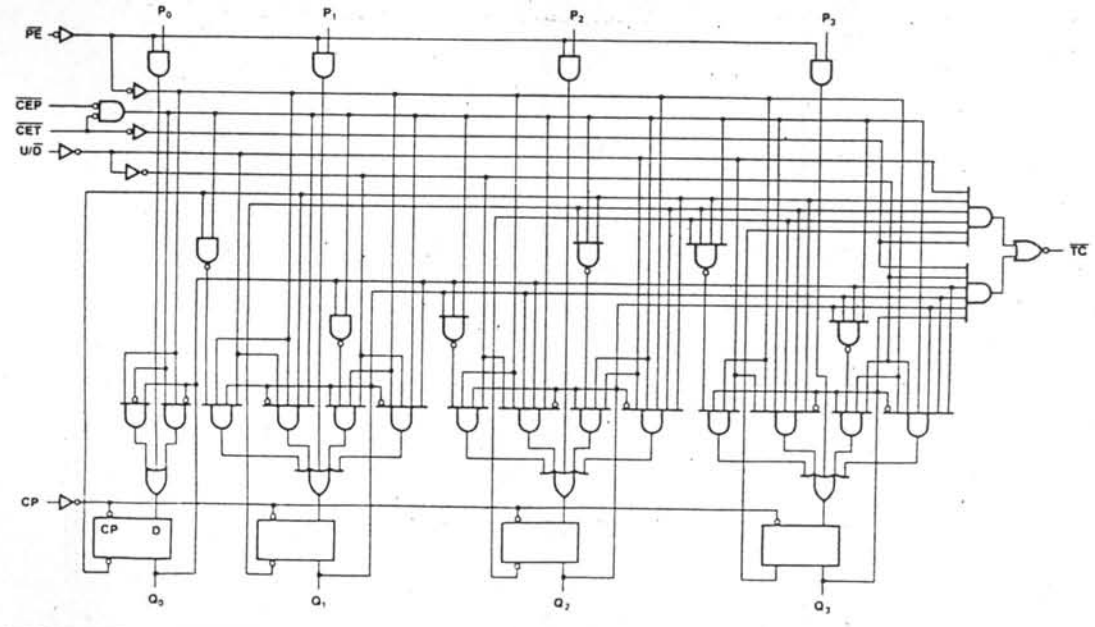
54LS/74LS169
UP TC = $Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (U/\overline{D})$
DOWN TC = $\overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (U/\overline{D})$

LOGIC DIAGRAMS

54LS/74LS168



54LS/74LS169



SN54LS168/SN74LS168 • SN54LS169/SN74LS169

FUNCTIONAL DESCRIPTION – The 54LS/74LS168 and 54LS/74LS169 use edge-triggered D-type flip-flops and that have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a set-up time before the rising edge of the clock and remain valid for the recommended hold time thereafter.

The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the P_0-P_3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH. The U/$\overline{D}$ input then determines the direction of counting.

The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the COUNT DOWN mode or reaches 15 (9 for the 54LS/74LS168) in the COUNT UP mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the 54LS/74LS168 decade counter can also be LOW in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the 54LS/74LS168 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended.

MODE SELECT TABLE

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load (Pn→Qn)
H	L	L	H	Count Up (increment)
H	L	L	L	Count Down (decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = immaterial

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS168/54LS169X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS168/74LS169X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5			
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5		I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current U/$\overline{D}$ CP, $\overline{PE}$ $\overline{CEP}$, P_0-P $\overline{CET}$				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					40		
	U/$\overline{D}$, CP, $\overline{PE}$, $\overline{CEP}$, P_0-P_3 $\overline{CET}$				0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
					0.2		
I_{IL}	Input LOW Current U/$\overline{D}$, CP, $\overline{PE}$, $\overline{CEP}$, P_0-P_3 $\overline{CET}$				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
					−0.8		
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			20	34	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the table, are chosen to guarantee operations under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS : T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH}	CP to Q		15	20	ns	Fig. 1	C_L = 15 pF
t_{PHL}			15	20			
t_{PLH}	CP to $\overline{TC}$		22	30	ns	Fig. 3	
t_{PHL}			22	30			
t_{PLH}	$\overline{CET}$ to $\overline{TC}$		10	15	ns	Fig. 2	
t_{PHL}			15	20			
t_{PLH}	U/$\overline{D}$ to $\overline{TC}$		20	25	ns	Fig. 6	
t_{PHL}			20	25			
f_{MAX}	Maximum Clock Frequency	25	32		MHz	Fig. 1	

AC SET-UP REQUIREMENTS: $T_A = 25°C$

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
$t_s(L)$	Set-up LOW, Data to CP	15	12		ns	Fig. 4	V_{CC} = 5.0 V
$t_s(H)$	Set-up HIGH, Data to CP	15	12				
$t_h(L)$	Hold LOW Data to CP	5.0	0		ns	Fig. 4	
$t_h(H)$	Hold HIGH, Data to CP	5.0	0				
$t_s(L)$	Set-up LOW, $\overline{PE}$ to CP	15	12		ns	Fig. 5	
$t_s(H)$	Set-up HIGH, $\overline{PE}$ to CP	15	12				
$t_h(L)$	Hold LOW, $\overline{PE}$ to CP	5.0	0		ns	Fig. 5	
$t_h(H)$	Hold HIGH, $\overline{PE}$ to CP	5.0	0				
$t_s(L)$	Set-up LOW, $\overline{CET}$ or $\overline{CEP}$ to CP	15	12		ns	Fig. 5	
$t_s(H)$	Set-up HIGH, $\overline{CET}$ or $\overline{CEP}$ to CP	15	12				
$t_h(L)$	Hold LOW, $\overline{CET}$ or $\overline{CEP}$ to CP	15	12		ns	Fig. 5	
$t_h(H)$	Set-up HIGH, $\overline{CET}$ or $\overline{CEP}$ to CP	15	12				
$t_h(H)$	Set-up LOW, U/$\overline{D}$ to CP	25	20		ns	Fig. 6	
$t_h(H)$	Set-up HIGH, U/$\overline{D}$ to CP	25	20				
$t_h(L)$	Hold LOW, U/$\overline{D}$ to CP	0	−4.0		ns	Fig. 6	
$t_h(H)$	Hold HIGH, U/$\overline{D}$ to CP	0	−4.0				
t_wCP(L)	Clock Pulse Width LOW	20	18		ns	Fig. 1	
t_wCP(H)	Clock Pulse Width HIGH	10	5.0				

DEFINITION OF TERMS:

SET-UP TIME (t_s) – is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW-to-HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) – is defined as the minimum time following the clock transition from LOW-to-HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW-to-HIGH and still be recognized.

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, COUNT FREQUENCY, AND CLOCK PULSE WIDTH.

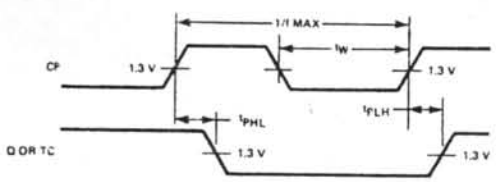


Fig. 1

COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS

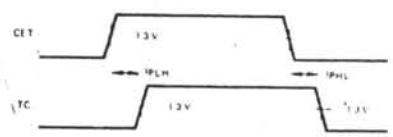


Fig. 2

CLOCK TO TERMINAL DELAYS

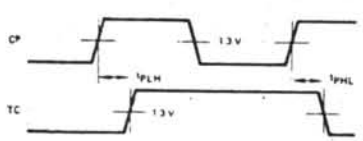


Fig. 3

SET-UP TIME (t_s) AND HOLD (t_h) FOR PARALLEL DATA INPUTS.

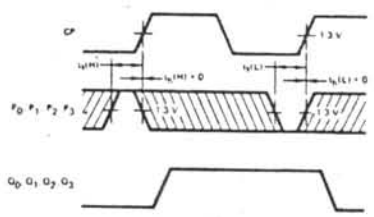
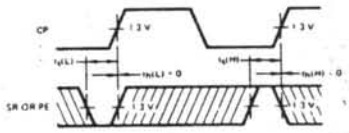
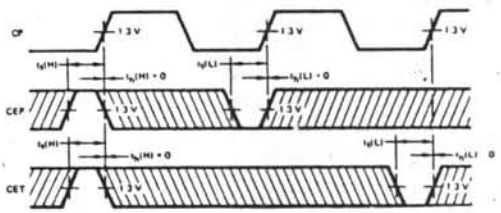


Fig. 4

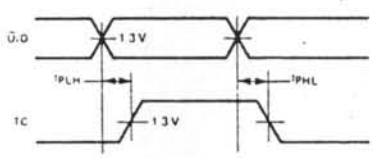


Set-up time (t_s) and hold time (t_h) for count enable (CEP) and (CET), parallel enable (PE) inputs, and up-down (U/D) control inputs.



The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 5



Up-Down input to Terminal Count Output Delays

Fig. 6

HEX D-TYPE FLIP-FLOP WITH CLEAR 54/74174

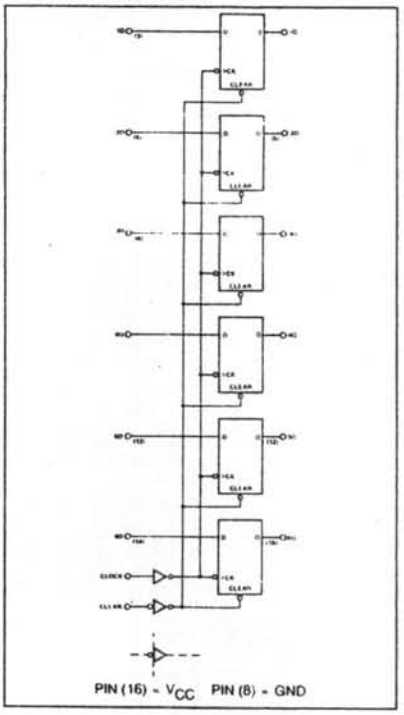
SPEED/PACKAGE AVAILABILITY

54	F,W	74	B
54LS	F,W	74LS	B
		74S	B

DESCRIPTION

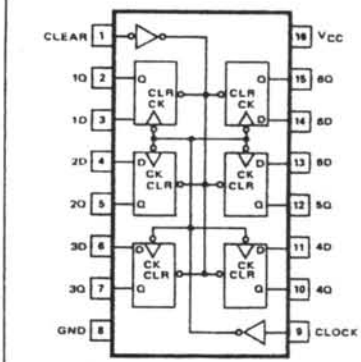
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the input signal has no effect at the output.

BLOCK DIAGRAM



PIN CONFIGURATION

B,F,W PACKAGE



TRUTH TABLE (Each Flip-Flop)

INPUTS			OUTPUTS
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			54/74S C_L=15pF R_L=280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			25	35		30	40		75	110		MHz
t_w	Width of pulse												
	Clock			20			20			12			ns
	Clear												
t_{Setup}	Input setup time												ns
	Data			20			20↑			8			
	Clear inactive			25			25↑			15			
t_{Hold}	Input hold time			0			5↑			2			ns
Propagation delay time													
t_{PLH}	Low-to-high	Clock			20	30		20	30		9	12	ns
t_{PHL}	High-to-low				21	30		21	35		11	17	
t_{PHL}	High-to-low	Clear	Q		23	35		23	35		13	22	

ภาคผนวก ข.

```
                        ;
                        ;       MONITOR  CRT  PROGRAM
                        ;         5  SEPTEMBER  1980
                        ;
0000                            ORG     0
0000 3E8A                       MVI     A,8AH
0002 D360                       OUT     ME3
0004 210004                     LXI     H,0400H
0007 31FF0B                     LXI     SP,STACK
000A C33300                     JMP     INA75
0030                            ORG     30H
0030 C31302                     JMP     INTSUM
                        ;
                        ;       INITIAL ROUTINE  "8275 CRT"
                        ;
0033 3E00               INA75   MVI     A,00H
0035 D391                       OUT     SUC
0037 3EBF                       MVI     A,0BFH
0039 D390                       OUT     SUP
003B 3E8F                       MVI     A,8FH
003D D390                       OUT     SUP
003F 3E77                       MVI     A,77H
0041 D390                       OUT     SUP
0043 3E09                       MVI     A,09H
0045 D390                       OUT     SUP
0047 3EA0                       MVI     A,0A0H
0049 D391                       OUT     SUC
004B 3E2F                       MVI     A,2FH
004D D391                       OUT     SUC
                        ;
                        ;       POWER  UP
                        ;       CLEAR MEMORY & HOME CURSOR
                        ;
004F 3E20               LOPP    MVI     A,20H
0051 77                         MOV     M,A
0052 7C                         MOV     A,H
0053 FE0B                       CPI     0BH
0055 CA5C00                     JZ      CMMHP
0058 23                 CMMLP   INX     H
0059 C34F00                     JMP     LOPP
005C 7D                 CMMHP   MOV     A,L
005D FEFF                       CPI     0FFH
005F CA6500                     JZ      CHOM1
0062 C35800                     JMP     CMMLP
0065 210004             CHOM1   LXI     H,0400H
0068 010000                     LXI     B,0000H
```

```
                        ;       INITIALIZE INTERFACE
                        ;
006B D3F4       PINIT   OUT     PREST
006D D3F5               OUT     PBOUD
006F CD2801     CRCHK   CALL    INKEY
0072 FE08               CPI     08H
0074 CA7A00             JZ      STIF
0077 C36F00             JMP     CRCHK
007A DB20       STIF    IN      ME1
007C B7                 ORA     A
007D F27A00             JP      STIF
0080 DBF4               IN      PREG2
0082 E608               ANI     08H
0084 CA8F00             JZ      HALFD
0087 3E04               MVI     A,04H
0089 D3F6               OUT     PREG3
008B FB                 EI
008C C39400             JMP     INPUT
008F 3E06       HALFD   MVI     A,06H
0091 D3F6               OUT     PREG3
0093 FB                 EI
                        ;
                        ;       MONITOR  START
                        ;
0094 CD7602     INPUT   CALL    PIST
0097 DB20               IN      ME1
0099 B7                 ORA     A
009A FA9400             JM      INPUT
009D DB20               IN      ME1
009F F5                 PUSH    PSW
00A0 DB20       OKEY    IN      ME1
00A2 B7                 ORA     A
00A3 F2A000             JP      OKEY
00A6 F1                 POP     PSW
00A7 FE0F               CPI     0FH
00A9 CA9400             JZ      INPUT
00AC FE03               CPI     03H     ; CURSOR RIGHT
00AE CAFE00             JZ      CRT
00B1 FE17               CPI     17H     ; CURSOR  LEFT
00B3 CA0401             JZ      CLEF
00B6 FE04               CPI     04H     ; CLEAR MOMERY
00B8 CA0A01             JZ      CLR
00BB FE18               CPI     18H     ; HOME
00BD CA1001             JZ      CHOM
00C0 FE02               CPI     02H     ; CURSOR DOWN
00C2 CA1601             JZ      CROLD
```

```
00C5 FE01              CPI     01H     ; CURSOR UP
00C7 CA1C01            JZ      CUP
00CA FE08              CPI     08H     ; ENTER
00CC CAD200            JZ      EENTT
00CF C3E200            JMP     SSVE
00D2 DBF4      EENTT   IN      PREG2
00D4 E608              ANI     08H
00D6 C2DC00            JNZ     PPPF
00D9 CD0402            CALL    ENTER
00DC 3E0D      PPPF    MVI     A,0DH
00DE F5                PUSH    PSW
00DF C3F700            JMP     FULL
00E2 F5        SSVE    PUSH    PSW
00E3 DBF4              IN      PREG2
00E5 E608              ANI     08H
00E7 C2F700            JNZ     FULL
00EA F1                POP     PSW
00EB 77                MOV     M,A     ; DATA KB TO MM
00EC CD3702            CALL    PSEND
00EF D300              OUT     ME0
00F1 CD8301            CALL    CRITE
00F4 C39400            JMP     INPUT
00F7 F1        FULL    POP     PSW
00F8 CD3702            CALL    PSEND
00FB C39400            JMP     INPUT
                ;
                ;       CALL SUBROUTINE
                ;
00FE CD8301    CRT     CALL    CRITE
0101 C39400            JMP     INPUT
                ;
0104 CD5A01    CLEF    CALL    CLEFT
0107 C39400            JMP     INPUT
                ;
010A CDE401    CLR     CALL    CLEAR
010D C39400            JMP     INPUT
                ;
0110 CD3701    CHOM    CALL    HOME
0113 C39400            JMP     INPUT
                ;
0116 CDAF01    CROLD   CALL    RDOWN
0119 C39400            JMP     INPUT
                ;
011C CD3E01    CUP     CALL    CURUP
011F C39400            JMP     INPUT
                ;
0122 CD0402    ENT     CALL    ENTER
0125 C39400            JMP     INPUT
```

```
                                ;
                                ;
                                ;       INKEY
                                ;
0128 DB20       INKEY   IN      ME1
012A B7                 ORA     A
012B F22801     LOPKB   JP      INKEY
012E DB20               IN      ME1
0130 B7                 ORA     A
0131 FA2B01             JM      LOPKB
0134 DB20               IN      ME1
0136 C9                 RET
                                ;
                                ;       HOME
                                ;
0137 010000     HOME    LXI     B,0000H
013A 210004             LXI     H,0400H
013D C9                 RET
                                ;
                                ;       CURSOR  UP
                                ;
013E 114000     CURUP   LXI     D,0040H
0141 78                 MOV     A,B
0142 FE00               CPI     00H
0144 CA5101             JZ      UPCR
0147 05                 DCR     B
0148 7D                 MOV     A,L
0149 9B                 SBB     E
014A 6F                 MOV     L,A
014B 7C                 MOV     A,H
014C 9A                 SBB     D
014D 67                 MOV     H,A
014E C35901             JMP     UPRET
0151 21C007     UPCR    LXI     H,07C0H
0154 79                 MOV     A,C
0155 85                 ADD     L
0156 6F                 MOV     L,A
0157 060F               MVI     B,0FH
0159 C9         UPRET   RET
```

```
                                ;
                                ;       CURSOR  LEFT
                                ;
015A 78         CLEFT   MOV     A,B
015B FE00               CPI     00H
015D CA6B01             JZ      CTEST
0160 79                 MOV     A,C
0161 FE00               CPI     00H
0163 CA7E01             JZ      CBCR
0166 0D         CDCR    DCR     C
0167 2B                 DCX     H
0168 C38201             JMP     CLRET
016B 79         CTEST   MOV     A,C
016C FE00               CPI     00H
016E CA7401             JZ      CBEGIN
0171 C36601             JMP     CDCR
0174 060F       CBEGIN  MVI     B,0FH
0176 0E3F               MVI     C,3FH
0178 21FF07             LXI     H,07FFH
017B C38201             JMP     CLRET
017E 05         CBCR    DCR     B
017F 0E3F               MVI     C,3FH
0181 2B                 DCX     H
0182 C9         CLRET   RET
                                ;
                                ;       MOVE  CURSOR  RIGHT
                                ;
0183 78         CRITE   MOV     A,B
0184 FE0F               CPI     0FH
0186 CA9401             JZ      CREND
0189 79                 MOV     A,C
018A FE3F               CPI     3FH
018C CA9D01             JZ      CRINR
018F 0C         CRNEXT  INR     C
0190 23                 INX     H
0191 C3AE01             JMP     CRRET
0194 79         CREND   MOV     A,C
0195 FE3F               CPI     3FH
0197 CAA401             JZ      CRLRP
019A C38F01             JMP     CRNEXT
019D 23         CRINR   INX     H
019E 04                 INR     B
019F 0E00               MVI     C,00H
01A1 C3AE01             JMP     CRRET
01A4 CDCE01     CRLRP   CALL    ROLLUP
01A7 060F               MVI     B,0FH
01A9 0E00               MVI     C,00H
01AB 21C007             LXI     H,07C0H
01AE C9         CRRET   RET
```

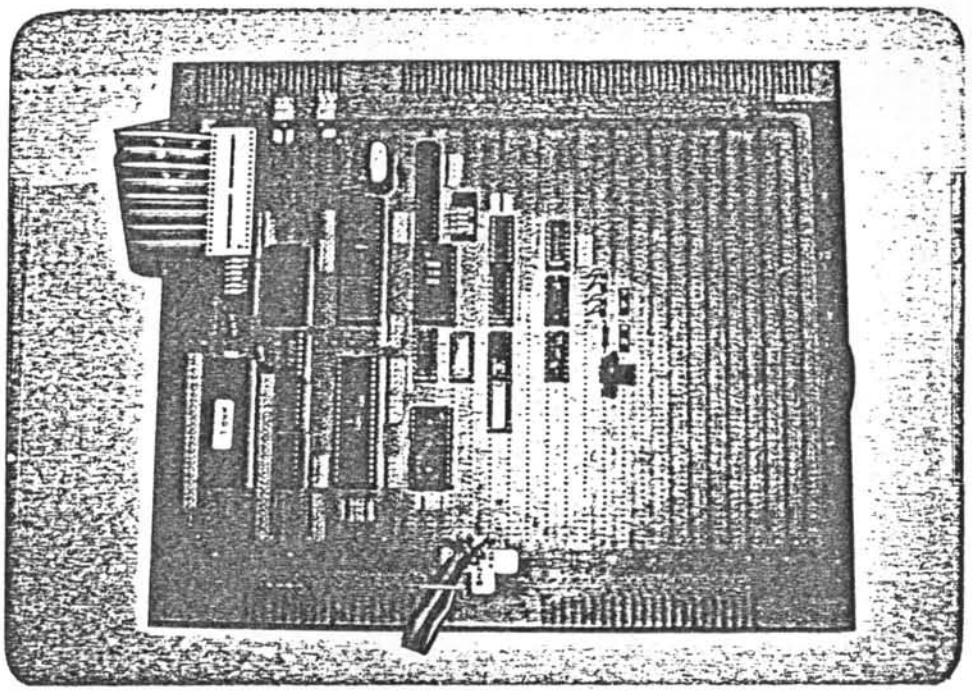
```
                        ;
                        ;       CURSOR  DOWN
                        ;
01AF 114000     RDOWN   LXI     D,0040H
01B2 78                 MOV     A,B
01B3 FE0F               CPI     0FH
01B5 CAC001             JZ      ROBIN
01B8 04                 INR     B
01B9 7D                 MOV     A,L
01BA 83                 ADD     E
01BB 6F                 MOV     L,A
01BC 7C                 MOV     A,H
01BD 8A                 ADC     D
01BE 67                 MOV     H,A
01BF C9         DORET   RET
01C0 CDCE01     ROBIN   CALL    ROLLUP
01C3 21C007             LXI     H,07C0H
01C6 79                 MOV     A,C
01C7 85                 ADD     L
01C8 6F                 MOV     L,A
01C9 060F               MVI     B,0FH
01CB C3BF01             JMP     DORET
                        ;
                        ;       SCROLL  MODE
                        ;
01CE 214004     ROLLUP  LXI     H,0440H
01D1 110004             LXI     D,0400H

01D4 7C         LOPUP   MOV     A,H
01D5 FE09               CPI     09H
01D7 CAE301             JZ      LOPRET
01DA 7E                 MOV     A,M
01DB EB                 XCHG
01DC 77                 MOV     M,A
01DD 23                 INX     H
01DE 13                 INX     D
01DF EB                 XCHG
01E0 C3D401             JMP     LOPUP
01E3 C9         LOPRET  RET
```

```
                        ;
                        ;       CLEAR  MEMORY
                        ;
01E4 210004     CLEAR   LXI     H,0400H
01E7 3E20       LOP     MVI     A,20H
01E9 77                 MOV     M,A
01EA 7C                 MOV     A,H
01EB FE0B               CPI     0BH
01ED CAF401             JZ      CMMH
01F0 23         CMML    INX     H
01F1 C3E701             JMP     LOP
01F4 7D         CMMH    MOV     A,L
01F5 FEFF               CPI     0FFH
01F7 CAFD01             JZ      BEGIN
01FA C3F001             JMP     CMML
01FD 210004     BEGIN   LXI     H,0400H
0200 010000             LXI     B,0000H
0203 C9                 RET
                        ;
                        ;       ENTER
                        ;
0204 7D         ENTER   MOV     A,L
0205 91                 SUB     C
0206 6F                 MOV     L,A
0207 0E00               MVI     C,00H
0209 CDAF01             CALL    RDOWN
020C C9                 RET
020D 7D         CRRT    MOV     A,L
020E 91                 SUB     C
020F 6F                 MOV     L,A
0210 0E00               MVI     C,00H
0212 C9                 RET
```

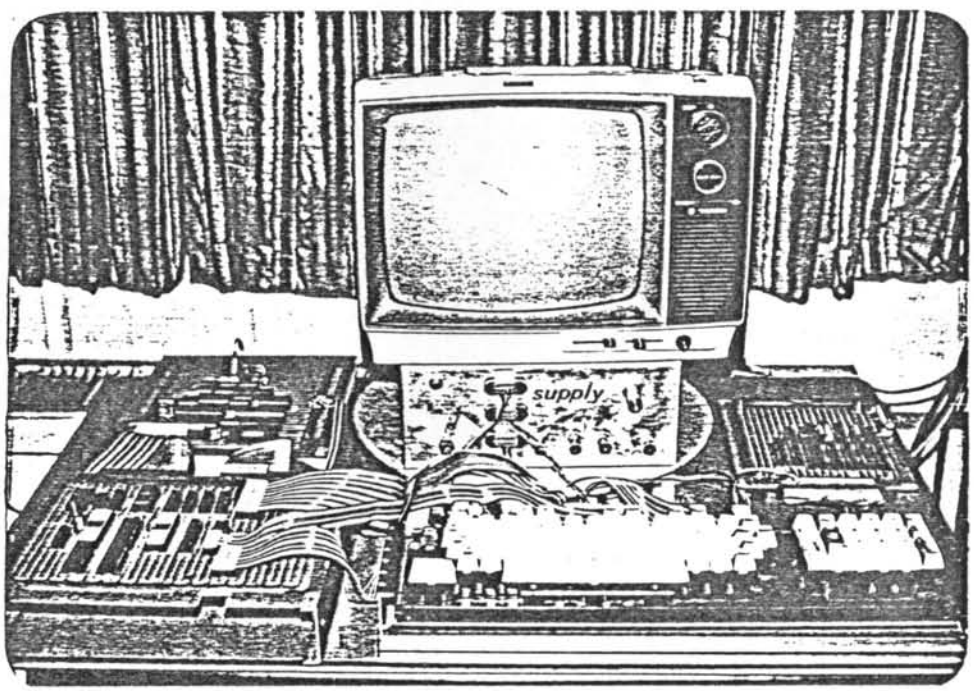
```
                        ;
                        ;       INTERRUPT  ROUTINE  "INITIAL  8257  DMA"
                        ;
0213 F5         INTSUM  PUSH    PSW
0214 DB91               IN      SUC
0216 3E00               MVI     A,00H
0218 D380               OUT     SUA
021A 3E04               MVI     A,04H
021C D380               OUT     SUA
021E 3E00               MVI     A,00H
0220 D381               OUT     SUT
0222 3E84               MVI     A,84H
0224 D381               OUT     SUT
0226 3E41               MVI     A,41H
0228 D388               OUT     SUS
022A 3E80               MVI     A,80H
022C D391               OUT     SUC
022E 79                 MOV     A,C
022F D390               OUT     SUP
0231 78                 MOV     A,B
0232 D390               OUT     SUP
0234 F1                 POP     PSW
0235 FB                 EI
0236 C9                 RET
                        ;
            023C C25002         JNZ     PPOUT   ; FULL
023F 3E04               MVI     A,04H   ; HALF SET RTS
0241 D3F6               OUT     PREG3
0243 DBF4               IN      PREG2
0245 E640               ANI     40H
0247 CA5002             JZ      PPOUT
024A DBF4       PCTS    IN      PREG2   ;CLEAR TO SEND
024C 17                 RAL
024D D24A02             JNC     PCTS
0250 DBF6       PPOUT   IN      PREG1
0252 E604               ANI     04H
0254 CA5002             JZ      PPOUT   ;NO
0257 F1                 POP     PSW
0258 D3F7               OUT     POUTP   ;SEND
025A F5                 PUSH    PSW
025B DBF4               IN      PREG2   ;FULL OR HALF
025D E608               ANI     08H
025F C26902             JNZ     RETN    ;FULL
0262 F1                 POP     PSW     ;HALF CHK
0263 FE0D               CPI     0DH
0265 CA6B02             JZ      HREST
0268 C9                 RET
0269 F1         RETN    POP     PSW
026A C9                 RET
026B DBF5       HREST   IN      PEOC    ;HALF RRESET
026D 17                 RAL
026E D26B02             JNC     HREST
0271 3E06               MVI     A,06H
0273 D3F6               OUT     PREG3
0275 C9                 RET
```

```
                        ;
                        ;       RECEIVE CHARACTER
                        ;
0276 DBF6               PIST    IN      PREG1
0278 1F                         RAR
0279 D0                         RNC
027A DBF7               PIIN    IN      PINP
027C E67F                       ANI     7FH
027E CD8402                     CALL    PCHA
0281 C37602                     JMP     PIST
                        ;
                        ;       CHARACTER INPUT CHECK
                        ;
0284 FE0D               PCHA    CPI     0DH
0286 C28F02                     JNZ     PLF
0289 CD0D02                     CALL    CRRT
028C C3AB02                     JMP     PRRT
028F FE0A               PLF     CPI     0AH
0291 C29A02                     JNZ     PBS
0294 CDAF01                     CALL    RDOWN
0297 C3AB02                     JMP     PRRT
029A FE08               PBS     CPI     08H
029C C2A502                     JNZ     PSAVE
029F CD5A01                     CALL    CLEFT
02A2 C3AB02                     JMP     PRRT
02A5 77                 PSAVE   MOV     M,A
02A6 D300                       OUT     ME0
02A8 CD8301                     CALL    CRITE
02AB C9                 PRRT    RET
0BFF =                  STACK   EQU     0BFFH
0000 =                  ME0     EQU     00H
0020 =                  ME1     EQU     20H
0060 =                  ME3     EQU     60H
0091 =                  SUC     EQU     91H
0090 =                  SUP     EQU     90H
0080 =                  SUA     EQU     80H
0081 =                  SUT     EQU     81H
0088 =                  SUS     EQU     88H
00F6 =                  PREG1   EQU     0F6H
00F4 =                  PREG2   EQU     0F4H
00F6 =                  PREG3   EQU     0F6H
00F4 =                  PREST   EQU     0F4H
00F5 =                  PBOUD   EQU     0F5H
00F5 =                  PEOC    EQU     0F5H
00F7 =                  PINP    EQU     0F7H
00F7 =                  POUTP   EQU     0F7H
02AC                            END
```

ภาคผนวก ค. ภาพถ่าย



ภาพถ่ายวงจรแสดงผลตัวอักษรที่สร้างเสร็จแล้ว



ภาพถ่ายวงจรแสดงผลที่ประกอบเข้ากับส่วนควบคุมและส่วนรับส่งข้อมูล

ประวัติผู้เขียน

นาย สำนวน หิรัญวงษ์ เกิดเมื่อวันที่ 4 เมษายน พ.ศ. 2495 ที่จังหวัดสุพรรณบุรี สำเร็จการศึกษาปริญญาครุศาสตรอุตสาหกรรมบัณฑิต สาขาวิศวกรรมไฟฟ้า จากสถาบันเทคโนโลยีพระจอมเกล้า วิทยาเขตพระนครเหนือ เมื่อปี พ.ศ. 2520 ปัจจุบันรับราชการที่ภาควิชาวิศวกรรมคอมพิวเตอร์ คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย