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APPENDIX A

CALCULATIONS

A.1. High Voltage Power Supply

A.1.1. Inverter

Given $P_{out} = HV. \times I_{max} = 2.5 \times 10^{3} \times 200 \times 10^{-6}$

$= 0.5\ W$

$V_{in} = 6\ V$

$V_{out} = 650\ V$

$$P_{in} = \frac{P_{out}}{\eta} = \frac{0.5}{0.8} = 0.625\ W$$

$$I_C = \frac{P_{in}}{V_{in}} = \frac{0.625}{6} = 0.104\ A$$

$$I_O = \frac{P_{out}}{V_{out}} = \frac{0.5}{650} = 7.69 \times 10^{-4}\ A$$

Select TR MPSU06 for Q_5, Q_6

$h_{FEmin} = 30$

$$I_B = I_C = \frac{0.104}{30} = 3.46 \times 10^{-3}\ A$$

Since $$R_C + R_B = \frac{V_{CC} - V_{BE}}{I_B}$$

$$R_C + R_B = \frac{5 - 0.6}{3.46 \times 10^{-3}} = 1271.68\ \Omega$$

Choose R_9, $R_{10} = 220\ \Omega$

Then $R_5, R_6 = 1 \ k\Omega$

Select TR 2N3904 as Q_3, Q_4

$$h_{FE\ min} = 50$$

$$I_C = \frac{V_{CC}}{R_C} = \frac{5}{1 \times 10^3} = 5 \times 10^{-3} \ A$$

$$I_B = \frac{I_C}{h_{FE}} = \frac{5 \times 10^{-3}}{50} = 1 \times 10^{-4} \ A$$

Since $R_c + R_b = \dfrac{V_{CC} - V_{BE}}{I_B}$

$$= \frac{5 - 0.6}{1 \times 10^{-4}} = 44000 \ \Omega$$

Choose $R_7, R_8 = 39 \ k\Omega$

Then $R_1, R_2 = 10 \ k\Omega$

Select ferrite core TDK.P2616 H5B. pot core, which is characterized by $A_{core} = 0.95 \ cm^2$, 80 % of $B_{sat} = 3500$ gauss.

From $N_p = \dfrac{V_{dc} \times 10^8}{4fBA_c}$

with given $V_{dc} = 6$ V. and frequency 5 kHz

$$N_p = \frac{6 \times 10^8}{4 \times 5 \times 10^3 \times 3500 \times 0.9}$$

$$= 9 \text{ turns}$$

Therefore, the transformer primary turns is 18 turns center-tap.

and $\dfrac{N_p}{N_s} = \dfrac{V_p}{V_s}$

$$N_s = \frac{N_p}{V_p} \times V_s$$

$$= \frac{9 \times 650}{6} = 975 \text{ turns}$$

The scondary turns is 975 turns

Select the wire size from the table

wire size of T_p = 34 SWG

wire size of T_s = 45 SWG

To keep the transistor Q_5, Q_6 saturate during the entire half cycle

$$C_4 = C_5 = \frac{T}{20R} = \frac{1}{20 \times 220 \times 5 \times 10^3} = 0.045\ \mu F$$

$$\approx 0.05\ \mu F$$

Given the power dissipation on clamp circuit = 0.05 P_{out} [7]

$$R_{11} = \frac{(2V_{in})^2}{0.05\ P_{out}} = \frac{(2 \times 6)^2}{0.05 \times 0.5} = 480\ \Omega$$

$$= 500\ \Omega$$

$$C_6 = \frac{20T}{R_{11}} = \frac{20}{5 \times 10^3 \times 500} = 8\ \mu F$$

A.1.2 Oscillator circuit

Select TR2N3904 with h_{FE} 50 as Q_1, Q_2

$$I_C = \frac{V_{CC}}{R_C} = \frac{5}{10 \times 10^3} = 5 \times 10^{-4}\ A$$

$$I_B = \frac{I_C}{h_{FE}} = \frac{5 \times 10^{-4}}{50} = 1 \times 10^{-5}\ A$$

$$R_b = \frac{V_{CC} - V_{BE}}{I_B} = \frac{5 - 0.6}{1 \times 10^{-5}} = 440\ k\Omega$$

Choose R_3, R_4 = 390 kΩ

For frequency 5kHz and 50% duty cycle

$$T = t_1 + t_2 = \frac{1}{f}$$

$$= 2 \times 0.693 \text{ RC}$$

$$C = \frac{1}{2 \times 0.693 \times 390 \times 10^3 \times 5 \times 10^3}$$

$$= 370 \text{ pF}$$

Choose $C_1, C_2 = 350$ pF

A.1.3 Regulator circuit

Given $V_o = 6$ V.

$$V_o = V_L - V_{BE}(Q_8) - V_{BE}(Q_7)$$

$$V_L = V_o + V_{BE}(Q_8) + V_{BE}(Q_7)$$

$$= 6 + 1.2 \simeq 8 \text{ V.}$$

From E_q 2.7, $V_L = V_R(1 + \frac{R_1}{R_2})$

When $R_2 >> R_1$

$$V_R \simeq V_L$$

Given $V_R = 9$ V.

Voltage reference adjust in range of $V_{BE}(Q_8) + V_{BE}(Q_7)$ to 9 V. i,e 1.2 V. - 9 V.

Choose $VR_1 = 10$ kΩ

$$R_{13} = \frac{VR_1 V_{R13}}{V_1 - V_{R13}}$$

$$= \frac{10 \times 10^3 \times 1.2}{9 - 1.2} = 1.54 \text{ k}\Omega$$

Choose $R_{13} = 1.5 \text{ k}\Omega$

$$V_{R17} \approx V_R$$

$$V_{R17} = \frac{V_{HV} R_{17}}{R_{17} + (R_{14} + R_{15} + R_{16})}$$

$$(R_{14} + R_{15} + R_{16}) = \frac{V_{HV} R_{17}}{V_{R17}} - R_{17}$$

$$= \frac{2.5 \times 10^3 \times 100 \times 10^3}{9} - 100 \times 10^3$$

$$= 27.68 \text{ M}\Omega$$

Choose $R_{14} = R_{15} = 10 \text{ M}\Omega$

$R_{16} = 6.8 \text{ M}\Omega$

A.1.4 Positive 9 V. power supply

$$I_{R22} = I_{z\,min} + I_L$$

Current I_L consumed at + 9 V. terminal is 0.05 A

$$I_{z\,min} = 0.2\, I_L = 0.01 \text{ A}$$

$$I_{R22} = 0.05 + 0.01 = 0.06 \text{ A}$$

$$R_{22} = \frac{V_{SUPP} - V_z}{I_{R22}} = \frac{12 - 9}{0.06} = 50\ \Omega$$

$$P_z = I_{z\,max} \times V_z = 0.54\ W$$

Select the zener 9 V.,1 W.

$$R_{22} = 50\Omega\ ,\ 1\ W$$

A.2 Amplifier Discriminator

A.2.1 Amplifier (IC_1, IC_2, IC_3)

Bias the noninverting input so that the output of operational amplifier operates at 2 V above ground level.

let $I_{R7} + R_8 = 100\ \mu A$

$$R_7 + R_8 = \frac{V_{CC}}{I} = \frac{5}{100 \times 10^{-6}} = 50\ k\Omega$$

$$V_{R8} = 2\ \text{volt}$$

$$R_8 = \frac{V_{R8} \times (R_7 + R_8)}{V_{CC}}$$

$$= \frac{2 \times 50 \times 10^3}{5} = 20\ k\Omega$$

$$R_7 = 50\ k\Omega - 20\ k\Omega = 30\ k\Omega$$

From Eq. 2,10 charge sensitive amplifier gain = $-\frac{C_i}{C_f}$

$$\frac{V_o}{V_i} = -\frac{C_i}{C_f}$$

Choose $C_3 = 1$ pF and $C_6 = 4.7$ pF (NPO.)

$$R_4 = 22\ M\Omega$$

From Eq 2.13 voltage gain of inverting amplifier $= -\frac{R_f}{R_{in}}$

Choose $R_{10} = R_{12} = 100\ k\Omega$

and $R_6 = R_{11} = 10\ k\Omega$

$$A_1 = -\frac{R_{10}}{R_6} = -\frac{100\ k\Omega}{10\ k\Omega} = -10$$

$$A_2 = -\frac{R_{12}}{R_{11}} = -\frac{100\ k\Omega}{10\ k\Omega} = -10$$

$$\text{cascade gain} = A_1 \times A_2 = 100$$

Overall gain of Amplifier can be adjusted by a trimpot or by a fixed resistor at R_f of IC_2

A.2.2 Discriminator (IC_4)

Bias level adjustable level from 0-2 V

Choose $VR_2 = 50\ k\Omega$

given $V_{R13} = V_{R14} = 1.5$ V.

$$R_{13} = R_{14} = \frac{VR_2 \cdot V_{R13}}{V_{R2}} = \frac{50K \times 1.5}{2} = 37.5\ k\Omega$$

Choose $R_{13} = R_{14} = 36\ k\Omega$

and pull up resistance $R_{15} = 10\ k\Omega$

A.3 Ratemeter and Low Voltage (LV) Power Supply

A.3.1 ratemeter

Time constant of meter circuit (τ_1) = $VR_6\ C_{10}$

at 0 to 90 % of final reading

$$\tau_1 = 2\ RC$$

$$= 2 \times 50 \times 10^3 \times 100 \times 10^{-6} = 10\ s$$

Pulse width of monostable multivibrator IC_{1c}, $IC_{1d} = \tau_2$

$$\tau_2 = 1.3\ RC$$

$$\tau_2 << \tau_1 \text{ (condition of ratemeter)}$$

given τ_2 in minimum range ($VR_5\ C_9$) $\frac{\tau_1}{10}$

$$\tau_2 \simeq 10\ ms$$

Choose $C_9 = 0.47\ \mu F$

$$VR_5 = \frac{\tau_2}{1.3C} = \frac{10 \times 10^{-3}}{1.3 \times 0.47 \times 10^{-6}}$$

$$= 16.37\ k\Omega$$

Choose $VR_5 = 22\ k\Omega$ for calibrated scale.

In the other ranges time constant decreses in step of ten then $C_8 = 0.047\ \mu F$

$C_7 = 0.0047\ \mu F$

$C_6 = 470\ pF$

with $VR_5 = VR_4 = VR_3 = VR_2 = 22\ k\Omega$

A.3.2 LV. Supply

Select LM 340 T-5, To-220 package three terminal voltage regulator which is characterized by

Io = 500 mA , unregulated input voltage maxinum 35 V.

In ac power supply full wave rectifier

Select D_1, D_2 1N 4001 with I_f 1 A_{max} and PIV 400 V.

$$V_{DC} = V_o + V_D$$

$$V_{rms} = \frac{V_{DC}}{\sqrt{2}} = \frac{12 + 0.6}{\sqrt{2}} = 9\ V.$$

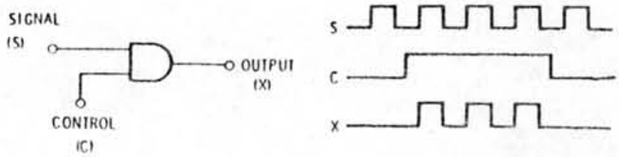
Secondary winding of transformer is 18 V. center-tap with I_L = 500 mA.

APPENDIX B

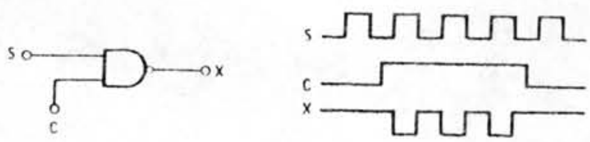
B.1 CMOS logic gates applications

In the circuits under digital control, a train of digital pulses may be wanted to turn on or off for some purposes. In one place this might occur at the input to a counting circuit, where we would like to count the number of pulses that happen in a period of time.

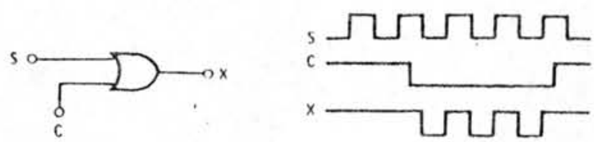
Fig. B.1 shows several ways to use CMOS as a simple switch.



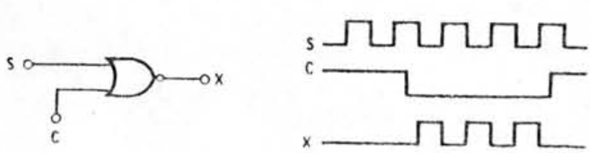
(A) AND gate



(B) NAND gate



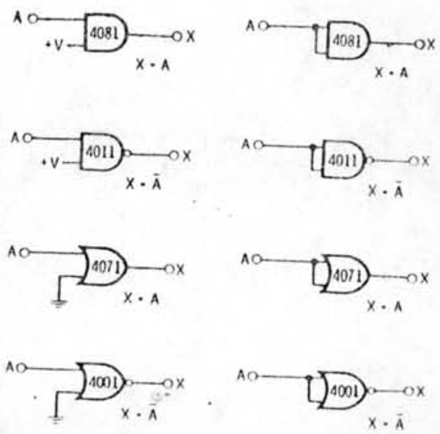
(C) OR gate



(D) NOR gate

All of the two-input gates can be converted to buffer or inverter.

Fig. B.2 shows how to use the two-input direct logic functions ; e.g. AND, NAND, OR, NOR, as inverter or buffer.



(A) AND gate (noninverting)

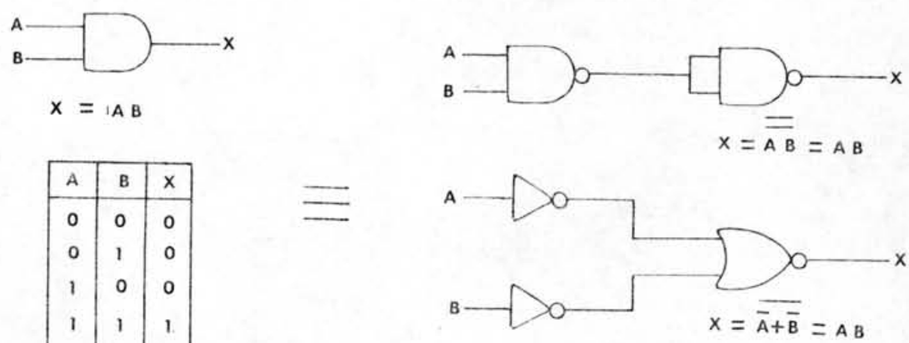
(B) NAND gate (invert)

(C) OR gate (noninverting)

(d) NOR gate (invert)

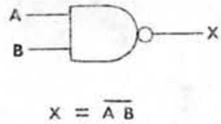
Fig. B.2 Converting multiple-input gates to inverters or buffers

In Fig. B.3 shows several ways to build an AND, OR, NOR and NAND gate by use of the remainder gate in circuit designed.



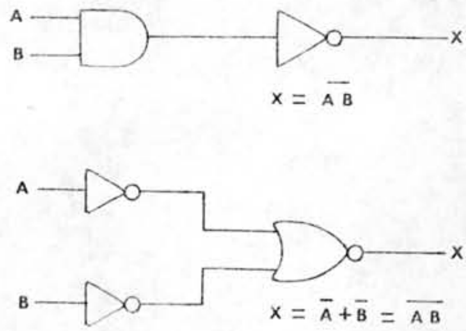
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

(A) The AND gate

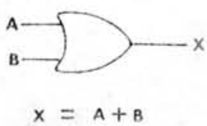


A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

≡

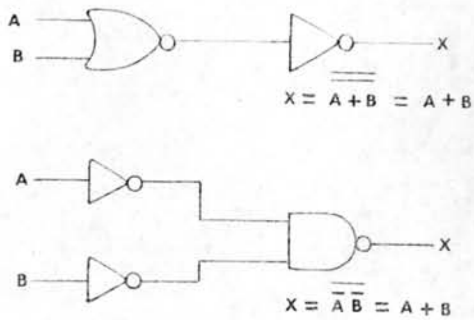


(B) The NAND gate

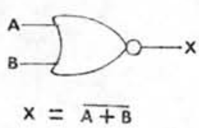


A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

≡

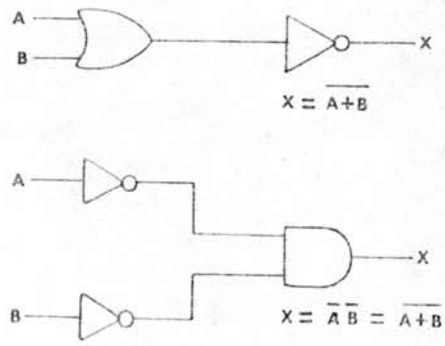


(C) The OR gate



A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

≡



(D) The NOR gate

Fig. B.3 Combination gates to other gate

B.2.2 Monostable multivibrators or One-shot circuits are built by cross-coupling feedback between two gates to hold the unstable state of Q in the interval of RC time constant, after being triggered by the set switch. This circuit is used for debouncing contact and time delay trigger.

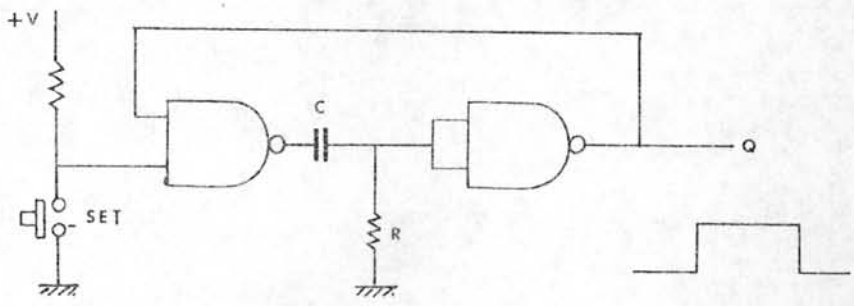


Fig. B.6 Monostable multivibrator built with NAND gates

B.2.3 Astable multivibrator circuits are built by conventional resistor-capacitor charging circuits. The cross-coupling feedback network between two inverter gates produces the automatic changing state in free running. The oscillator source is formed as shown in Fig. B.7

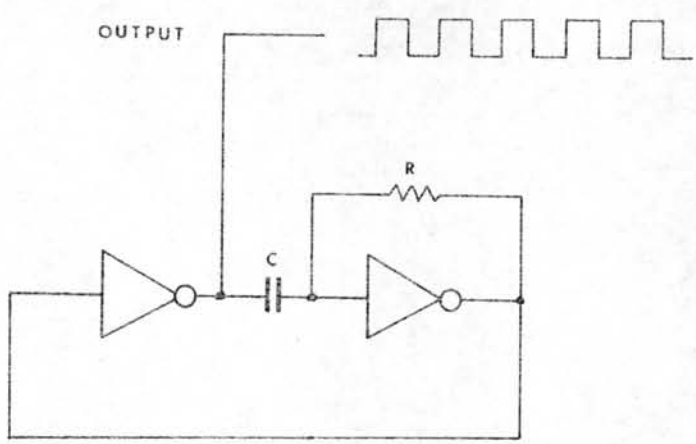
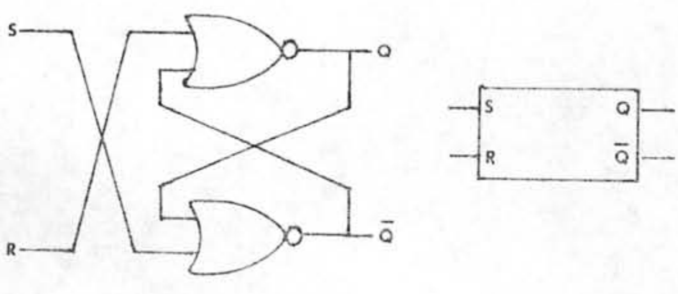


Fig. B.7 Astable multivibrator built with inverter gates

B.2 CMOS Multivibrators

The multivibrators are two states circuits. These circuits become two-stated by cross-coupled feedback between a pair of inverting gates or a pair of inverters. The circuit has monostable state, bistable state and nonstable state or astatble state, depending on the feedback component.

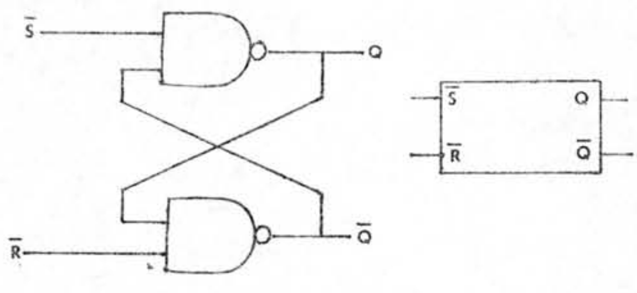
B.2.1 Bistable multivibrators or Flip-Flop circuits are built by symmetry eross-coupling at the input of the two gates. Fig. B.4 and B.5 show the simplest flip-flop which is useful for latch-condition of Q and $\bar{Q}$ in the circuit design.



S	R	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$
0	1	0	1
1	0	1	0
1	1	0	0
		disallowed	

(a) circuit (b) symbol (c) truth table

Fig. B.4 Set-reset flip-flop built with NOR gates



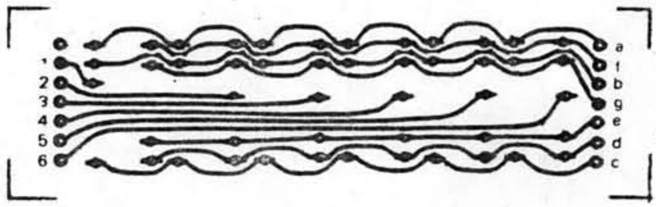
$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$
0	0	1	1
		disallowed	
0	1	1	0
1	0	0	1
1	1	Q	$\bar{Q}$

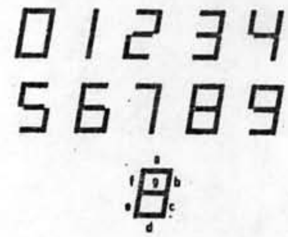
(a) circuit (b) symbol (c) truth table

Fig. B.5 Set reset flip-flop built with NAND gates

APPENDIX C

PRINTED CIRCUIT LAYOUTS

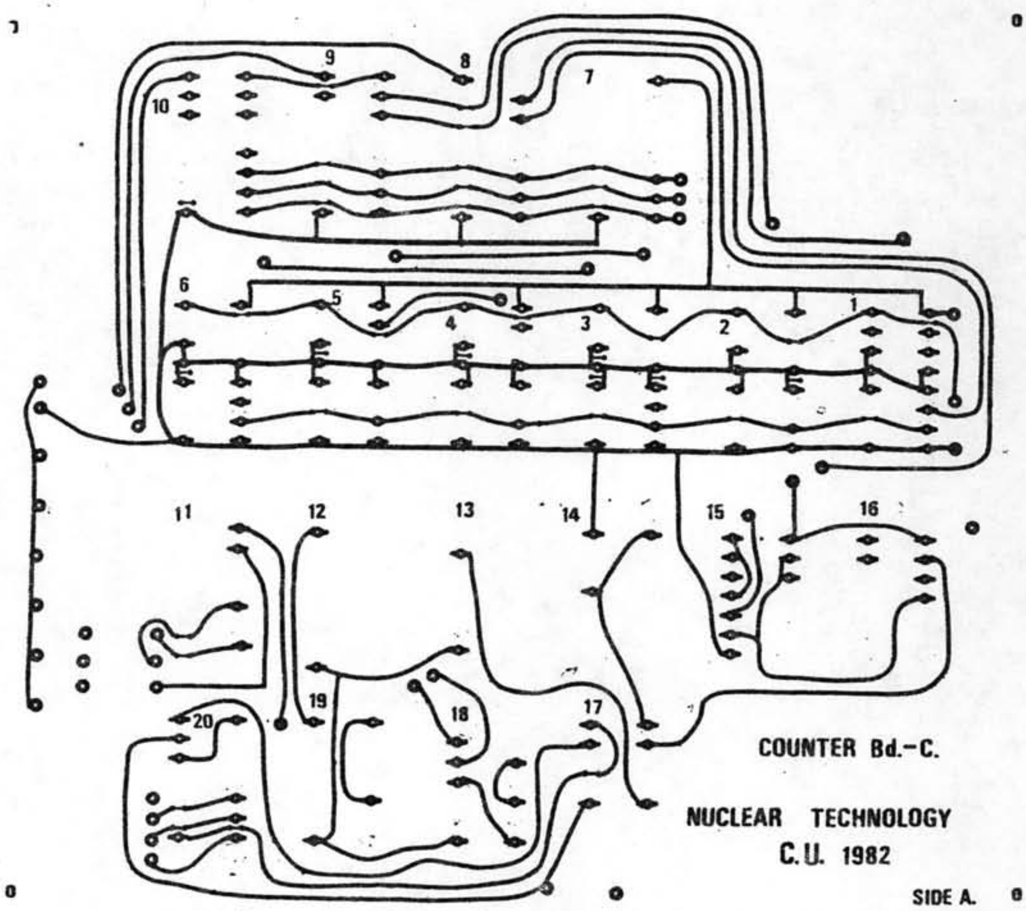




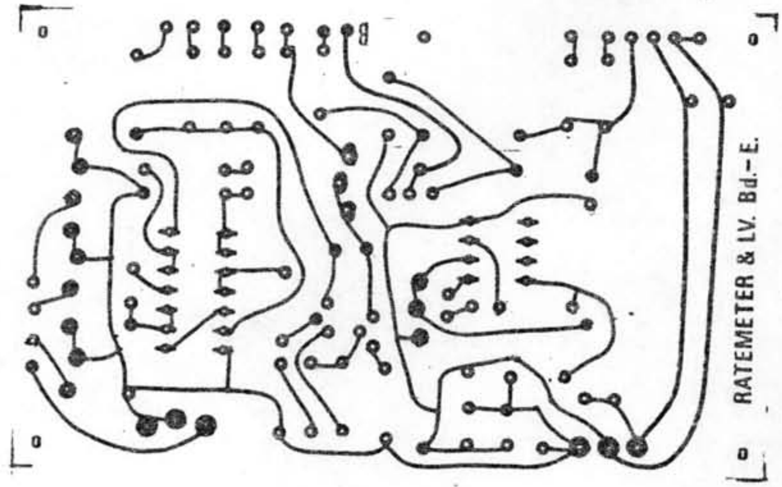
DISPLAY BOARD

SEGMENT

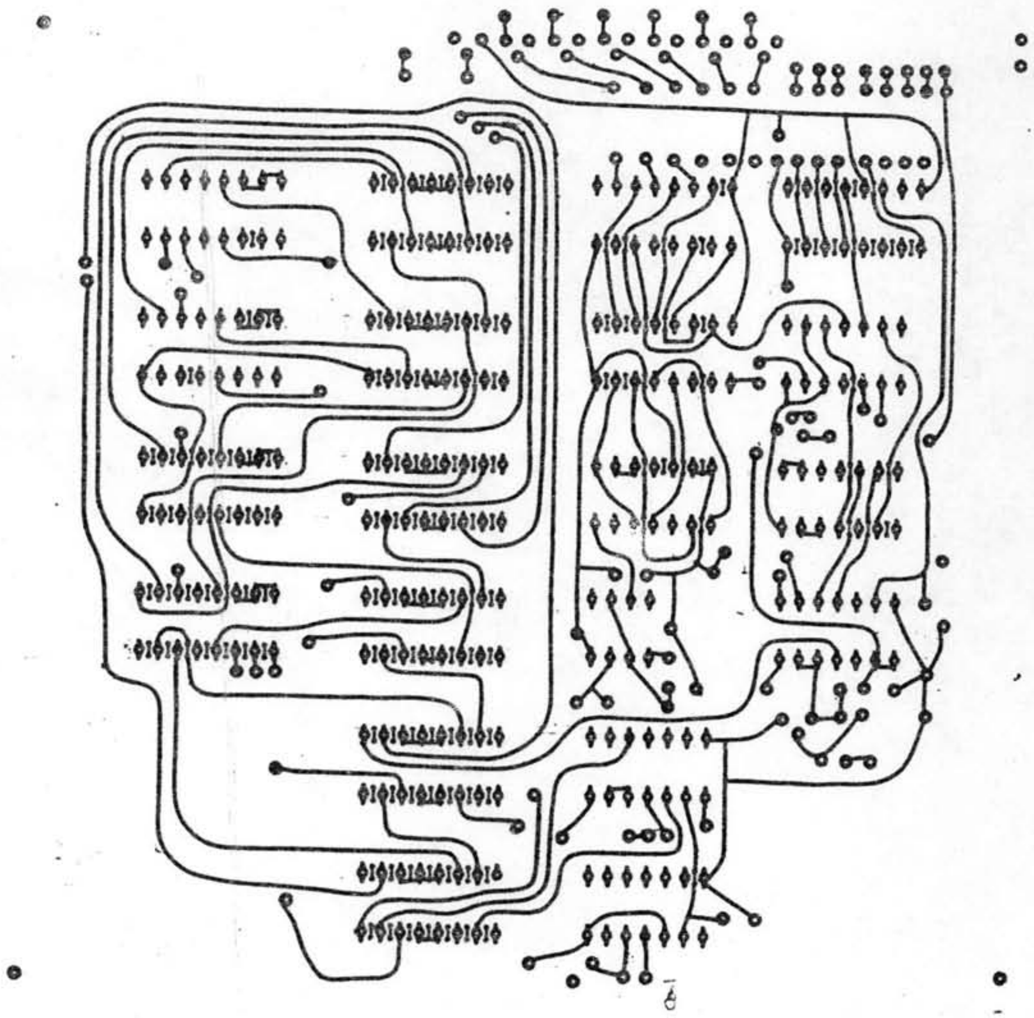
IDENTIFICATION



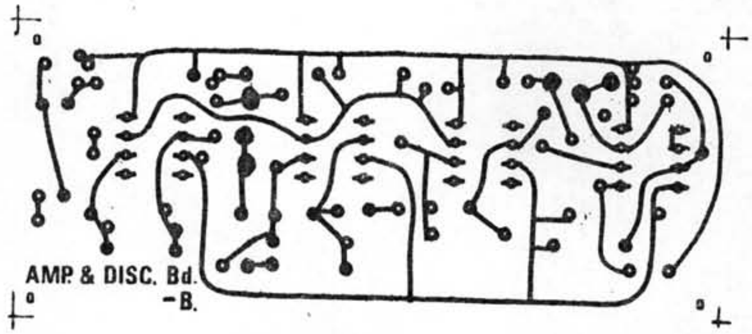
COUNTER BOARD SIDE. A



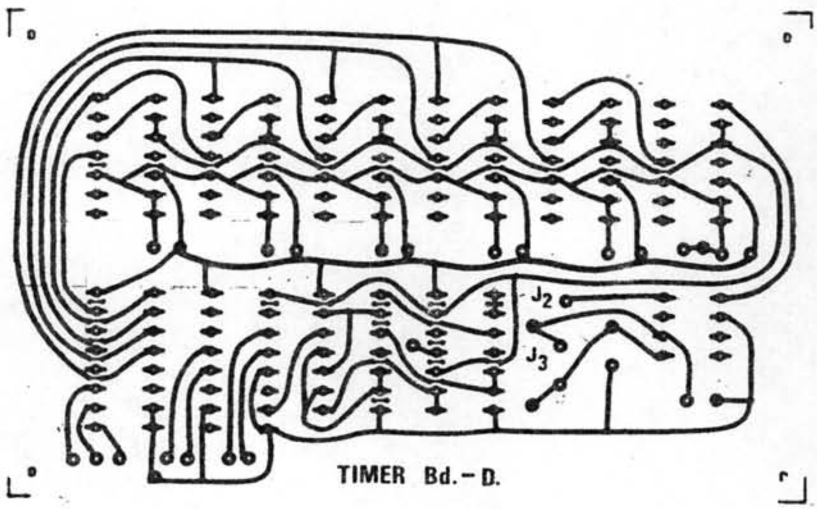
RATEMETER & LOW VOLTAGE BOARD



COUNTER BOARD SIDE B

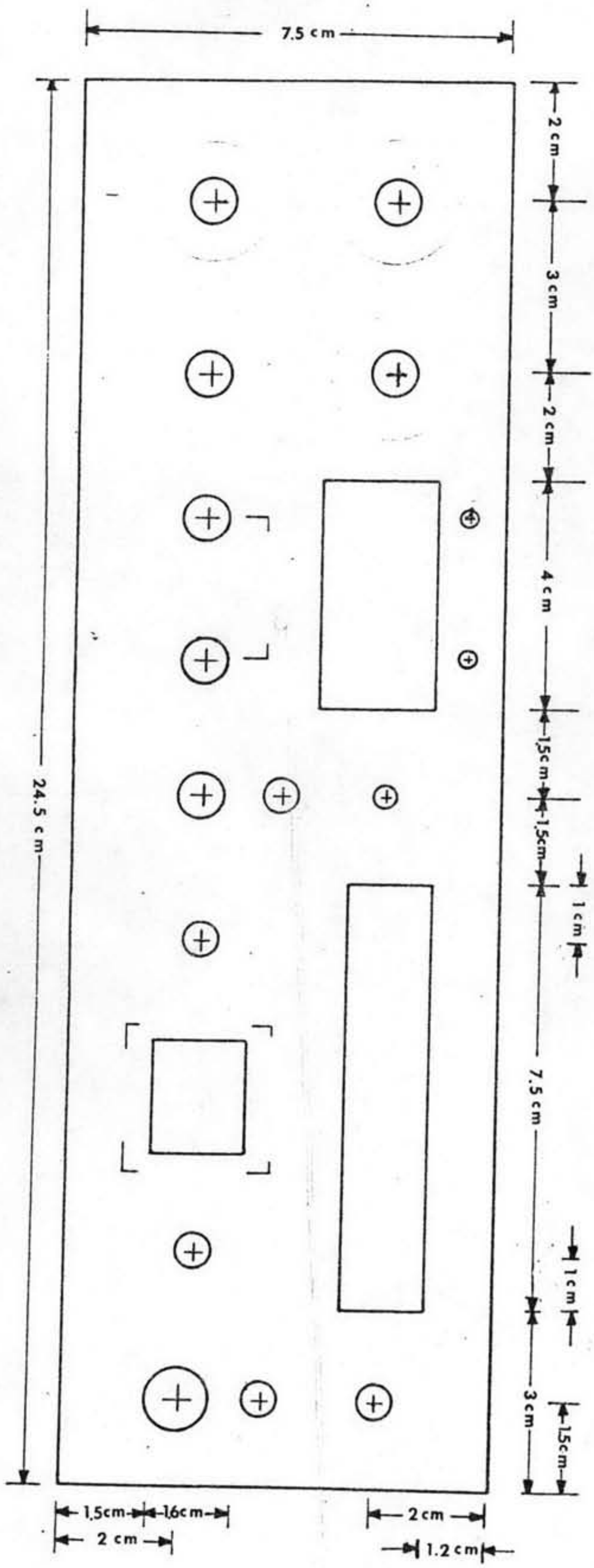


AMPLIFIER & DISCRIMINATOR BOARD

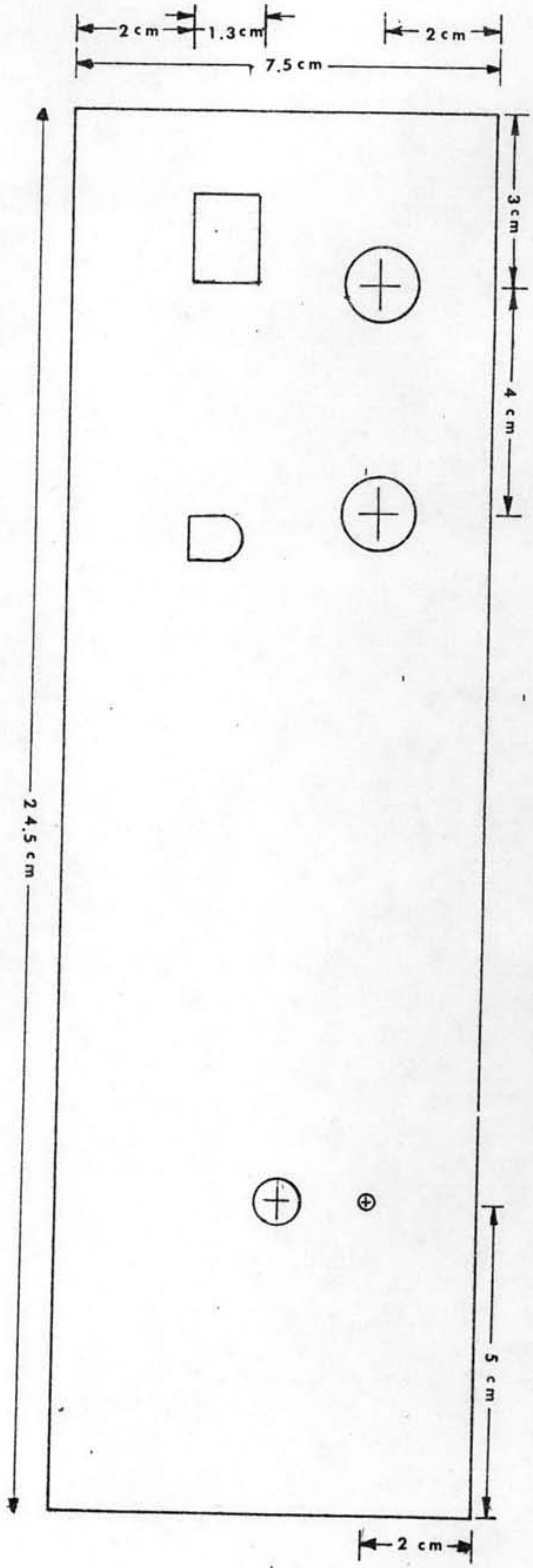


TIMER BOARD

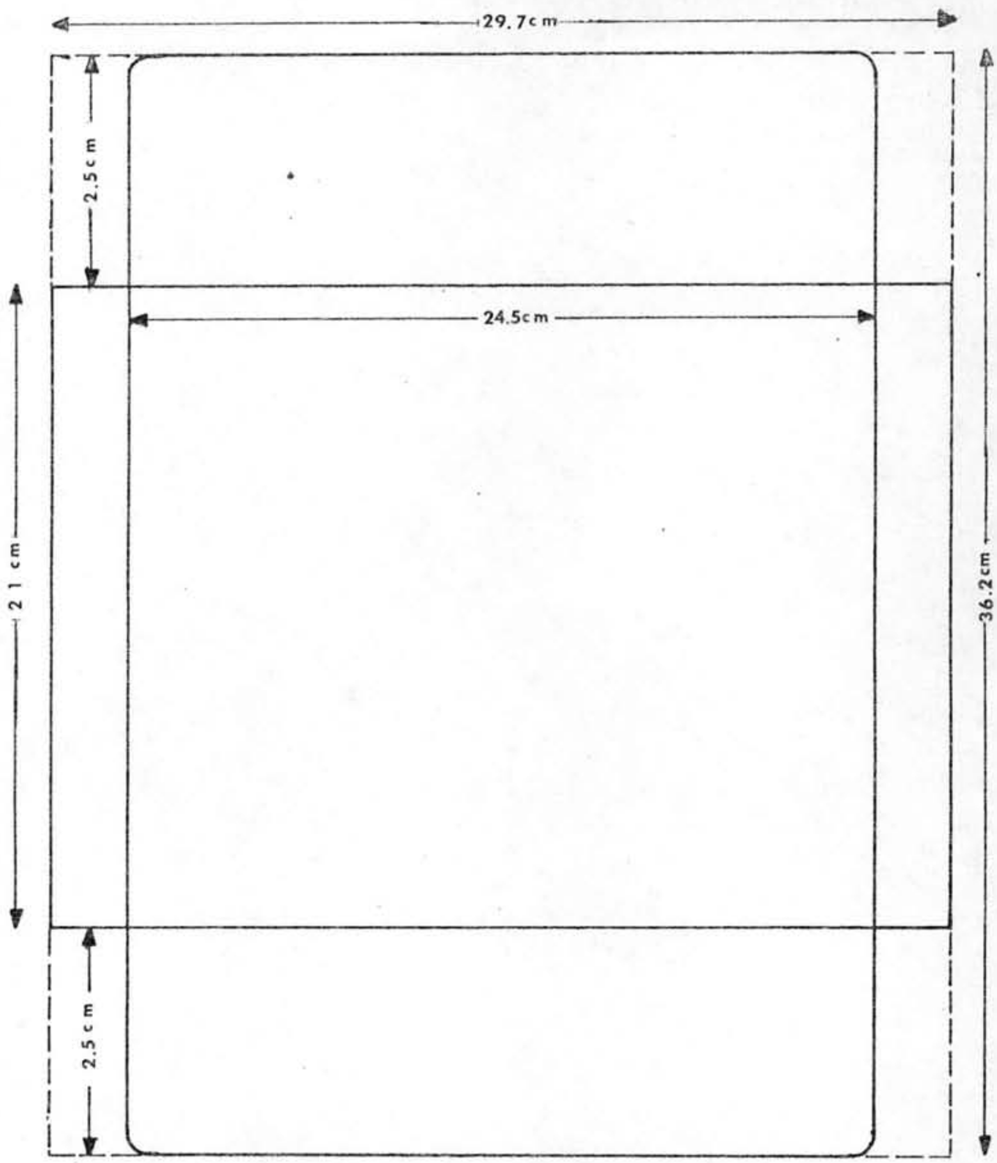
HIGH VOLTAGE BOARD



FRONT PANEL LAYOUT



REAR PANEL LAYOUT



CHASSIS LAYOUT

BIOGRAPHY

Mr. Suvit Punnachaiya was born on August 29, 1954 in Chonburi, Thailand. He received a Bachelor of Science in Technological Education, major in Electrical Technology - Communication from the Institute of Technology and Vocational Education in 1977. In the same year he worked at the Department of Nuclear Technology, Faculty of Engineering, Chulalongkorn University and continued his study towards the degree of Master of Engineering in Nuclear Technology at the same place in 1980. He is now working as teaching staff in the Department of Nuclear Technology, Faculty of Engineering, Chulalongkorn University.