CHAPTER 4

CIRCUIT OPERATION

4.1 General

The high voltage power supply develops high voltage for the detector. When radiation reacts in the detector, a negative pulse is generated. The pulses are coupled into the ampliflier and amplified. Pulses from the amplifier of sufficient magnitude pass through the discriminator controlled by front panel controls. They are then applied to ratemeter circuit and to a gate which is controlled either manually or by the timer before being counted by the decade counters.

The timer use crystal controlled oscillator as time base. Preset time can be selected for counting by use of two thumbwheel switches. The decade scaler has two modes of operation i,e additive or subtractive data counting. In the ADD. position, each coming pulse adds to exiting data in scaler, and in the SUB position, each coming pulse subtracts from previous data contained in the scaler after the end of counting period. This mode of operation enables background subtraction to obtain net count of data.

4.2 High voltage power supply circuit (Fig. 4.1)

The high voltage power supply circuit makes use of AC-DC driven type converter. Transistor Q_1 and Q_2 are connected as astable multivibrator which oscillates at 5 kHz. Its outputs are fed to drive the push pull

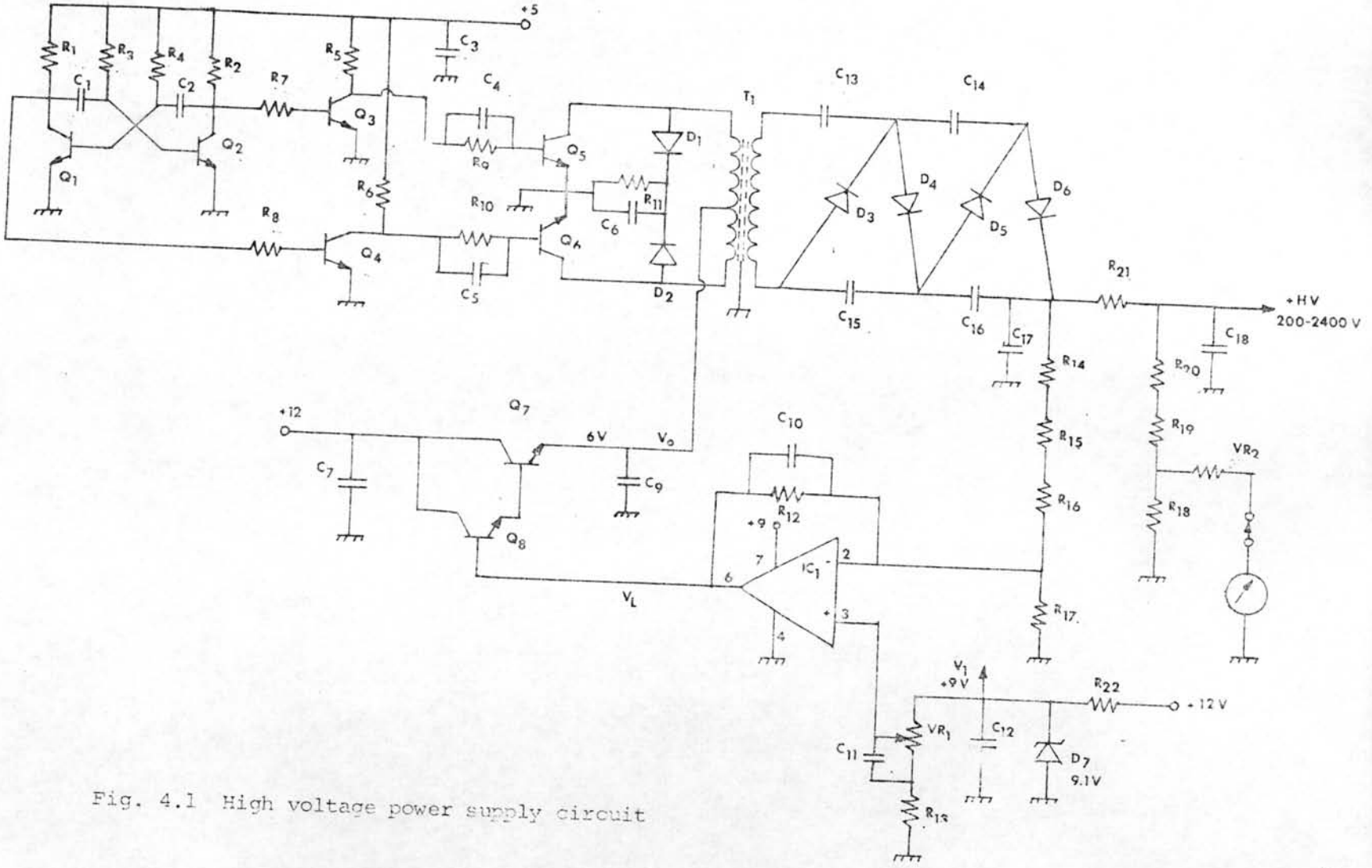

Fig. 4.1 High voltage power supply circuit

transistor Q_5 and Q_6 by passing through buffer transistor Q_3 and Q_4. High voltage transformer T_1 step up the low voltage square wave to higher one. This high voltage at secondary winding is multiplied four folds by quadruper voltage multiplier which consists of D_3-D_6 and C_{13}-C_{16} the filter C_{17} reduces the voltage ripple from loading. One part of the high voltage output is fed to the comparator to be compared with the reference voltage at voltage regulator circuit through the network R_{14}, R_{15}, R_{16} and R_{17}.

The voltage regulator consists of IC_1, Q_7, Q_8 and reference voltage network VR_1, R_{13}. This circuit is in balance when the voltages on the differential in put of IC_1 are equal. The high voltage is varied by varying the voltage on reference side with VR_1, HV. ADJUST. As the reference is increased the diferential in put of IC_1 in unbalanced causing the output voltage to increase. The increase in H.V. output continues until the voltage on R_{17} is equal to reference voltage. and restores the balance which in turns keep the H.V. output at a certain value.

When the high voltage is loaded this tends to lower the high voltage causing unbalance at the input of differential amplifier. This increases the level of high voltage until original value is attained. Fluctuation in ac power supply is also compensated by this voltage regulator.

4.3 Amplifier discriminalor (Fig 4.2)

4.3.1 Amplifier

Operational amplifier IC_1, C_6, C_3 and R_6 form a charge sensitive preamplifier whose output is proportional to the charge input from detector.

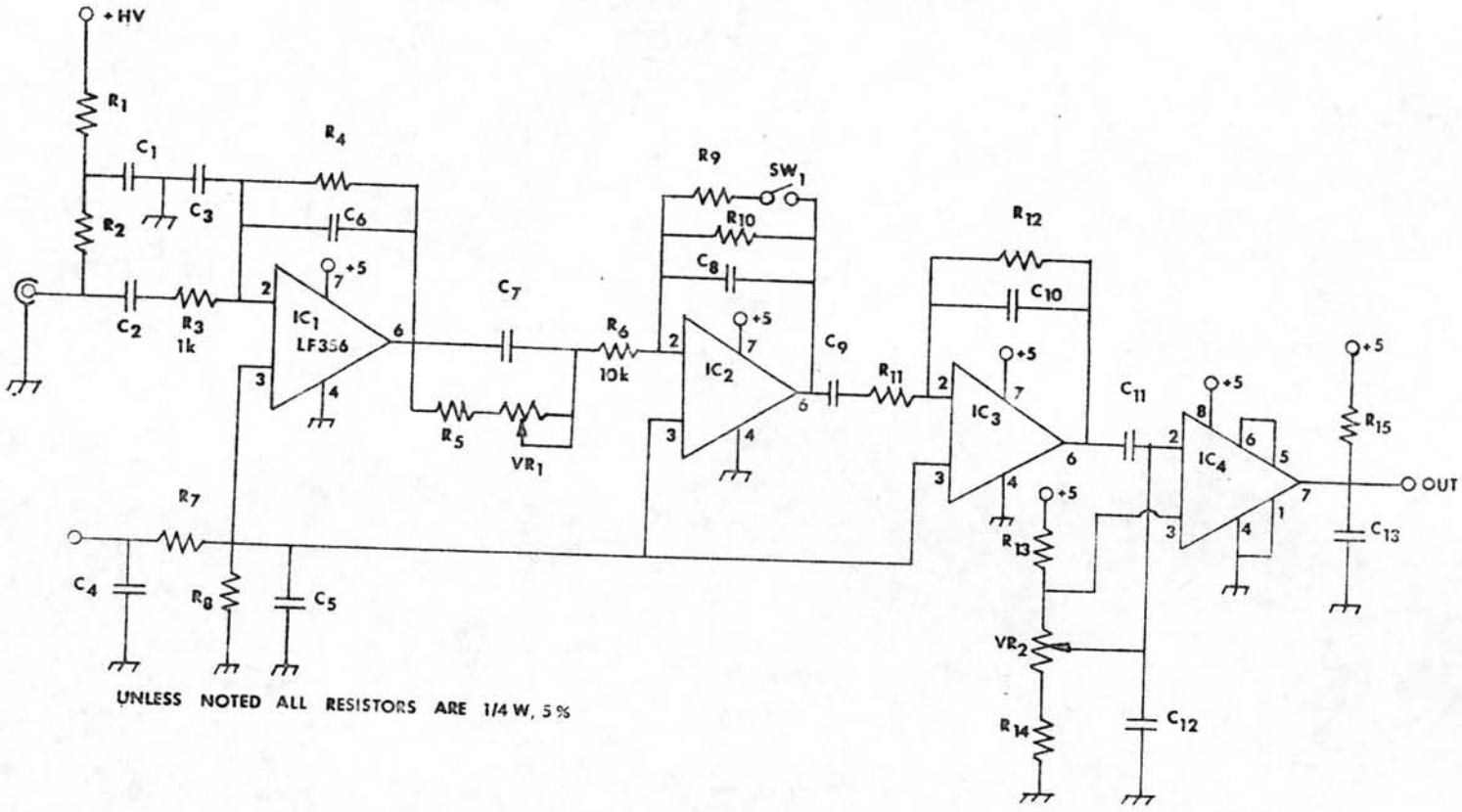

Fig. 4.2 Amplifier discrimator

The output pulse from pin 6 of IC_1 is fed to the cascade ac coupled amplifier where gain in amplitude and pulse shaping through feedback and coupling network working as differentiator/integrator network at IC_1 and IC_3 are attained. The voltage gain of IC_1 and IC_2 are determined by $-R_{10}/R_8$ and $-R_{12}/R_{11}$ respectively. The voltage gain of IC_1 can be reduced by switch on SW_1 to replace R_9 with R_{10}. The network R_4 and R_5 provides the op-amp bias for operation at 2/3 V_{CC} from a single end supply. The pole zero network C_7, R_7 and VR_1 acts to compensate the undershoot of output pulse from preamplifier.

4.3.2 Discriminator

The voltage comparator IC_3 is connected as discriminator. The discriminator level at control input (pin2, IC_3) can be adjusted through the network R_{13}, VR_2 and R_{14}, while the reference input (pin3, IC_3) is connected to fixed bias from the same network. An output pulse will occur only when input pulse from amplifier output exceeds the voltage difference between the reference side and the control side of the voltage comparator. This output pulse is logic output to drive the scaler and ratemeter circuits.

4.4 Scaler circuit

4.4.1 Up/Down decade counter (Fig 4.3)

Integrated circuit IC_1-IC_6 (CD40192) is connected in cacade forming six decade up/down counter. Counting up and counting down is performed by two count input, one being held at high state logic while

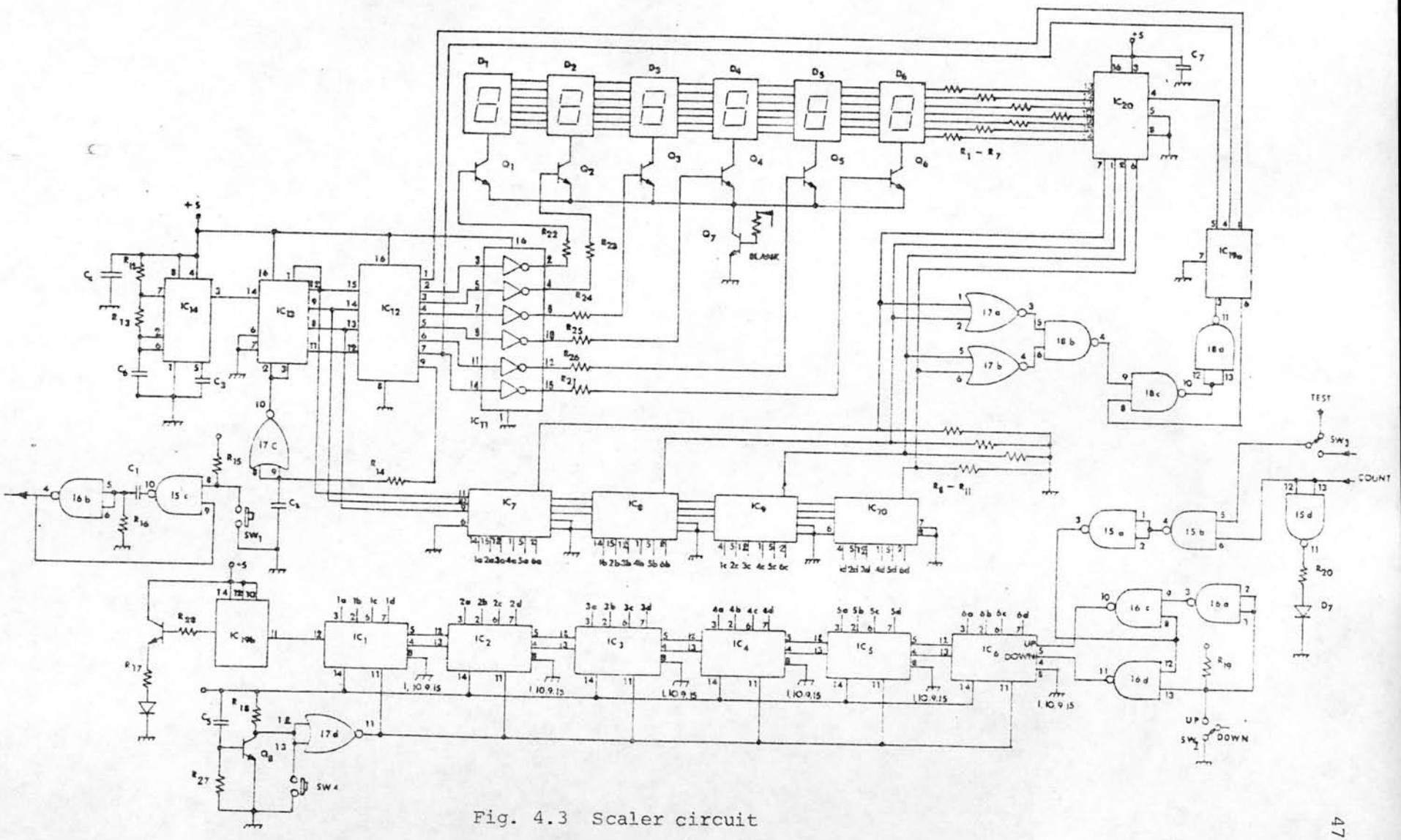

Fig. 4.3 Scaler circuit

the other is clocked. This condition is provide by the combination gates IC_{16a}, IC_{16c}, IC_{16d} and SW_2 (ADD-SUB switch). In count up, when the data content overflows, the overflow in dicator D_8 is lighted by carry output clocking the D-flip-flop. IC_{19b}. The transistor Q_8 and network R_{27}, C_5, R_{18} and inverter gate IC_{17d} are connected as an auto matic clearing device when power is first turned on. SW_4 is push butlon switch for clearing data of the counter.

Integrated circuit IC_{15a} and IC_{15b} form and AND gate to gate the signal to counter. If pin 6 (IC_{15b}) is low (stop condition), no signal is on pin 3 (IC_{15a}). If pin 6 (IC_{15b}), in high (counting condition), signal on pin 5 (IC_{15b}) is passed through to pin 3 (IC_{15a}), to decade counter. The counting indicator D_7 lights up on counting and becomes off when counting is stopped. The SW_3 is the test switch which selectes eiter the discriminator output or time base frequency (50Hz) for the scaler and ratemeter. SW_1 is the start timer switch IC_{16b} and IC_{15c} are connected as monostable multivibrator to debounce contact switch SW_1. Its output controls pin 8 (IC_{10c}) at timer board.

4.4.2 Multiplexing displays

The common cathode seven segment light emitting diodes D_1-D_6 form decimal display. The BCD code from counter is decoded to seven segment code by IC_{20}. By using the technique of multiplexing the decoder is reduced to single chip. Each digit display is scanned synchronizingly both the digit and BCD data. In this circuit IC_7-IC_{10} are BCD data selector, and IC_{12} is digit selector, both selectors are synchronized with the same scanner whose BCD scanner code is produced by rotary count

up of IC_{13} which is rotary cleared by IC_{17c}. The clock input of IC_{13} pin14 is the 1 kHz frequency which is generated by IC_{14} pin3 and its RC network. IC_{11} is hex-buffer digit drive between output of IC_{12} and input of Q_1-Q_6, and transistor Q_7 acts as blanking switch controlled by the timer output. The leading zero circuit comprises IC_{19a}, $IC_{17a,b}$, $IC_{18b,c,d}$. The integrated circuit IC_{17a}, IC_{17b}, IC_{18b}, IC_{18c} and IC_{18d} form combination gate to check the zero code of BCD data of each counter, and IC_{19a} is a D-flip-flop to generate the blanking control output (B1) at Q output (pin5 IC_{19a}) and fed to pin4 IC_{20}. This operation is discribed in 2.2.4 and simplified circuit diagram of leading-zero blanking is shown in Fig 2.19.

4.5 Ratemeter and low voltage supply circuits(Fig 4.4)

4.5.1 Ratemeter circuit

Integrated circuit IC_1 is connected to operate as a monostatole multivibrator which is triggered by IC_{1a}, IC_{1b} and R_b, C_5. Pulse width of monostable output is controlled by the RC time constant between IC_{1c}, IC_{1d}(pin8 and 13). This time constant is estabished by the setting of the range switch SW_{1a}, SW_{1b} which selects a particular R and C. The calibration of the scale of readout meter can be done by varying the pulse width continously.

The transistor Q_2, Q_3 form meter driver circuit. The driver Q_3 is normally off so no current flows through the meter. When the trigger is on, Q_3 turn on and current flows. The amount of current is determined by the voltage on the base of Q_3 and R_{12}. The length of time that current

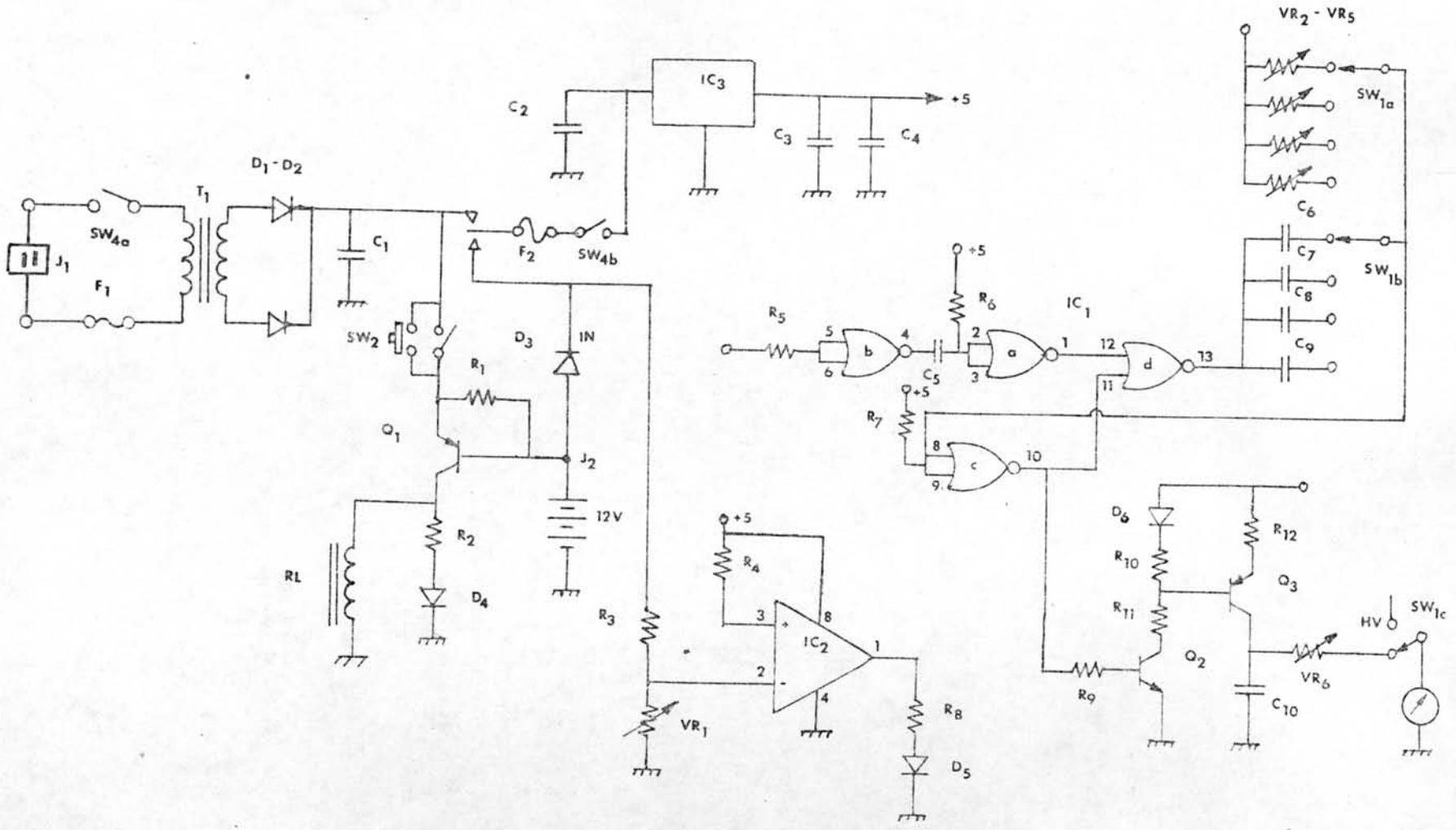

Fig. 4.4 Ratemeter and Low voltage power supply circuits

flows is determined by the pulse width of the triggering pulse from monostable output. This current generates a certain amount of charge which is transferred to C_{10} for each event counted. C_{10} discharges through the meter, yielding a certain average current dependent on the rate of input pulses. Changing the pulse width of the monostable by range switch also changes the average current for a given input pulse rate. This allows the meter to react in CPM from the discriminator.

The response time of the meter is controlled by the RC time constant of VR_6 and C_{10} the response control with VR_6 set to low resistance, the time constant is fast, and at high resistance it is slow.

4.5.2 Low voltage circuit

The ac line voltage is stepped down by T_1 rectified by D_1, D_2 and filtered by C_1. The three terminal voltage regulator IC_3 is a series regulator and supplies +5 volt to the circuitry. External connector J_2 is isolated by D_3 in order to prevent the damage in case of wrong polarity connection of battery. SW_3 is a self cutting switch of J_1. It connects the input supply to retifier circuit when ac line cord is plugged in and connects the input supply to battery source when ac line cord is plugged out. The low voltage battery indicator IC_2 is a voltage comparator. One of its input is connected to reference with 5 V supply, and the other to voltage devider network R_3 and VR_4 which is connected to battery output. The light emitting diode D_5 is lighted when the battery voltage is lower than 9.5 V. R_{13} is current limit resistor for battery charger. The switching transistor Q_1 is normally off and no charging current flows. When SW is pressed to charge the amount of charging current is produced Q_1 is on

turning on the relay and its contact is closed until the battery is fully charged and there is no current flowing through R_{13}, thus Q_1 is automatically cut off.

4.6 Timer

Integrated circuit IC_1 is programmable osciltator/divider. A precision osciltator is provided by interconnection of a 3.58 Hz quartz crystal and RC network (R_8, C_1, C_2) at pins 5 and 6 of IC_1. An internal pulse is divided by binary diver stages and generate 50 Hz output at pin 1 which forms a time base.

Integrated circuits IC_2 are connected as five count down counters reducing the frequency at IC_1 output (pin 1.) to 10 Hz IC_3, IC_4, IC_5, IC_6 and IC_7 are divide by ten counters. So the output 10^0, 10^1, 10^2, 10^3 and 10^4 are generated from 10 Hz output of the time base. The selection of IC_8 (1 of 8 data selector) is controlled by BCD thumbwheel switch. TH_1(M), for each BCD code (see Fig. 2.23). The selected pulse is fed to presettable decade count down IC_4 by passing through the combination gate IC_{11a} IC_{10a}, IC_{11b} to inhibit pulse at the input of IC_9 (pin 15) in absence of triggering. The presettable count down presets the data count down by BCD thumbwheel switch TH_2 (N) at the jams input. When count down goes to zero the carry in output (pin 7) will reset the R-S flip-flop IC_{10d} and IC_{10c}, changing the initial state. This changing state of flip-flop is controlled at IC_{10b}, and IC_{11d}. The output of IC_{11d} (pin 11) is in a high state during counting time interval and at a low state when counting is stopped. The output of IC_{10b} (pin 4) is in a low state during counting time interval to

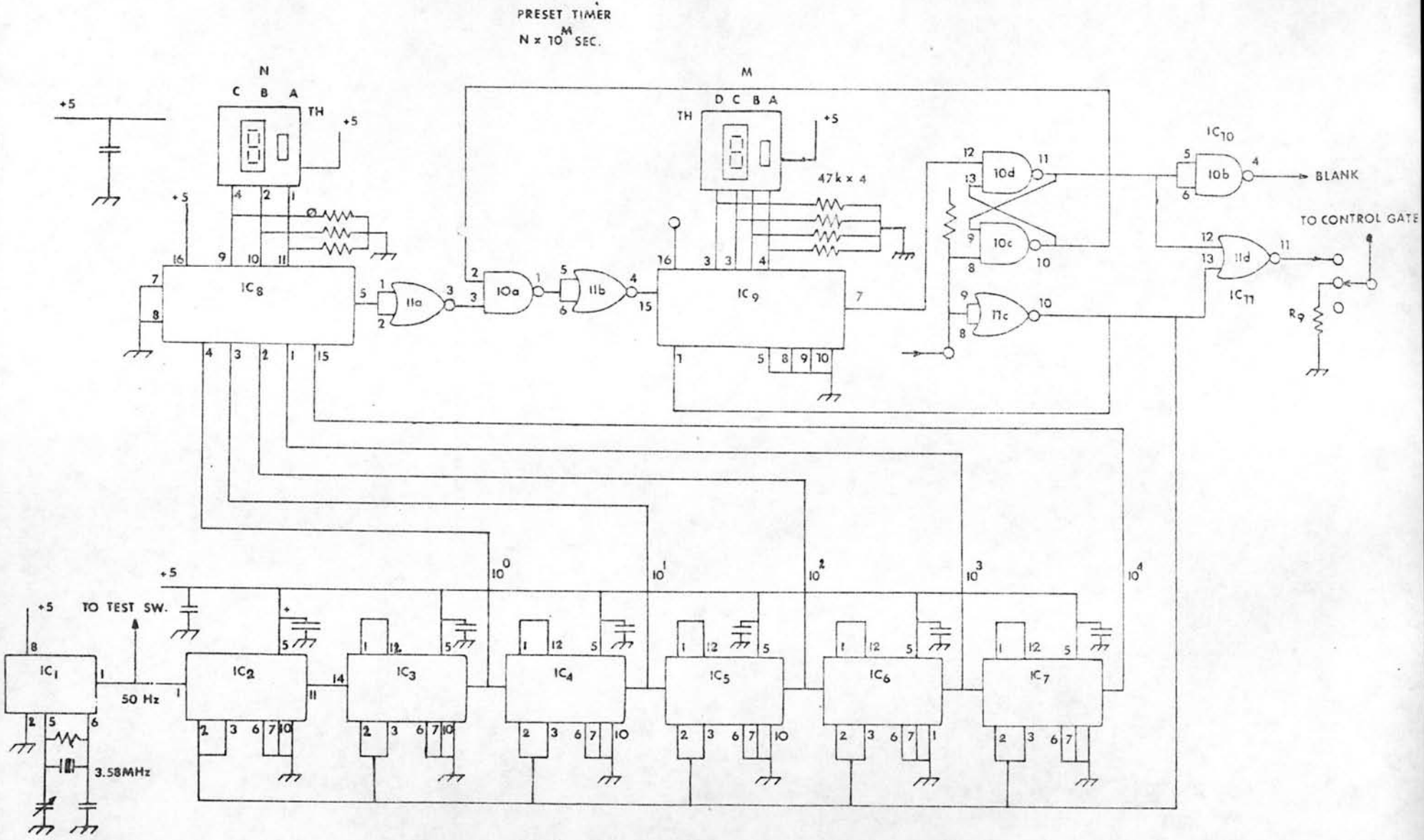

Fig. 4.5 Timer circuit

display blanking and at a high state during non-counting time in TIMED mode only. IC_{11c} is on inverter gate for clearing all counters in time circuit when the timer is started.

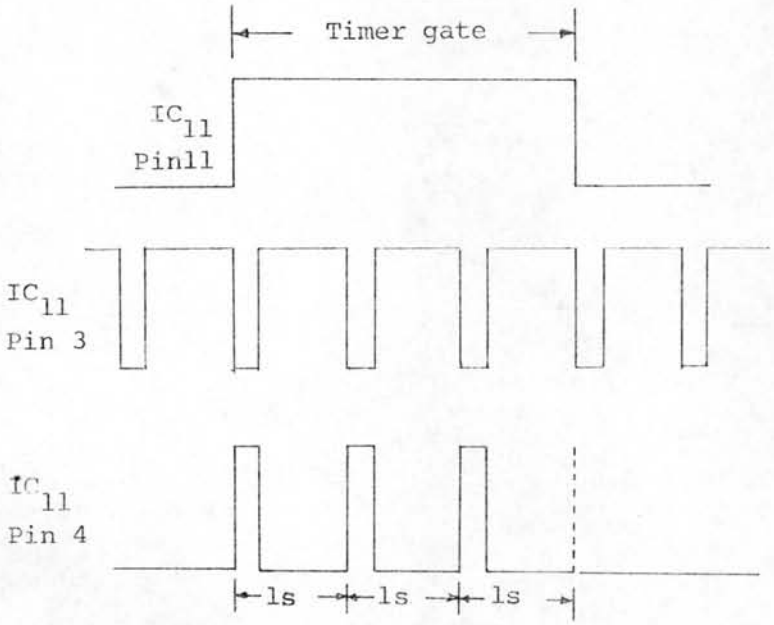

Fig. 4.6 Timing diagram of timer output preset time at 3×10^{0} sec.