CHAPTER 2

PORTABLE SCALER

Basically the portable scaler consists of : a variable high voltage power supply, discriminator amplifier, six decades scaler, linear ratemeter , presettable timer and low voltage power supply. The development of all electronic circuits is based on CMOS integrated circuits and the instrument is designed for use with practically any detectors ranging from scintillation, Geiger Mueller or proportional detectors. The block diagram with the signal chain is shown in Fig. 2.2

2.1 High voltage power supply

Most radiation detectors require a suitable high voltage for their proper operation. This voltage is conventionally called "detector bias", and high voltage power supply is used for this purpose. In Fig. 2.1 the high voltage power supply is subdivided into two parts : the DC-DC converter and voltage regulator.

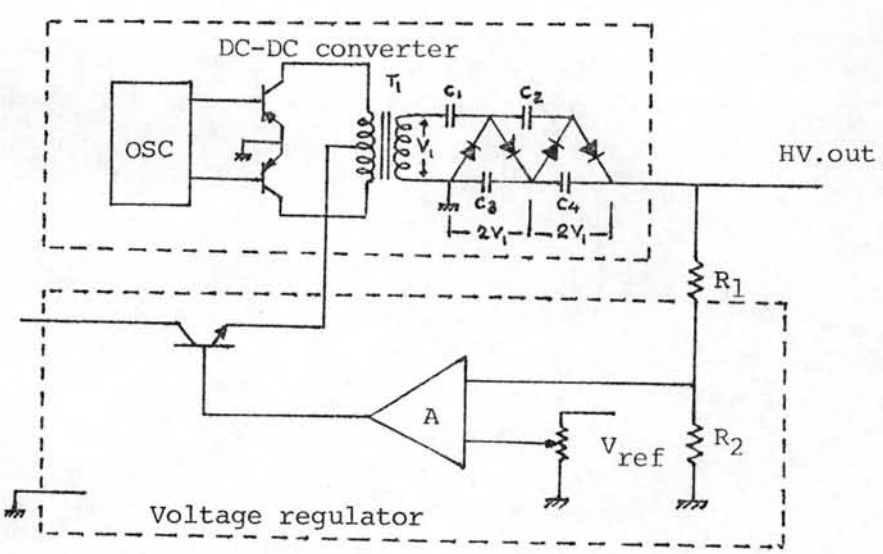


Fig. 2.1 High voltage power supply configuration

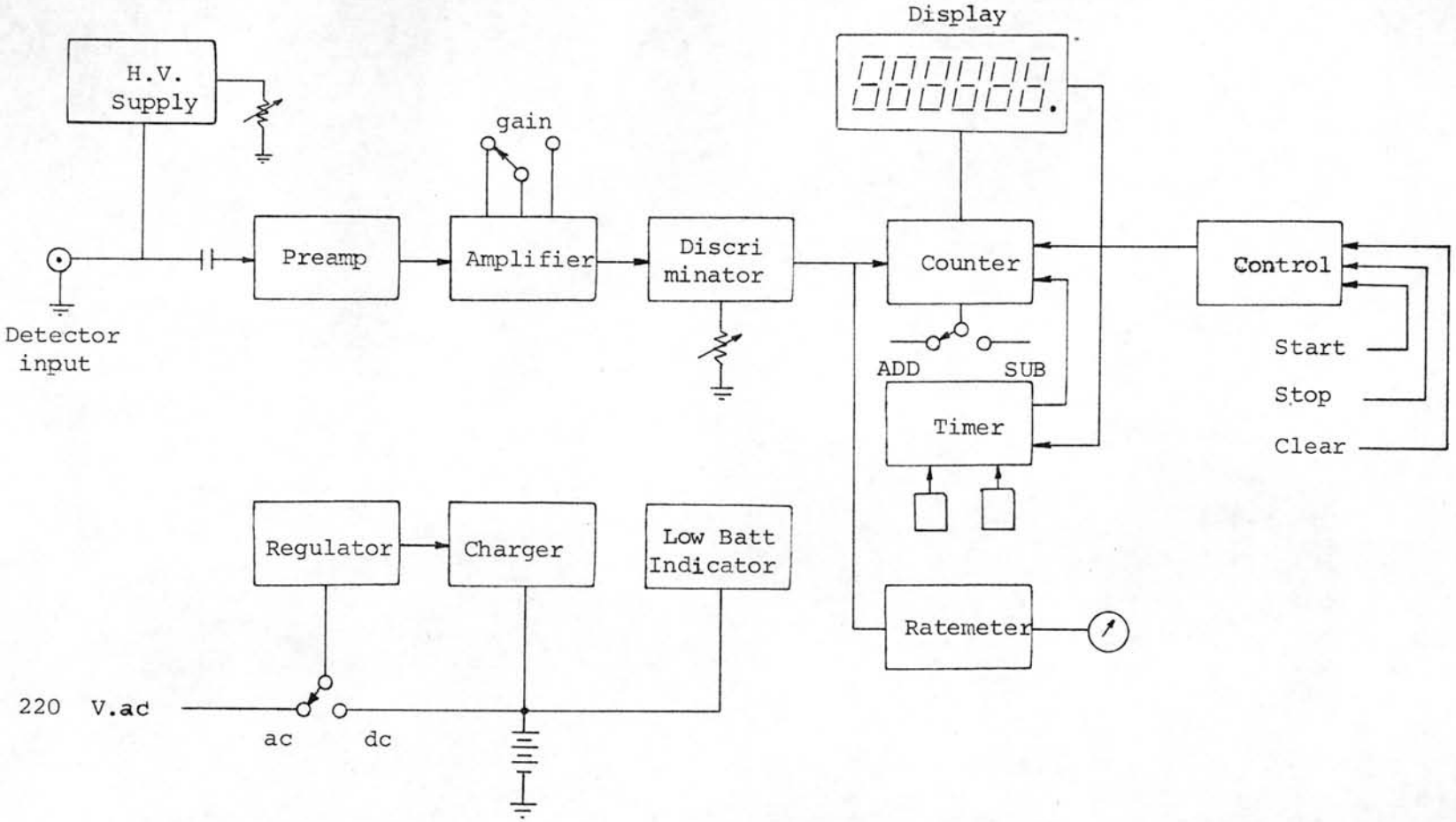


Fig. 2.2 Block diagram of a portable scaler

2.1.1 DC-DC Converter

The DC-DC converter is required in all portable electronic equipment where dc voltage level other than that from dc power source is required. In its basic form in Fig.2.2, DC-DC converter comprises a DC-AC driven type converter followed by a voltage multiplier.

In the DC-AC converter, a pair of push pull power transistor Q_1 and Q_2 operates in switching action. The base drives are alternated by the output of an astable multivibrator oscillator with frequency of 5 KHz which is found appropriate for the selected ferrite core of transformer T_1. This switching action i,e; Q_1 turns on and Q_2 turns off or vice versa, produces an a.c. voltage in primary winding T_p of transformer T_1, which in turn induces an ac square wave voltage on the secondary winding T_s. The magnitude of ac voltage may be changed by turn ratio of primary and secondary windings, according to the equation:

$$\frac{T_p}{T_s} = \frac{V_{in}}{V_{out}} \quad \text{.....2.1}$$

However, the induced voltage on secondary winding of converter transformer is limited by the insulation breakdown. So if higher voltage is required the voltage multiplier is essential. The voltage multiplier is convenient and efficient method to obtain the relatively high voltage. The cascade circuit of diodes and capacitors in Fig.2.1 gives a voltage quadrupler. In this circuit, capacitors are charged in parallel and discharge in series to produce $2V_{in}$ on C_3 and C_4, thus the output voltage is $4V_{in}$.

2.1.2 Voltage requlators

The output from DC-DC converter circuit will have ripple and a variable d.c. level, both being dependent on the load. Fluctuations and transients from the main supply will also be present. To obtain a stable supply with low output impedance, it is necessary to use a regulating servo system.[4]

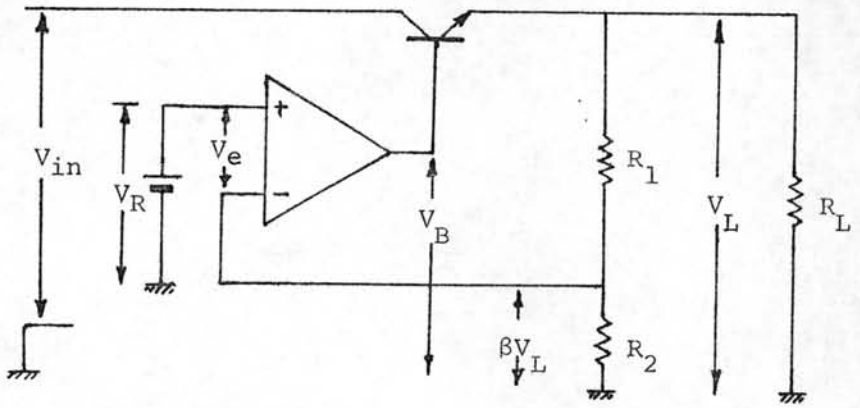


Fig. 2.3 Series requlator circuit schematic

The schematic of series voltage requlator is shown in Fig. 2.3. A series transistor between input (V_i) and output (V_L) is controlled by an amplifier, the in put of which is the difference between the requlator output and a fixed reference voltage (V_R). Any change in output is amplified to control the conductance of series transistor in the correct sense to counteract the initial change.

The unrequlated d.c. input voltage is at least a few volts higher than the output voltage across load terminals. This maintains the emitter follower in its active region enabling it to have a voltage gain very close to unity and low output resistance. Therefore

$$V_L \simeq V_B \quad \text{.....2.2}$$

and $$V_L = AV_e \quad \text{.....2.3}$$

but, $$V_e = V_R - \beta V_L$$

So $$V_L = A(V_R - \beta V_L) \quad \text{.....2.4}$$

where A is the voltage gain of the d.c. amplifier, V_e is the error signal, V_R is the reference voltage and β is the feedback factor given by

$$\beta = \frac{R_2}{R_1 + R_2} \quad \text{.....2.5}$$

From equation (2.4), it is seen that

$$V_L = \frac{V_R A}{1 + A\beta} \quad \text{.....2.6}$$

as A tends to large values

$$V_L \propto \frac{V_R}{\beta} \simeq V_R \frac{(R_1 + R_2)}{R_2}$$

$$= V_R \left(1 + \frac{R_1}{R_2}\right) \quad \text{.....2.7}$$

2.2 Amplifier discriminator

The fundamental output of all pulse type radiation detectors is a burst of charge (Q) which is liberated by the incident radiation. For gas filled and scintillation detectors, the voltage pulse is produced by integrating this charge pulses across the summed capacitance represented

by the detector, connecting cable, and input of the scaler circuitry. If the time constant of detector circuit is the parallel combination of C_D and R_t, then the voltage pulses will have amplitude equal to

$$V = - \frac{Q_D e^{-t/R_t C_D}}{C_D}$$

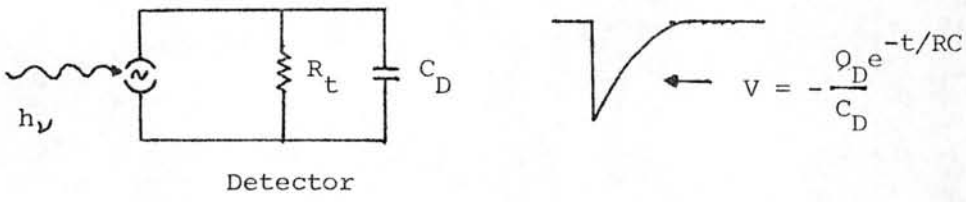


Fig. 2.4 The equivalent circuit of detector.

In most other detectors, however, the change is so small that it is impractical to deal with the signal pulses without an intermediate amplification. In order to count the pulse properly and discriminate noise signal, the pulses must be suppressed by bias level and converted into logic signal.

For this concept in the processing of pulses from radiation detectors the signal processing chain is therefore provided as in Fig.2.5

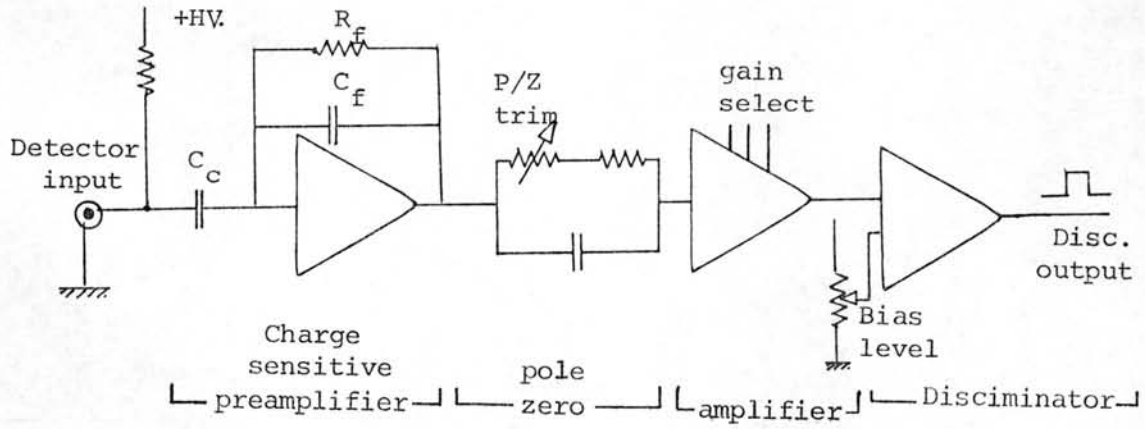


Fig. 2.5 Functional schematic of discrimirator amplifier

2.2.1 Charge sensitive preamplifier

A preamplifier is an amplifying element that is specifically designed to accept signal from a detector and to amplify that signal with minimum shaping in a way that will preserve signal to noise ratio. It also acts as impedance matching between detector and amplifier providing high input impedance while the output impedance is relatively low. Three basic types of preamplifiers that are normally used, are charge sensitive, voltage sensitive and current sensitive. The charge sensitive preamplifier is by far the most important type since its gain is highly stable and is independent on detector capacitance. Fig.2.6 shows a charge sensitive preamplifier configuration.[5]

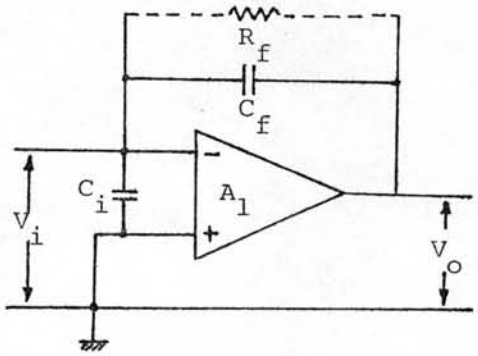


Fig. 2.6 Schematic diagram of a charge sensitive preamplifier

In terms of conventional operational amplifer theory [6], the function of A_1 in Fig. 2.6 is to provide a large voltage gain, low output impedance and high input impedance. C_f closes the loop as the feedback impedance Z_f and C_i acts as the source impedance Z_s. The voltage gain may then be calculated as

$$A_v = -\frac{V_o}{V_i} = -\frac{Z_f}{Z_s} \quad \text{.....2.8}$$

by putting $Z_f = \frac{1}{C_f}$, and $Z_s = \frac{1}{C_i}$

So, $$A_v = -\frac{C_i}{C_f} \quad \text{.....2.9}$$

and $$V_o = -\frac{V_i C_i}{C_f} = -\frac{Q_D}{C_f} \quad \text{.....2.10}$$

From equation 2.10, Q_D is the charge produced at detector by the energy of the incident radiation. The resistor R_f in Fig. 2.6 is required to discharge capacitor C_i and C_f. Without its presence these capacitors would build up a charge and run the operational amplifier into saturation. The decay rate of the tail of the output pulse is detemined by the time constant of $R_f C_f$.

2.2.2 Pole-zero cancellation

Pole-zero cancellation is a method for eliminating pulse undershoot after passing from CR network wave shaping in preamplifier. Because the output pulses from preamps have long decays (of the order of 50 μS), the undesirable undershoots persist for a long time when they are processed by successive RC differentiators. Fig. 2.7 (a) shows a pulse with undershoot.

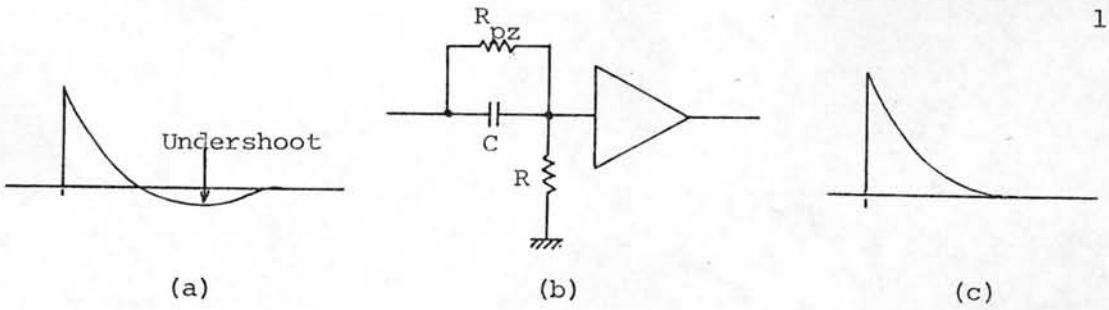


Fig. 2.7 Application of pole-zero cancellation.

This effect can be reduced by using pole-zero cancellation network as shown in Fig.2.7 (b). A resistance R_{pz} is added in paralle with the capacitor of the CR net work of input ampllfier to give a modified transfer function of the form

$$\frac{Sk\tau_1 (1 + S R_{pz} C_1)}{(1 + S\tau_2)(1 + Sk\tau_1)} \quad \text{.....2.11}$$

where $k \equiv \frac{\tau_2}{\tau_1 + \tau_2}$ τ_1 is time constant of preamps

τ_2 is time constant of CR differentiator

The value of R_{pz} is now adjusted such that

$$R_{pz} = \frac{\tau_2}{C_1} \quad \text{.....2.12}$$

In practice, a proper choice for the resistance value depends on the decay time of preamplifier.

2.2.3 Amplifier

The function of an amplifier is to provide, pulse shaping and amplitude gain. Most amplifiers in use today employ the passive pulse shaping methods for improvement in signal-to-noise ratios. At low counting rate, shaping pulse into unipolar from nearly "Semi-Gaussian"

is provided by differentiator /integrator CR-RC circuits as shown in Fig. 2.9

Fig. 2.8 shows configuration of amplifier sections and Fig. 2.9 illustrates the equivalent circuit of shaping network of the amplifier.

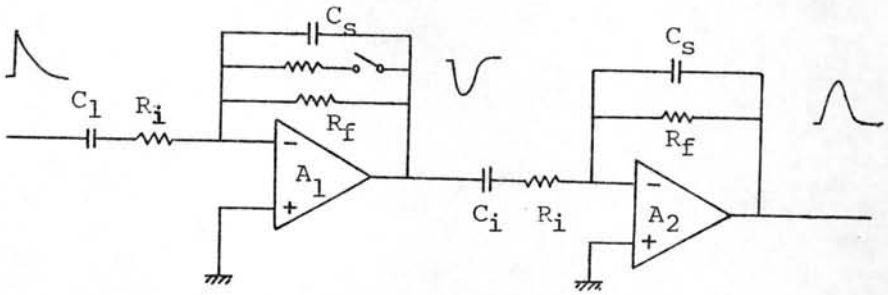


Fig. 2.8 Schematic diagram of amplifier

The two stages cascaded ac amplifier in Fig.2.8 provides overall gain squal to $A_1.A_2$.By using the terms of conventional operational amplifier the inverting input is virtualy ground. R_f closes the loop as the feedback, Ri acts as source resistance. The voltage gain is then calculated from

$$A = -\frac{V_o}{V_i} = -\frac{R_f}{R_i} \qquad \text{.....2.13}$$

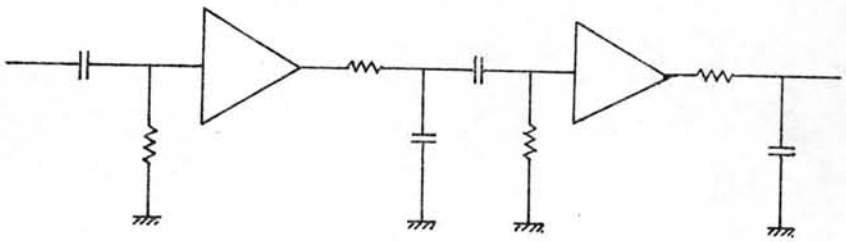


Fig. 2.9 Equivalent circuit of shaping network

2.2.4 Discriminator

In order to discriminator unwanted signal and to count the pulses properly, the shaped pulse must be compared with discriminator level and converted into logic pulses. The discriminator consists of a device which

produces a logic pulse only if the amplitude of shaped input pulse exceeds a set discrimination level as illustrate in Fig. 2.10 (a)

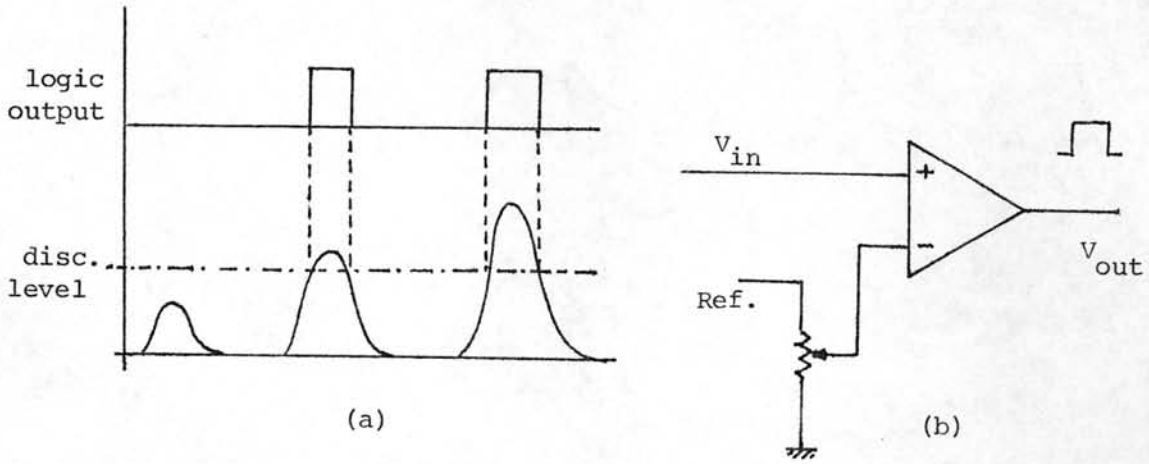


Fig. 2.10 (a) Illustration of the operation of discriminator

(b) Comparator is used as discriminator

A voltage comparator, as shown in Fig. 2.10 (b), is a device used as discriminator. The discrimination level is adjustable by using reference bias control at (-) input of the comparator. An output will give a logic pulse only when V_i at (+) input is more positive than positive reference voltage.

2.3 Scaler

The final step in nuclear pulse counting system is that the logic pulse must be accumulated and their number recorded over a fixed period of time. The device used for this purpose is a six decade counter or scaler, and counting period is controlled by the timer. This device consists of a cascaded up/down decade counter, decoder, display, multiplexer and leading zero suppress circuits, as shown schematically in Fig. 2.11.

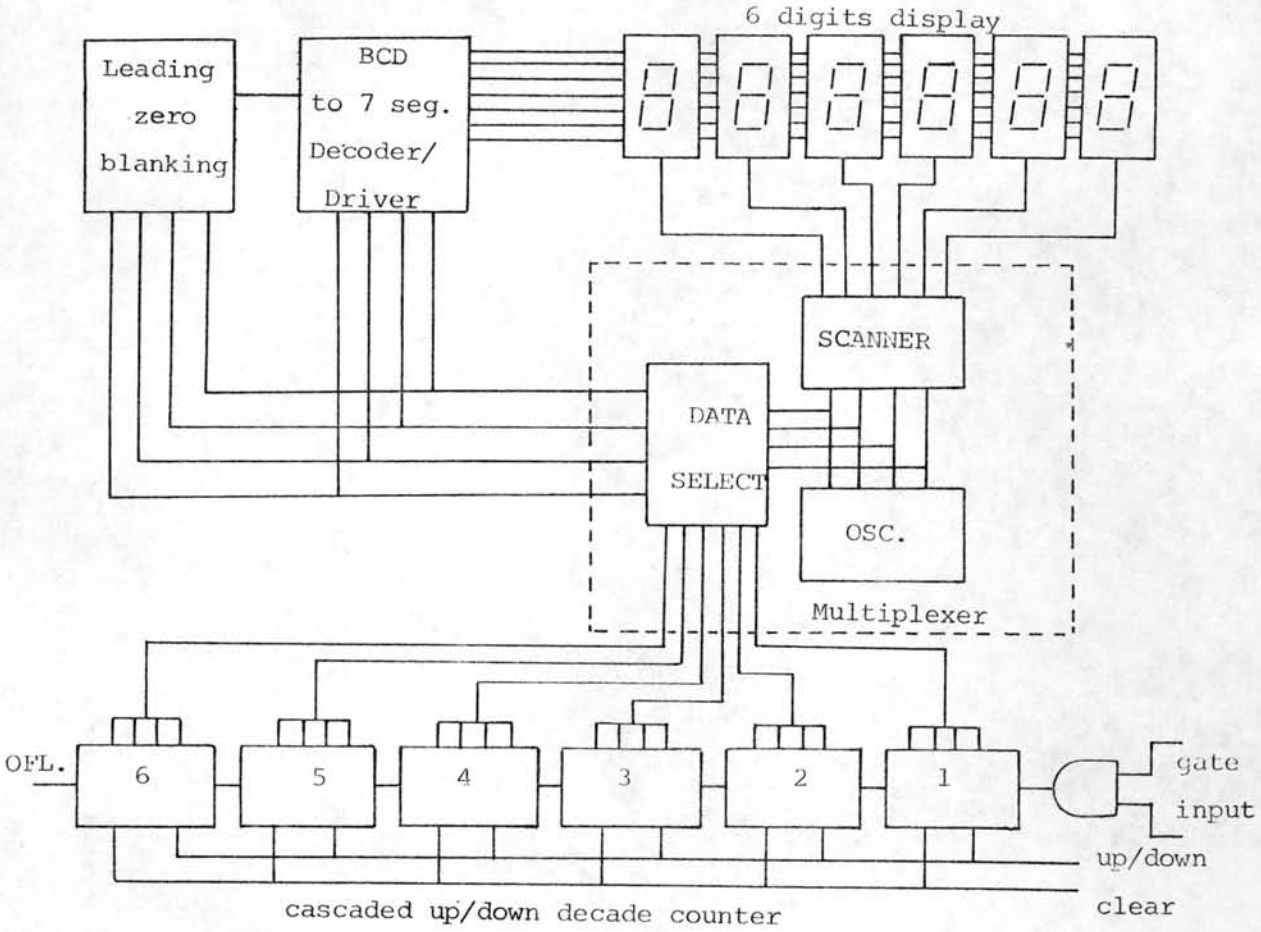


Fig. 2.11 Block diagram of scaler

2.3.1 Up/Down decade counter

A circuit, that has two stable states, is called a bi-stable multivibrator, more commonly referred to as a flip-flop (F.F). These can be used to store data, adding, or subtracting known as counting up or down and is called up/down binary counter. A 4-bit up/down binary counting unit can be converted to a decimal counter (BCD counter) by prematurely resetting the flip-flops.

The CD 40192 a CMOS Synchonous 4 - Bit up/down decade counter is shown in Fig. 2.12 (a).

Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive-going transition of this clock.

These counters feature preset inputs that are enabled when load is a logical " 0 " and a clear which forces all outputs to " 0 " when it is at logical " 1 ". The counters also have carry and borrow outputs so that they can be cascaded directly. Fig. 2.12(a) shows timing diagram of CD 40192.

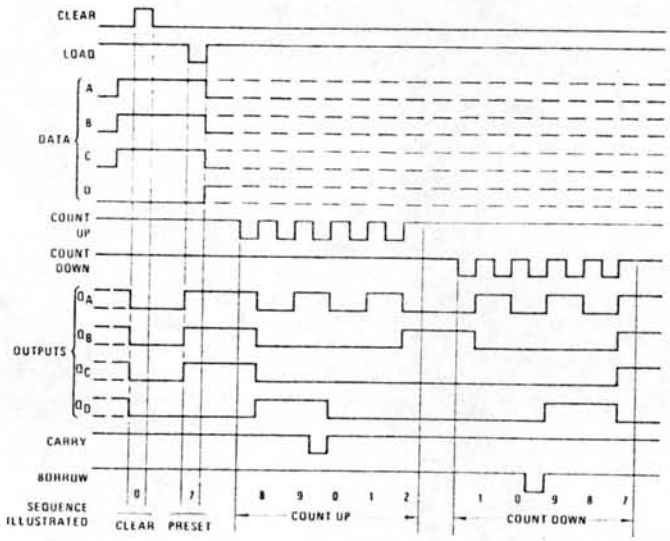


Fig. 2.12(a) Timing diagram of CD 40192

Sequence :

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one and two.
4. Count down to one, zero, borrow, nine, eight and seven.

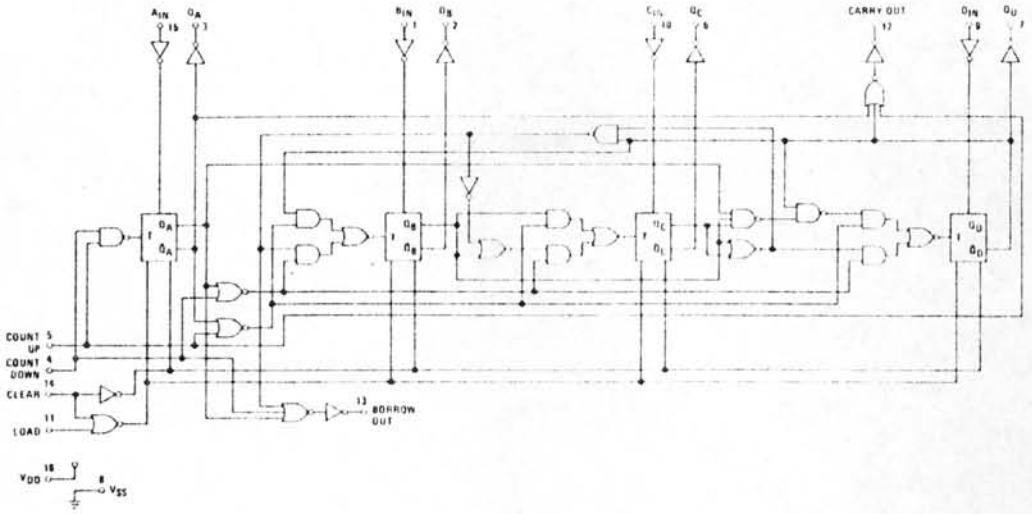


Fig.12 (b) Logic diagram of CD 40192

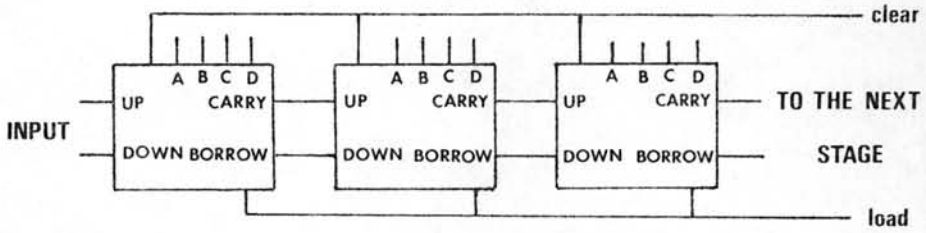
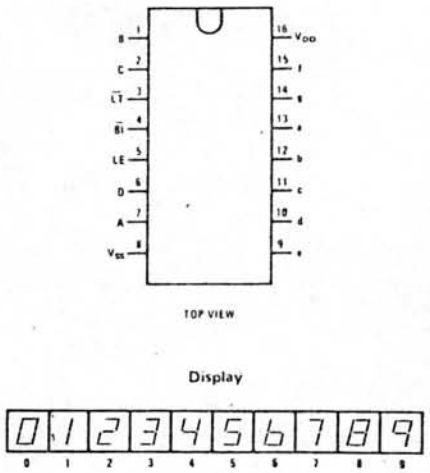


Fig. 2.13 cascading packages

2.3.2 Decoder and Display

Because humans are used to decimal number, the BCD output from up/down decade counter must be converted into decimal number. One technique is to use BCD-to-seven segment decoder together with seven-segment light emitting diodes display. By lighting the segment in appropriate combinations, all the numbers from 0 - 9 can be displayed. All BCD to seven segment conversion code are determined from the truth table in Fig. 2.14. The decoder is constructed with output drivers, lamp test (LT), blanking (BI), and latch enable (LE), for used to drive the segment, to test the display, to control brightness of the display and to store a BCD code, respectively.



INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	
0	1	1	1	0	1	1	0	0	0	0	0	0	0	
0	1	1	1	1	0	0	0	0	0	0	0	0	0	
0	1	1	1	1	0	1	0	0	0	0	0	0	0	
0	1	1	1	1	1	0	0	0	0	0	0	0	0	
0	1	1	1	1	1	1	0	0	0	0	0	0	0	
1	1	1	X	X	X	X				*				

X = Don't care
*Depends upon the BCD code applied during the 0 to 1 transition of LE

Fig. 2.14 Seven segment display and decoder

2.3.3 Multiplexer

A method sometimes used to reduce the quantity of ICs in the circuit using only one decoder circuit shared by all the display digits is called multiplexing. The principle of operation of multiplexing is illustrated in Fig. 2.15. There are two mechanical switchs, one is digital scanner switch and other BCD data scanner switch. These two switches are synchronized and scan the data and digit display by use of the common scan oscillator.

The mechanical switch as shown in Fig. 2.15 can be represented by decoder or data distributor logic. The digital scanner switch is represented by 1 of 10 decoder (see Fig. 2.16). For six digits the 6^{th} output is fed to clear counter to recycle for every 7 clock pulses.

In the same way, the BCD data scanner switch is represented by 1 of 8 data selector logic (see Fig. 2.17). For six digits and four data output (A,B,C,D) the data input and output of data selector logic must be

combined into four expanders, and data input use only 0 to 6

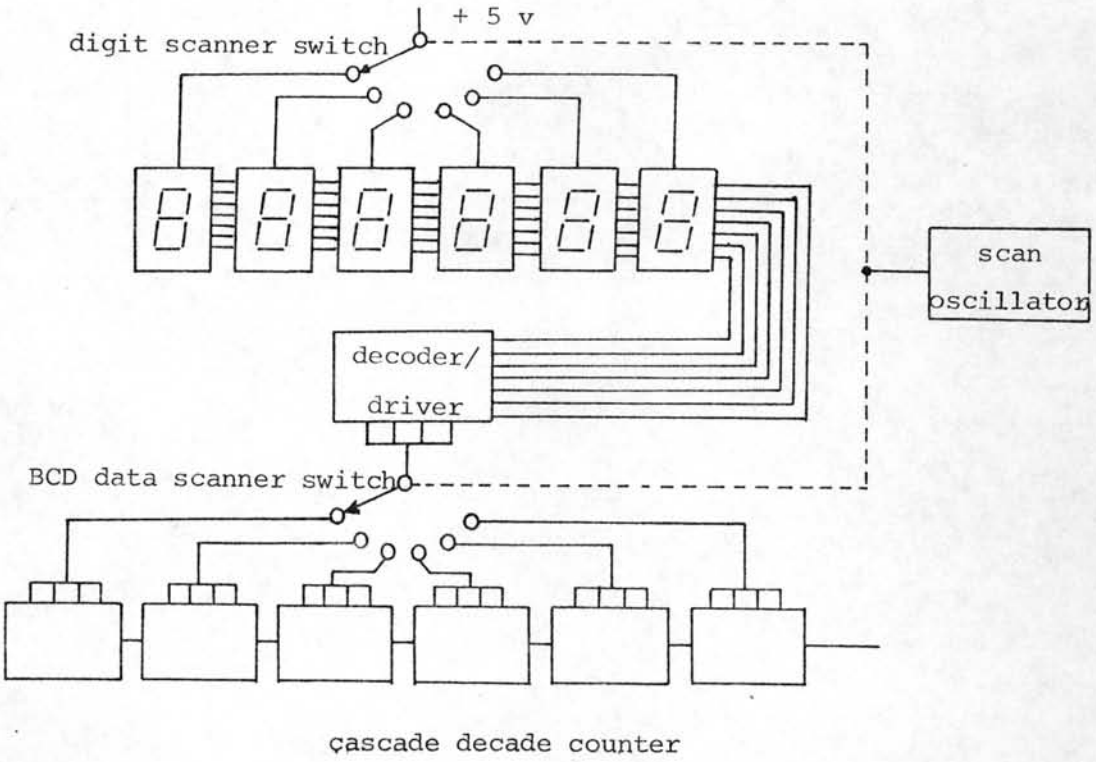


Fig. 2.15 Multiplexed digital display system

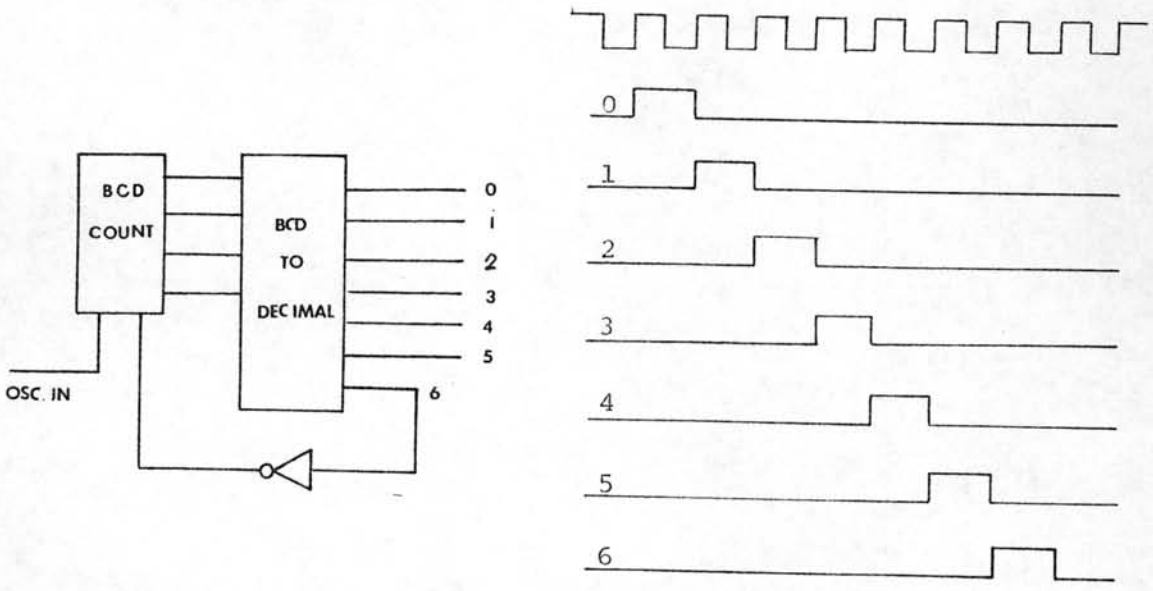
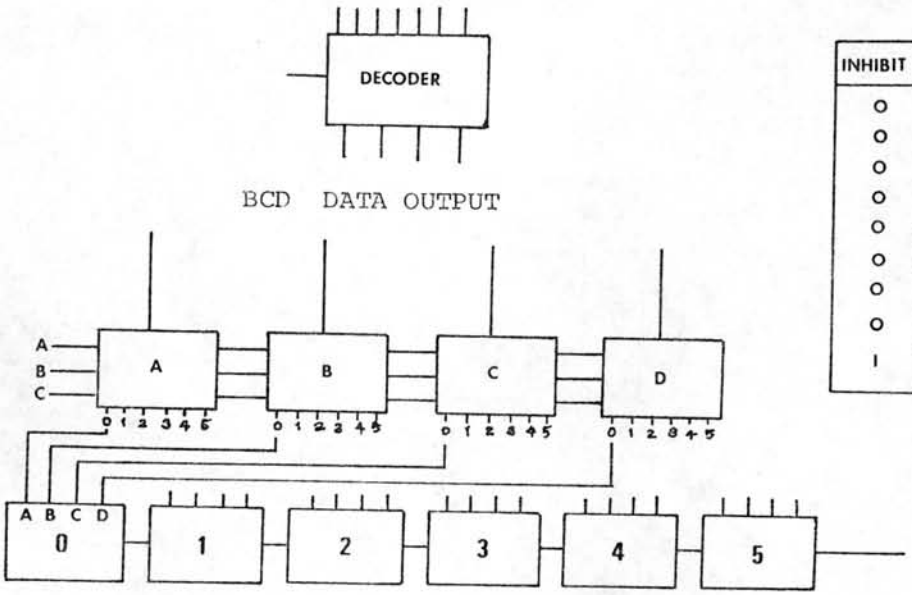


Fig. 2.16 Data selector logic for digit scanner switch



INHIBIT	C	B	A	ON CH.
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	ø	ø	ø	none

BCD decade counter

Fig. 2.17 Data selector logic for BCD data scanner

A,B,C,D are called 1 of 8 data selector logic switch.

2.3.4 Leading zero blanking

This circuit is designed for lopping off all the zeros to the left of the first significant digit in a display to save supplied power. Fig.2.18 shows how much the appearance of a display is improved in this manner.

(a) Without blanking

(b) Same number with blank

Fig. 2.18 Leading zero blanking improves display appearance

The technique for automatic leading-zero elemination is common in decoder system. From the decoder truth table in Fig. 2.14, when Bl input is logical o the output drivers are blank. This condition and some scanning outputs from multiplexer are determined in leading zero blanking circuit.

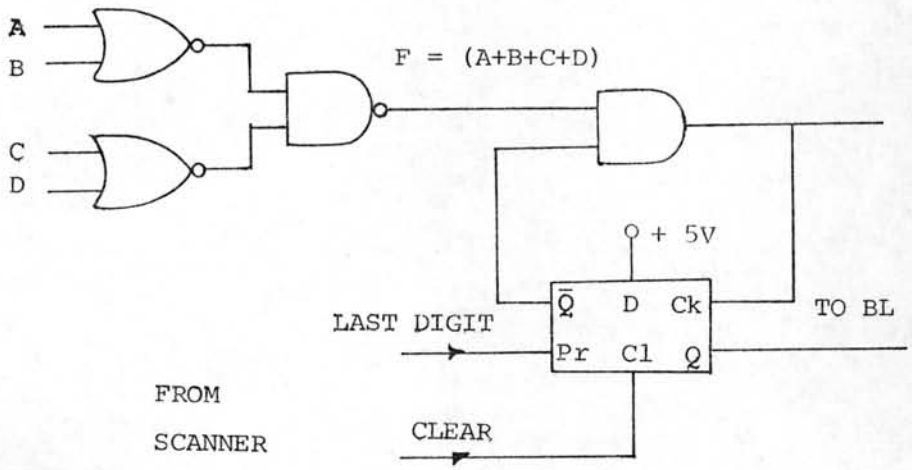


Fig. 2.19 Circuit diagram of leading-zero blanking

In Fig. 2.19, the blanking control output (Bl) is generated by the Q output of D flip-flop. At the start cycle of the scanner from left of the first significant digit, the clear condition is set, the Q output to logical D and $\bar{Q}$ to logical 1. The $\bar{Q}$ output is AND with combination gate { F = (A+B+C+D) } which checks the zero BCD code from first digit to last digit of counters. If the scanner reaches a non-zero BCD code output, the combination gate changes logical state to 1 and clock input of D flip-flop, changes to positive edge going. Suddenly, the state of Q output is changed to logical 1, the display of this digit is brightened through the last digit.

In case of all counter code being zero, the zero display will appear at the last digit by changing the state of Q output to logical 1 from last digit scanner at preset input.

2.4 Linear ratemeter

Linear ratemeter is a device that indicates the average rate of in coming pulses. The basic principle is that of feeding a known charge per pulse into a capacitor that is shunted by resistor and measured the average voltage appearing at the output of the circuit. A linear rate-meter configuration is shown in Fig. 2.20. The monostable circuit provides a pulse with constant pulse width for each in coming pulse, and controls charge transfer to the capacitor from meter driver circuit.

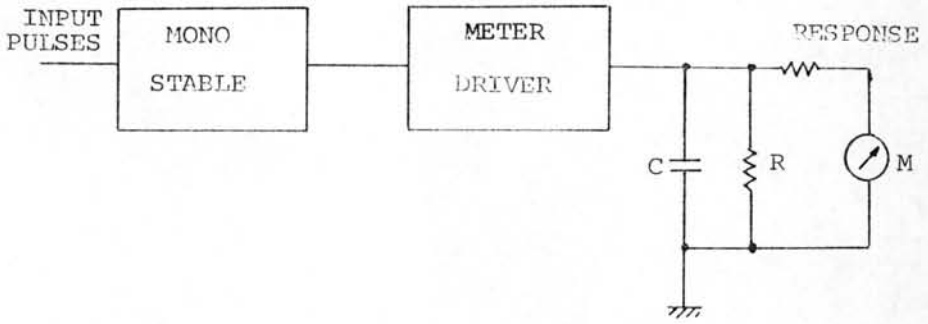


Fig. 2.20 Configuration of linear ratemeter

If the pulse rate is r and the charge transferred to the capacitor per pulse is q, then the charge rate is rq, thus the voltage of capacitor will increase until the current being drawn by the resistor is equal to charging rate. At this equilibrium point,

$$rq = \frac{V}{R}$$

and the voltage across the capacitor is

$$V = rqR \quad \text{.....2.14}$$

which is proportional to the pulse rate, r. Note that the voltage is independent of the value of capacitance. However, the capacitance does determine the time constant of the circuit, which is the time required for the voltage to respond to a change in the counting rate.

The charge on the capacitor, Q, at any time is a function of the in coming pulse rate, r, the charge per pulse, q, and the time constant of the rate meter, RC.

Since the charging rate is qr

and the discharging rate is $\frac{Q}{RC}$

The net rate of change of the charge on the capacitor, $\frac{dQ}{dt}$, is given by the differential equation.

$$\frac{dQ}{dt} = rq - \frac{Q}{RC} \quad \text{.....2.15}$$

The solution to Eq.2.15 for Q initially zero, assuming that r is constant,

$$Q(t) = qrRC\,(1-e^{-t/RC}) \quad \text{....2.16}$$

The voltage across the capacitor at any time is simply

$$V(t) = \frac{Q(t)}{C} = qrR(1-e^{-t/RC}) \quad \text{...2.17}$$

Note that when $t \gg RC$ Eq 2.17 reduce to

$$Q(t) = qrRC \quad \text{.....2.18}$$

$$V(t) = qrR \quad \text{.....2.19}$$

2.5 Timer

The function of a timer is simply to start and stop the accumulation period for a decade counter. The preset time can be selected by two digits thumbwheel switch N x 10^{M} in range of 1 - 9 x 10^{4} second. A Block diagram is shown in Fig. 2.21, consisting of time base and preset time sections.

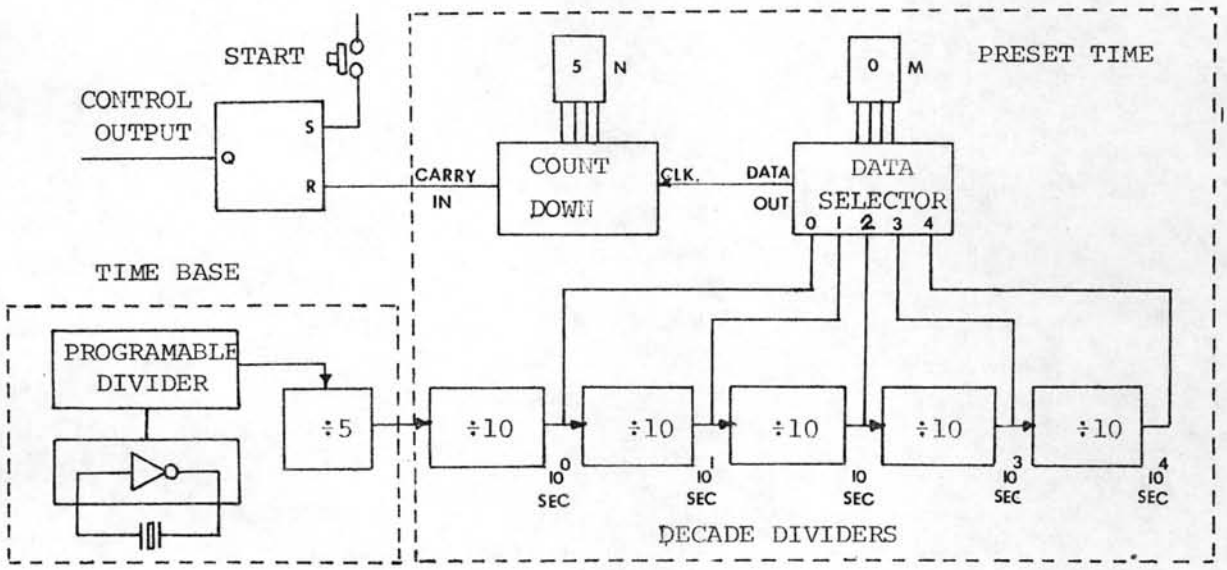


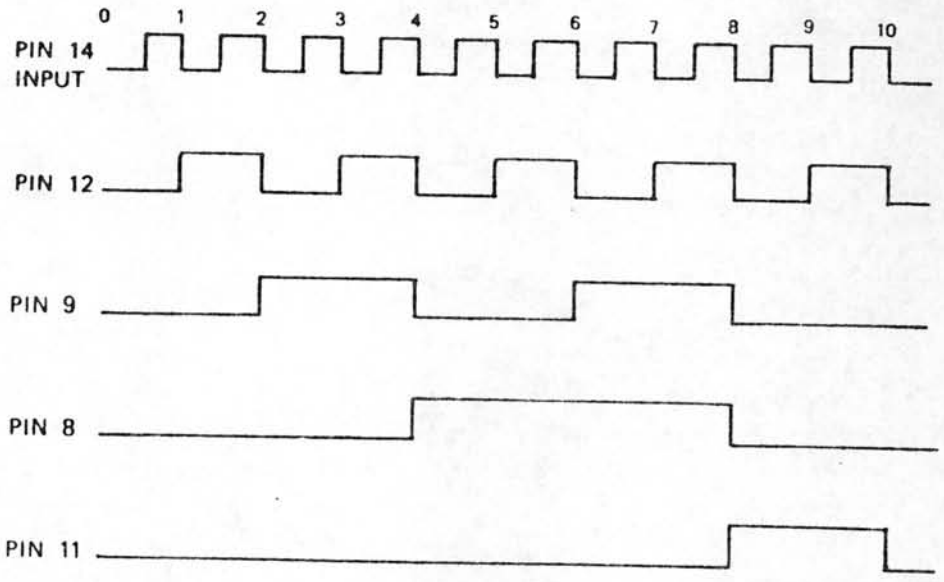
Fig. 2.21 A block diagram of timer

2.5.1 Time base

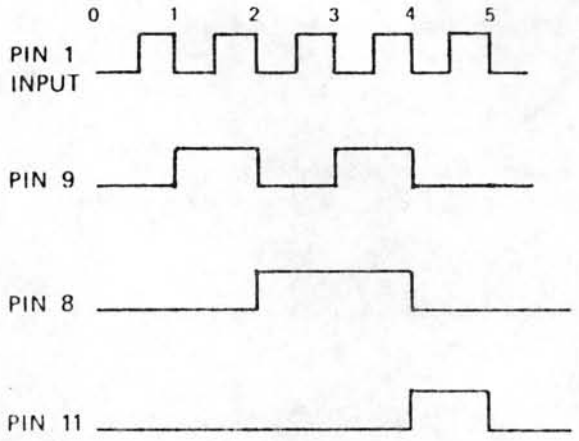
A precision time base is provided by the interconnection of a 3.58 MHz quartz crystal and the RC network shown in Fig. 2.21 together with programmable oscillator/divider. An oscillator frequency is devided by 17 stage internal divider giving a frequency of 50 Hz at its output. To obtain the 10 Hz time base output, the previous frequency is divided again by ÷ 5 stage {see the timing diagram in Fig. 2.22 (b)}.

2.5.2 Preset timer

A decade counter totalizes the number of pulses on its input and gives the output information in BCD. For every 10 inputs pulses, the next decade counter increments by 1 and thus the decade counter also performs a ÷ 10 function, as shown the timing diagram in Fig. 2.22 (a). With a series of decade deviders, we can obtain 10^0, 10^1, 10^2, 10^3 and 10^4 second space pulses from 10 Hz, output of time base. Each pulse can be selected by using data selector which is controlled by BCD thumbwheel switch, M, at data select (see in Fig. 2.21). The selected data output is fed to presettable count down, which is preset by BCD thumbwheel switch, N, at jams input. When count down goes to zero the carry in output will reset the R-S flip-flop, changing initial state. The Q output of R-S flip-flop gives the time interval for counting. For example, if two thumbwheel switches are set at 5×10^0 ($N \times 10^M$), the selected data is 5 seconds and count down from 5 to 0, the carry output will reset F-F.

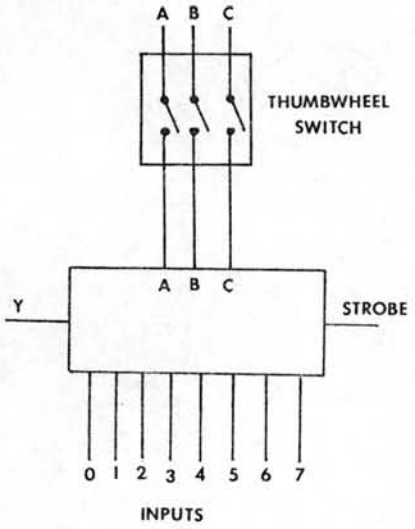


(a) in ÷ 10 MODE



(b) in ÷ 5 MODE

Fig. 2.22 Decade counter (7490) in ÷5 and ÷ 10 devider mode



INPUTS												OUTPUTS	
C	B	A	STROBE	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

Fig. 2.23 Block diagram and truth table of data selector

2.6 Low voltage power supply

The low voltage power supply is an important part for energizing electronic circuits and can be obtained from both ac source and a battery. All electronic circuits in a portable scaler require a stable source of dc power for its proper operation. This is provided by the voltage regulated power supply, using of a three-terminal voltage requlator and Zener diode as shown in Fig. 2.24

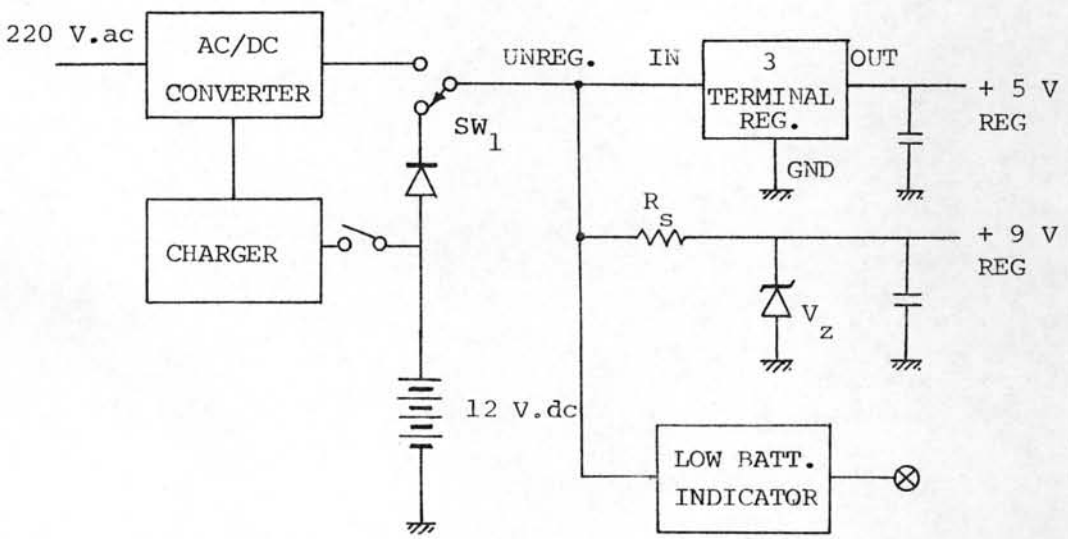


Fig. 2.24 Block diagram of low voltage power supply

2.6.1 Voltage regulated power supply

The voltage regulated power supply comprises the ac to dc converter (transformer, rectifier and filter) to provide unregulated dc voltage and regulator circuits to provide regulated output voltage. The diagram in Fig. 2.25 represents a full wave center-tapped rectifier using a capacitor filter and three-terminal voltage regulator.

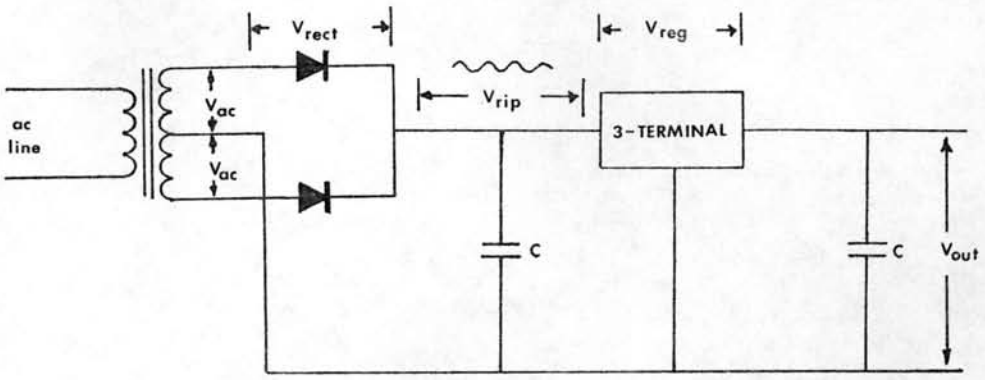


Fig. 2.25 Full wave center-tapped voltage regulator

From the circuit, the transformer secondary voltage (V_{ac}) can be calculated from the formula ;

$$V_{ac} = \frac{(V_{out} + V_{reg} + V_{rect} + V_{rip})}{0.92} \times \frac{V_{nor}}{V_{low\ line}} \times \frac{1}{\sqrt{2}}$$

where V_{reg} must be 3 volts dc or greater.

V_{rect} is about 1.25 volts dc.

V_{rip} is about 10 % of V_{dc} peak.

and 0.92 is a rectifier efficiency (typical)

In low power circuit, the regulated power supply using zener diode is very useful. The zener diode circuit arrangement is given in Fig.2.26, R_s is the series drop resistance and the load R_L is connected directly across the zener diode. The characteristics of the voltage regulator are governed by the range of unregulated dc input voltage (V_{in}) and the output load current (I_L) over which the zener diode maintains the constancy of its voltage drop.

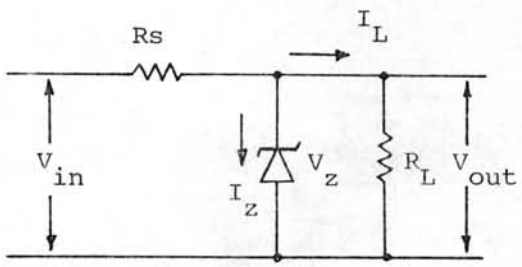


Fig. 2.26 Zener diode regulator circuit

The calculation of the value of series resistance to meet the V_{in} and I requirement is given in eq. 2.30

$$R_s = \frac{V_{in} - V_z}{I_z + I_L} \quad \text{.....2.30}$$

where I_z is chosen to be about 20 % of I_L.

2.6.2 Charger and Low battery voltage indicator

When the voltage of the battery becomes weak after a certain period in field work, the battery need be recharged. This can be done by simply pressing the push button switch with the scaler connected to ac line of 220 V. The charger will convert electrical energy into chemical energy stored in the battery. The maximum charging rate is about 1 A and the charging is automatically cut off when the battery is fully charged.

The scaler is also provided with low battery voltage indicator in order to prevent the malfunction of the scaler when the battery voltage becomes to low. The indicator circuit utilizes a comparator network the two inputs of which are directly connected to the battery output voltage and an internal voltage reference.