เอกสารอ้างอิง

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Z80®-CPU
Z80A-CPU

Product Specification

MARCH 1978

The Zilog Z80 product line is a complete set of microcomputer components, development systems and support software. The Z80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

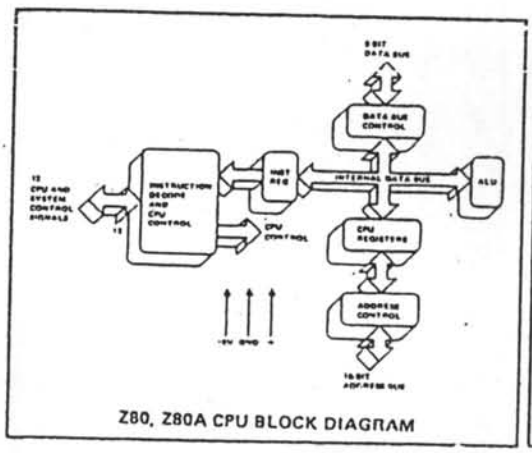
The Z80 and Z80A CPU's are third generation single chip microprocessors with unrivaled computational power. This increased computational power results in higher system through-put and more efficient memory utilization when compared to second generation microprocessors. In addition, the Z80 and Z80A CPU's are very easy to implement into a system because of their single voltage requirement plus all output signals are fully decoded and timed to control standard memory or peripheral circuits. The circuit is implemented using an N-channel, ion implanted, silicon gate MOS process.

Figure 1 is a block diagram of the CPU, Figure 2 details the internal register configuration which contains 208 bits of Read/Write memory that are accessible to the programmer. The registers include two sets of six general purpose registers that may be used individually as 8-bit registers or as 16-bit register pairs. There are also two sets of accumulator and flag registers. The programmer has access to either set of main or alternate registers through a group of exchange instructions. This alternate set allows foreground/background mode of operation or may be reserved for very fast Interrupt response. Each CPU also contains a 16-bit stack pointer which permits simple implementation of multiple level interrupts, unlimited subroutine nesting and simplification of many types of data handling.

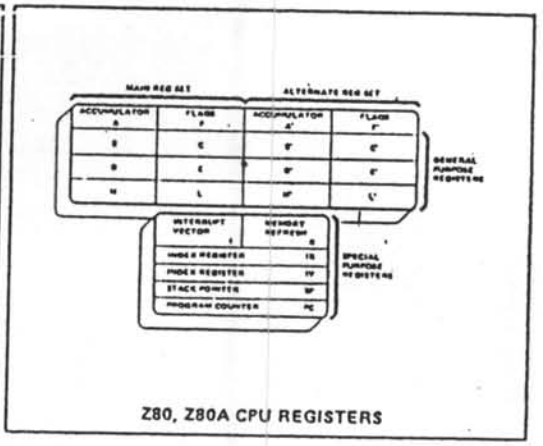
The two 16-bit index registers allow tabular data manipulation and easy implementation of relocatable code. The Refresh register provides for automatic, totally transparent refresh of external dynamic memories. The I register is used in a powerful interrupt response mode to form the upper 8 bits of a pointer to a interrupt service address table, while the interrupting device supplies the lower 8 bits of the pointer. An indirect call is then made to this service address.

FEATURES

- Single chip, N-channel Silicon Gate CPU.
- 158 instructions—includes all 78 of the 8080A instructions with total software compatibility. New instructions include 4-, 8- and 16-bit operations with more useful addressing modes such as indexed, bit and relative.
- 17 internal registers.
- Three modes of fast interrupt response plus a non-maskable interrupt.
- Directly interfaces standard speed static or dynamic memories with virtually no external logic.
- 1.0 μs instruction execution speed.
- Single 5 VDC supply and single-phase 5 volt Clock.
- Out-performs any other single chip microcomputer in 4-, 8-, or 16-bit applications.
- All pins TTL Compatible
- Built-in dynamic RAM refresh circuitry.

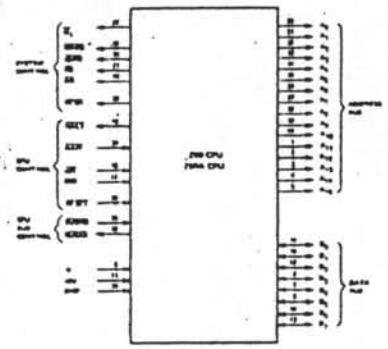


Z80, Z80A CPU BLOCK DIAGRAM



Z80, Z80A CPU REGISTERS

Z80, Z80A-CPU Pin Description



Z80, Z80A CPU PIN CONFIGURATION

A_0-A_{15} (Address Bus) Tri-state output, active high. A_0-A_{15} constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges.

D_0-D_7 (Data Bus) Tri-state input/output, active high. D_0-D_7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.

$\overline{M_1}$ (Machine Cycle one) Output, active low. $\overline{M_1}$ indicates that the current machine cycle is the OP code fetch cycle of an instruction execution.

$\overline{MREQ}$ (Memory Request) Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

$\overline{IORQ}$ (Input/ Output Request) Tri-state output, active low. The $\overline{IORQ}$ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An $\overline{IORQ}$ signal is also generated when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus.

$\overline{RD}$ (Memory Read) Tri-state output, active low. $\overline{RD}$ indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

$\overline{WR}$ (Memory Write) Tri-state output, active low. $\overline{WR}$ indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

$\overline{RFSH}$ (Refresh) Output, active low. $\overline{RFSH}$ indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current $\overline{MREQ}$ signal should be used to do a refresh read to all dynamic memories.

$\overline{HALT}$ (Halt state) Output, active low. $\overline{HALT}$ indicates that the CPU has executed a HALT software instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

$\overline{WAIT}$ (Wait) Input, active low. $\overline{WAIT}$ indicates to the Z-80 CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active.

$\overline{INT}$ (Interrupt Request) Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled.

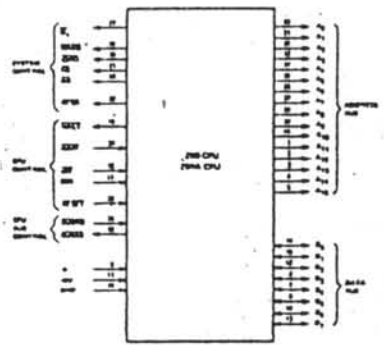
$\overline{NMI}$ (Non Maskable Interrupt) Input, active low. The non-maskable interrupt request line has a higher priority than $\overline{INT}$ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. $\overline{NMI}$ automatically forces the Z-80 CPU to restart to location 0066_H.

$\overline{RESET}$ Input, active low. $\overline{RESET}$ initializes the CPU as follows: reset interrupt enable flip-flop, clear PC and registers I and R and set interrupt to 8080A mode. During reset time, the address and data bus go to a high impedance state and all control output signals go to the inactive state.

$\overline{BUSRQ}$ (Bus Request) Input, active low. The bus request signal has a higher priority than $\overline{NMI}$ and is always recognized at the end of the current machine cycle and is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these busses.

$\overline{BUSAK}$ (Bus Acknowledge) Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

Z80, Z80A-CPU Pin Description



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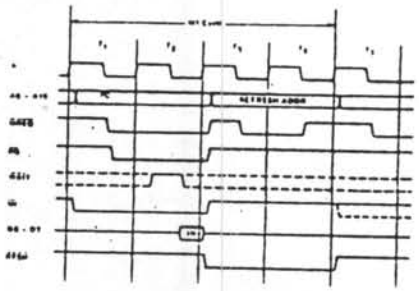
$\overline{BUSAK}$ (Bus Acknowledge) Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

Timing Waveforms

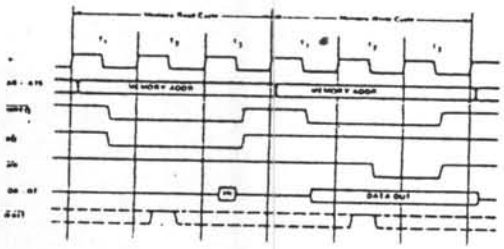
INSTRUCTION OP CODE FETCH

The program counter content (PC) is placed on the address bus immediately at the start of the cycle. One half clock time later $\overline{MREQ}$ goes active. The falling edge of $\overline{MREQ}$ can be used directly as a chip enable to dynamic memories. $\overline{RD}$ when active indicates that the memory data should be enabled onto the CPU data bus. The CPU samples data with the rising edge of the clock state T_3. Clock states T_3 and T_4 of a fetch cycle are used to refresh dynamic memories while the CPU is internally decoding and executing the instruction. The refresh control signal $\overline{RFSH}$ indicates that a refresh read of all dynamic memories should be accomplished.



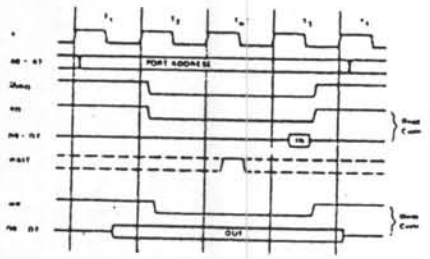
MEMORY READ OR WRITE CYCLES

Illustrated here is the timing of memory read or write cycles other than an OP code fetch (M_1 cycle). The $\overline{MREQ}$ and $\overline{RD}$ signals are used exactly as in the fetch cycle. In the case of a memory write cycle, the $\overline{MREQ}$ also becomes active when the address bus is stable so that it can be used directly as a chip enable for dynamic memories. The $\overline{WR}$ line is active when data on the data bus is stable so that it can be used directly as a R/W pulse to virtually any type of semiconductor memory.



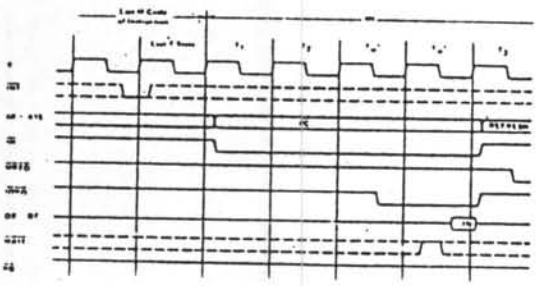
INPUT OR OUTPUT CYCLES

Illustrated here is the timing for an I/O read or I/O write operation. Notice that during I/O operations a single wait state is automatically inserted (Tw*). The reason for this is that during I/O operations this extra state allows sufficient time for an I/O port to decode its address and activate the $\overline{WAIT}$ line if a wait is required.



INTERRUPT REQUEST/ACKNOWLEDGE CYCLE

The interrupt signal is sampled by the CPU with the rising edge of the last clock at the end of any instruction. When an interrupt is accepted, a special M_1 cycle is generated. During this M_1 cycle, the $\overline{IORQ}$ signal becomes active (instead of $\overline{MREQ}$) to indicate that the interrupting device can place an 8-bit vector on the data bus. Two wait states (Tw*) are automatically added to this cycle so that a ripple priority interrupt scheme, such as the one used in the Z80 peripheral controllers, can be easily implemented.



Z80, Z80A Instruction Set

The following is a summary of the Z80, Z80A instruction set showing the assembly language mnemonic and the symbolic operation performed by the instruction. A more detailed listing appears in the Z80-CPU technical manual, and assembly language programming manual. The instructions are divided into the following categories:

8-bit loads	Miscellaneous Group
16-bit loads	Rotates and Shifts
Exchanges	Bit Set, Reset and Test
Memory Block Moves	Input and Output
Memory Block Searches	Jumps
8-bit arithmetic and logic	Calls
16-bit arithmetic	Restarts
General purpose Accumulator & Flag Operations	Returns

In the table the following terminology is used.

b ≡ a bit number in any 8-bit register or memory location

cc ≡ flag condition code
- NZ ≡ non zero
- Z ≡ zero
- NC ≡ non carry
- C ≡ carry
- PO ≡ Parity odd or no over flow
- PE ≡ Parity even or over flow
- P ≡ Positive
- M ≡ Negative (minus)

d ≡ any 8-bit destination register or memory location

dd ≡ any 16-bit destination register or memory location

e ≡ 8-bit signed 2's complement displacement used in relative jumps and indexed addressing

L ≡ 8 special call locations in page zero. In decimal notation these are 0, 8, 16, 24, 32, 40, 48 and 56

n ≡ any 8-bit binary number

nn ≡ any 16-bit binary number

r ≡ any 8-bit general purpose register (A, B, C, D, E, H, or L)

s ≡ any 8-bit source register or memory location

s_b ≡ a bit in a specific 8-bit register or memory location

ss ≡ any 16-bit source register or memory location

subscript "L" ≡ the low order 8 bits of a 16-bit register

subscript "H" ≡ the high order 8 bits of a 16-bit register

( ) ≡ the contents within the ( ) are to be used as a pointer to a memory location or I/O port number

8-bit registers are A, B, C, D, E, H, L, I and R

16-bit register pairs are AF, BC, DE and HL

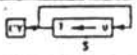
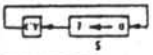
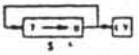
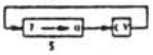
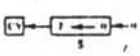
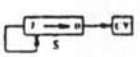
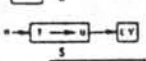
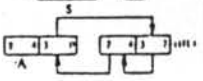
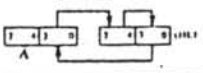
16-bit registers are SP, PC, IX and IY

Addressing Modes implemented include combinations of the following:

Immediate	Indexed
Immediate extended	Register
Modified Page Zero	Implied
Relative	Register Indirect
Extended	Bit

	Mnemonic	Symbolic Operation	Comments
8-BIT LOADS	LD r, s	r ← s	s ≡ r, n, (HL), (IX+e), (IY+e)
	LD d, r	d ← r	d ≡ (HL), r (IX+e), (IY+e)
	LD d, n	d ← n	d ≡ (HL), (IX+e), (IY+e)
	LD A, s	A ← s	s ≡ (BC), (DE), (nn), I, R
	LD d, A	d ← A	d ≡ (BC), (DE), (nn), I, R
16-BIT LOADS	LD dd, nn	dd ← nn	dd ≡ BC, DE, HL, SP, IX, IY
	LD dd, (nn)	dd ← (nn)	dd ≡ BC, DE, HL, SP, IX, IY
	LD (nn), ss	(nn) ← ss	ss ≡ BC, DE, HL, SP, IX, IY
	LD SP, ss	SP ← ss	ss ≡ HL, IX, IY
	PUSH ss	$(SP-1) \leftarrow ss_H$; $(SP-2) \leftarrow ss_L$	ss ≡ BC, DE, HL, AF, IX, IY
	POP dd	$dd_L \leftarrow (SP)$; $dd_H \leftarrow (SP+1)$	dd ≡ BC, DE, HL, AF, IX, IY
EXCHANGES	EX DE, HL	DE ↔ HL	
	EX AF, AF'	AF ↔ AF'	
	EXX	$\begin{pmatrix} BC \\ DE \\ HL \end{pmatrix} \leftrightarrow \begin{pmatrix} BC' \\ DE' \\ HL' \end{pmatrix}$	
	EX (SP), ss	$(SP) \leftrightarrow ss_L$, $(SP+1) \leftrightarrow ss_H$	ss ≡ HL, IX, IY

	Mnemonic	Symbolic Operation	Comments
MEMORY BLOCK MOVES	LDI	(DE) ← (HL), DE ← DE+1 HL ← HL+1, BC ← BC-1	
	LDIR	(DE) ← (HL), DE ← DE+1 HL ← HL+1, BC ← BC-1 Repeat until BC = 0	
	LDD	(DE) ← (HL), DE ← DE-1 HL ← HL-1, BC ← BC-1	
	LDDR	(DE) ← (HL), DE ← DE-1 HL ← HL-1, BC ← BC-1 Repeat until BC = 0	
MEMORY BLOCK SEARCHES	CPI	A-(HL), HL ← HL+1 BC ← BC-1	
	CPIR	A-(HL), HL ← HL+1 BC ← BC-1, Repeat until BC = 0 or A = (HL)	A-(HL) sets the flags only. A is not affected
	CPD	A-(HL), HL ← HL-1 BC ← BC-1	
	CPDR	A-(HL), HL ← HL-1 BC ← BC-1, Repeat until BC = 0 or A = (HL)	
8-BIT ALU	ADD s	A ← A + s	
	ADC s	A ← A + s + CY	CY is the carry flag
	SUB s	A ← A - s	
	SBC s	A ← A - s - CY	s ≡ r, n, (HL) (IX+e), (IY+e)
	AND s	A ← A ∧ s	
	OR s	A ← A ∨ s	
	XOR s	A ← A ⊕ s	

	Mnemonic	Symbolic Operation	Comments
8-BIT ALU	CP s	A - s	s = r, n (HL) (IX+e), (IY+e)
	INC d	d ← d + 1	d = r, (HL) (IX+e), (IY+e)
	DEC d	d ← d - 1	
16-BIT ARITHMETIC	ADD HL, ss	HL ← HL + ss	ss ≡ BC, DE HL, SP
	ADC HL, ss	HL ← HL + ss + CY	
	SBC HL, ss	HL ← HL - ss - CY	
	ADD IX, ss	IX ← IX + ss	ss ≡ BC, DE, IX, SP
	ADD IY, ss	IY ← IY + ss	ss ≡ BC, DE, IY, SP
	INC dd	dd ← dd + 1	dd ≡ BC, DE, HL, SP, IX, IY
	DEC dd	dd ← dd - 1	dd ≡ BC, DE, HL, SP, IX, IY
GP ACC. & FLAG	DAA	Converts A contents into packed BCD following add or subtract.	Operands must be in packed BCD format
	CPL	$A \leftarrow \overline{A}$	
	NEG	A ← 00 - A	
	CCF	$CY \leftarrow \overline{CY}$	
	SCF	CY ← 1	
MISCELLANEOUS	NOP	No operation	
	HALT	Halt CPU	
	DI	Disable Interrupts	
	EI	Enable Interrupts	
	IM 0	Set interrupt mode 0	8080A mode Call to 0038_H Indirect Call
	IM 1	Set interrupt mode 1	
	IM 2	Set interrupt mode 2	
ROTATES AND SHIFTS	RLC s		s ≡ r, (HL) (IX+e), (IY+e)
	RL s		
	RRC s		
	RR s		
	SLA s		
	SRA s		
	SRL s		
	RLD		
	RRD		

	Mnemonic	Symbolic Operation	Comments
BIT S, R, & T	BIT b, s	$Z \leftarrow \overline{s_b}$	Z is zero flag
	SET b, s	$s_b \leftarrow 1$	s ≡ r, (HL) (IX+e), (IY+e)
	RES b, s	$s_b \leftarrow 0$	
INPUT AND OUTPUT	IN A, (n)	A ← (n)	
	IN r, (C)	r ← (C)	Set flags
	INI	(HL) ← (C), HL ← HL + 1 B ← B - 1	
	INIR	(HL) ← (C), HL ← HL + 1 B ← B - 1 Repeat until B = 0	
	IND	(HL) ← (C), HL ← HL - 1 B ← B - 1	
	INDR	(HL) ← (C), HL ← HL - 1 B ← B - 1 Repeat until B = 0	
	OUT(n), A	(n) ← A	
	OUT(C), r	(C) ← r	
	OUTI	(C) ← (HL), HL ← HL + 1 B ← B - 1	
	OTIR	(C) ← (HL), HL ← HL + 1 B ← B - 1 Repeat until B = 0	
	OUTD	(C) ← (HL), HL ← HL - 1 B ← B - 1	
	OTDR	(C) ← (HL), HL ← HL - 1 B ← B - 1 Repeat until B = 0	
JUMPS	JP nn	PC ← nn	
	JP cc, nn	If condition cc is true PC ← nn, else continue	cc ≡ NZ PO, Z PE, NC P, C M
	JR e	PC ← PC + e	
	JR kk, e	If condition kk is true PC ← PC + e, else continue	kk ≡ NZ NC, Z C
	JP (ss)	PC ← ss	ss = HL, IX, IY
	DJNZ e	B ← B - 1, if B = 0 continue, else PC ← PC + e	
CALLS	CALL nn	$(SP-1) \leftarrow PC_H$ $(SP-2) \leftarrow PC_L$, PC ← nn	
	CALL cc, nn	If condition cc is false continue, else same as CALL nn	cc ≡ NZ PO, Z PE, NC P, C M
RESTARTS	RST L	$(SP-1) \leftarrow PC_H$ $(SP-2) \leftarrow PC_L$, $PC_H \leftarrow 0$ $PC_L \leftarrow L$	
RETURNS	RET	$PC_L \leftarrow (SP)$, $PC_H \leftarrow (SP+1)$	
	RET cc	If condition cc is false continue, else same as RET	cc ≡ NZ PO, Z PE, NC P, C M
	RETI	Return from interrupt, same as RET	
	RETN	Return from non-maskable interrupt	

A.C. Characteristics Z80-CPU

T_A = 0°C to 70°C, Vcc = +5V ± 5%, Unless Otherwise Noted.

Signal	Symbol	Parameter	Min	Max	Unit	Test Condition	
Φ	t_c	Clock Period	4	[12]	nsec		[12] $t_c = t_{w(\Phi H)} + t_{w(\Phi L)} + t_r + t_f$
	$t_{w(\Phi H)}$	Clock Pulse Width, Clock High	180	[E]	nsec		
	$t_{w(\Phi L)}$	Clock Pulse Width, Clock Low	180	2000	nsec		
	t_r, t_f	Clock Rise and Fall Time		30	nsec		
A_{0-15}	$t_{D(AD)}$	Address Output Delay		145	nsec	C_L = 50pF	
	$t_{F(AD)}$	Delay to Float		110	nsec		
	t_{acm}	Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	[1]		nsec		[1] $t_{acm} = t_{w(\Phi H)} + t_f - 75$
	t_{aci}	Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	[2]		nsec		[2] $t_{aci} = t_c - 40$
	t_{ca}	Address Stable from $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$ or $\overline{MREQ}$	[3]		nsec		
	t_{cal}	Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float	[4]		nsec		
D_{0-7}	$t_{D(D)}$	Data Output Delay		230	nsec	C_L = 50pF	[3] $t_{cd} = t_{w(\Phi L)} + t_f - 40$
	$t_{F(D)}$	Delay to Float During Write Cycle		90	nsec		
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	50		nsec		[4] $t_{cdf} = t_{w(\Phi L)} + t_f - 60$
	$t_{S\overline{\Phi}(D)}$	Data Setup Time to Falling Edge of Clock During M2 to M5	60		nsec		
	t_{dcm}	Data Stable Prior to $\overline{WR}$ (Memory Cycle)	[5]		nsec		[5] $t_{dcm} = t_c - 210$
	t_{dci}	Data Stable Prior to $\overline{WR}$ (I/O Cycle)	[6]		nsec		
	t_{cdf}	Data Stable From $\overline{WR}$	[7]		nsec		[6] $t_{dcl} = t_{w(\Phi L)} + t_f - 210$
	t_{H}	Any Hold Time for Setup Time	0		nsec		[7] $t_{cdf} = t_{w(\Phi L)} + t_f - 80$
$\overline{MREQ}$	$t_{DL\Phi(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low		100	nsec	C_L = 50pF	
	$t_{DH\Phi(MR)}$	$\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High		100	nsec		
	$t_{DH\overline{\Phi}(MR)}$	$\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High		100	nsec		
	$t_{w(MRL)}$	Pulse Width, $\overline{MREQ}$ Low	[8]		nsec		[8] $t_{w(MRL)} = t_c - 40$
	$t_{w(MRH)}$	Pulse Width, $\overline{MREQ}$ High	[9]		nsec		[9] $t_{w(MRH)} = t_{w(\Phi H)} + t_f - 30$
$\overline{IORQ}$	$t_{DL\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low		90	nsec	C_L = 50pF	
	$t_{DL\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low		110	nsec		
	$t_{DH\Phi(IR)}$	$\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High		100	nsec		
	$t_{DH\overline{\Phi}(IR)}$	$\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High		110	nsec		
$\overline{RD}$	$t_{DL\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low		100	nsec	C_L = 50pF	
	$t_{DL\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low		130	nsec		
	$t_{DH\Phi(RD)}$	$\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High		100	nsec		
	$t_{DH\overline{\Phi}(RD)}$	$\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High		110	nsec		
$\overline{WR}$	$t_{DL\Phi(WR)}$	$\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low		80	nsec	C_L = 50pF	
	$t_{DL\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low		90	nsec		
	$t_{DH\overline{\Phi}(WR)}$	$\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High		100	nsec		
	$t_{w(WRL)}$	Pulse Width, $\overline{WR}$ Low	[10]		nsec		[10] $t_{w(WRL)} = t_c - 40$
$\overline{M1}$	$t_{DL(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ Low		130	nsec	C_L = 50pF	
	$t_{DH(M1)}$	$\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High		130	nsec		
$\overline{RFSH}$	$t_{DL(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low		180	nsec	C_L = 50pF	
	$t_{DH(RF)}$	$\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ High		150	nsec		
$\overline{WAIT}$	$t_{s(WT)}$	$\overline{WAIT}$ Setup Time to Falling Edge of Clock	70		nsec		
$\overline{HALT}$	$t_{D(HT)}$	$\overline{HALT}$ Delay Time From Falling Edge of Clock		300	nsec	C_L = 50pF	
$\overline{INT}$	$t_{s(IT)}$	$\overline{INT}$ Setup Time to Rising Edge of Clock	80		nsec		
$\overline{NMI}$	$t_{w(NML)}$	Pulse Width, $\overline{NMI}$ Low	80		nsec		
$\overline{BUSRQ}$	$t_{s(BQ)}$	$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	80		nsec		
$\overline{BUSAK}$	$t_{DL(BA)}$	$\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low		120	nsec	C_L = 50pF	
	$t_{DH(BA)}$	$\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ High		110	nsec		
$\overline{RESET}$	$t_{s(RS)}$	$\overline{RESET}$ Setup Time to Rising Edge of Clock	90		nsec		
	$t_{F(C)}$	Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)		100	nsec		
	t_{m}	$\overline{M1}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	[11]		nsec		[11] $t_m = 3t_c + t_{w(\Phi H)} + t_f - 80$

NOTES

A. Data should be enabled onto the CPU data bus when $\overline{RD}$ is active. During interrupt acknowledge data should be enabled when $\overline{M1}$ and $\overline{IORQ}$ are both active.

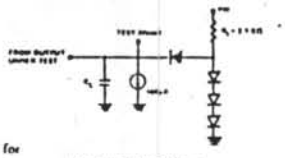
B. All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.

C. The $\overline{RESET}$ signal must be active for a minimum of 3 clock cycles.

D. Output Delay vs. Loaded Capacitance

TA = 70°C Vcc = +5V ±5%

Add 10nsec delay for each 50pf increase in load up to a maximum of 200pf for the data bus & 100pf for address & control lines



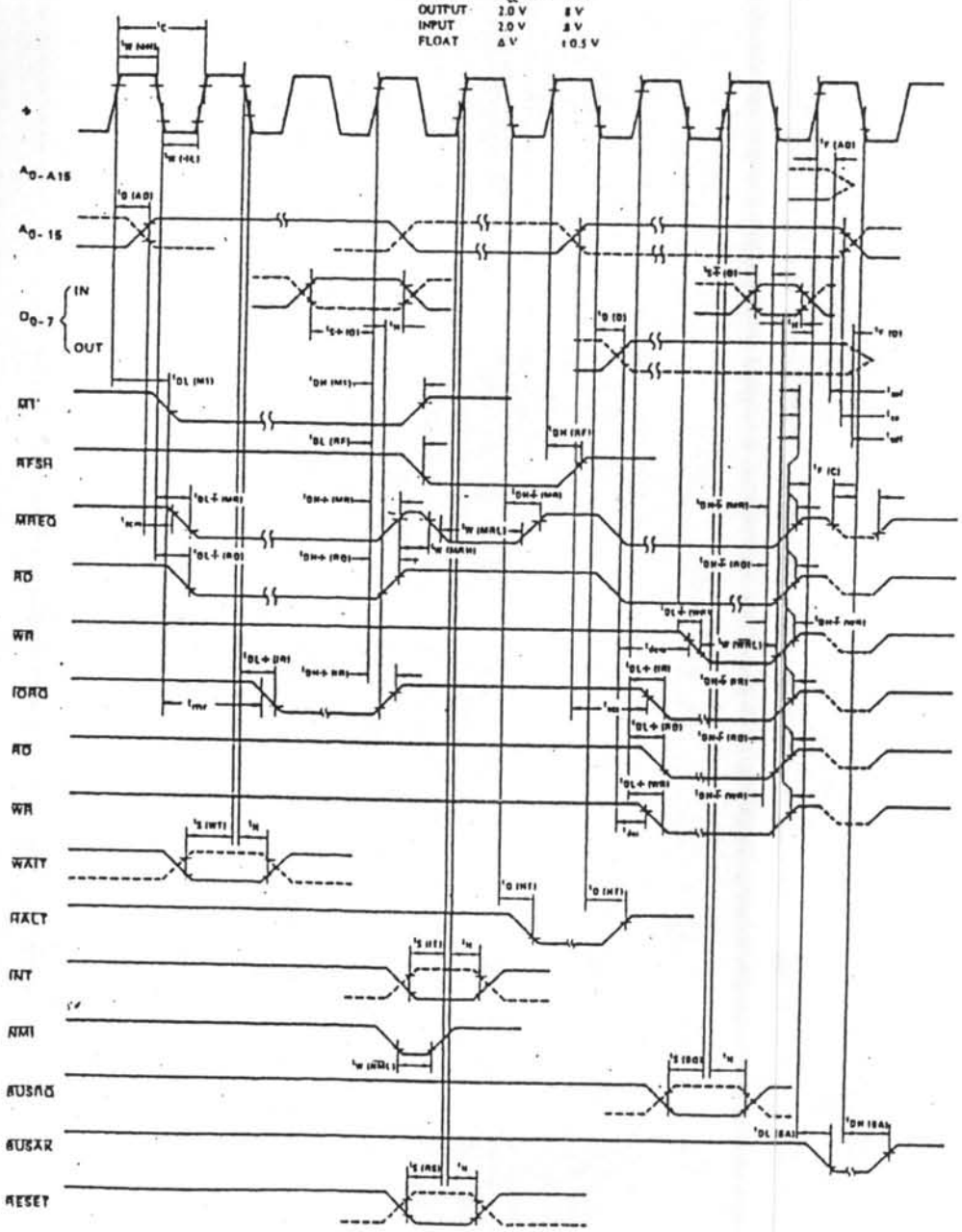
Load circuit for Output

E. Although static by design, testing guarantees $t_{w(\Phi H)}$ of 200 usec maximum

A.C. Timing Diagram

Timing measurements are made at the following voltages, unless otherwise specified:

	"1"	"0"
CLOCK	V_{CC} -.6V	.45V
OUTPUT	2.0 V	.8 V
INPUT	2.0 V	.8 V
FLOAT	Δ V	±0.5 V



Absolute Maximum Ratings

Temperature Under Bias	Specified operating range.
Storage Temperature	-65°C to +150°C
Voltage On Any Pin with Respect to Ground	-0.3V to +7V
Power Dissipation	1.5 W

*Comment

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: For Z80-CPU all AC and DC characteristics remain the same for the military grade parts except I_{cc}.

I_{cc} = 200 mA

Z80-CPU D.C. Characteristics

T_A = 0°C to 70°C, V_{cc} = 5V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	V_{cc} -.6		V_{cc}+.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{cc}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -250uA
I_{CC}	Power Supply Current			150	mA	
I_{LI}	Input Leakage Current			10	µA	V_{IN} = 0 to V_{cc}
I_{LOH}	Tri-State Output Leakage Current in Float			10	µA	V_{OUT} = 2.4 to V_{cc}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	µA	V_{OUT} = 0.4V
I_{LD}	Data Bus Leakage Current in Input Mode			±10	µA	$0 \leq V_{IN} \leq V_{cc}$

Capacitance

T_A = 25°C, f = 1 MHz,
unmeasured pins returned to ground

Symbol	Parameter	Max.	Unit
C_ϕ	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

Z80-CPU Ordering Information

C – Ceramic
P – Plastic
S – Standard 5V ±5% 0° to 70°C
E – Extended 5V ±5% -40° to 85°C
M – Military 5V ±10% -55° to 125°C

Z80A-CPU D.C. Characteristics

T_A = 0°C to 70°C, V_{cc} = 5V ± 5% unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{ILC}	Clock Input Low Voltage	-0.3		0.45	V	
V_{IHC}	Clock Input High Voltage	V_{cc} -.6		V_{cc}+.3	V	
V_{IL}	Input Low Voltage	-0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{cc}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.8mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -250uA
I_{CC}	Power Supply Current		90	200	mA	
I_{LI}	Input Leakage Current			10	µA	V_{IN} = 0 to V_{cc}
I_{LOH}	Tri-State Output Leakage Current in Float			10	µA	V_{OUT} = 2.4 to V_{cc}
I_{LOL}	Tri-State Output Leakage Current in Float			-10	µA	V_{OUT} = 0.4V
I_{LD}	Data Bus Leakage Current in Input Mode			±10	µA	$0 \leq V_{IN} \leq V_{cc}$

Capacitance

T_A = 25°C, f = 1 MHz,
unmeasured pins returned to ground

Symbol	Parameter	Max.	Unit
C_ϕ	Clock Capacitance	35	pF
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	10	pF

Z80A-CPU Ordering Information

C – Ceramic
P – Plastic
S – Standard 5V ±5% 0° to 70°C

A.C. Characteristics — Z80A-CPU

T_A = 0°C to 70°C, Vcc = +5V ± 5%, Unless Otherwise Noted.

Signal	Symbol	Parameter	Min	Max	Unit	Test Condition	
Φ	t_c	Clock Period	25	1121	μsec		[12] $t_c = t_{w(\Phi H)} + t_{w(\Phi L)} + t_r + t_f$
	$t_{w(\Phi H)}$	Clock Pulse Width, Clock High	110	[E]	nsec		
	$t_{w(\Phi L)}$	Clock Pulse Width, Clock Low	110	2000	nsec		
	t_r, t_f	Clock Rise and Fall Time		30	nsec		
A_{0-15}	$t_{D(AD)}$	Address Output Delay		110	nsec	C_L = 50pF	
	$t_{F(AD)}$	Delay to Float		90	nsec		
	t_{acm}	Address Stable Prior to MREQ (Memory Cycle)	111		nsec		[1] $t_{acm} = t_{w(\Phi H)} + t_f - 45$
	t_{aci}	Address Stable Prior to IORQ, RD or WR (I/O Cycle)	121		nsec		[2] $t_{aci} = t_c - 70$
	t_{ca}	Address Stable from RD, WR, IORQ or MREQ	131		nsec		
	t_{caf}	Address Stable From RD or WR During Float	141		nsec		
D_{0-7}	$t_{D(D)}$	Data Output Delay		150	nsec	C_L = 50pF	[3] $t_{ca} = t_{w(\Phi L)} + t_f - 50$
	$t_{F(D)}$	Delay to Float During Write Cycle		90	nsec		[4] $t_{caf} = t_{w(\Phi L)} + t_f - 45$
	$t_{S\Phi(D)}$	Data Setup Time to Rising Edge of Clock During M1 Cycle	35		nsec		[5] $t_{dcm} = t_c - 170$
	$t_{S\overline{\Phi}(D)}$	Data Setup Time to Falling Edge of Cluck During M2 to M5	50		nsec		[6] $t_{dci} = t_{w(\Phi L)} + t_f - 170$
	t_{dcm}	Data Stable Prior to WR (Memory Cycle)	151		nsec		[7] $t_{cdf} = t_{w(\Phi L)} + t_f - 70$
	t_{dci}	Data Stable Prior to WR (I/O Cycle)	161		nsec		
	t_{cdf}	Data Stable From WR	171				
	t_H	Any Hold Time for Setup Time		0	nsec		
MREQ	$t_{DL\overline{\Phi}(MR)}$	MREQ Delay From Falling Edge of Clock, MREQ Low		85	nsec	C_L = 50pF	
	$t_{DH\Phi(MR)}$	MREQ Delay From Rising Edge of Clock, MREQ High		85	nsec		
	$t_{DH\overline{\Phi}(MR)}$	MREQ Delay From Falling Edge of Clock, MREQ High		85	nsec		[8] $t_{w(\overline{MR}L)} = t_c - 30$
	$t_{w(\overline{MR}L)}$	Pulse Width, MREQ Low	181		nsec		[9] $t_{w(\overline{MR}H)} = t_{w(\Phi H)} + t_f - 20$
	$t_{w(\overline{MR}H)}$	Pulse Width, MREQ High	191		nsec		
IORQ	$t_{DL\Phi(IR)}$	IORQ Delay From Rising Edge of Clock, IORQ Low		75	nsec	C_L = 50pF	
	$t_{DL\overline{\Phi}(IR)}$	IORQ Delay From Falling Edge of Clock, IORQ Low		85	nsec		
	$t_{DH\Phi(IR)}$	IORQ Delay From Rising Edge of Clock, IORQ High		85	nsec		
	$t_{DH\overline{\Phi}(IR)}$	IORQ Delay From Falling Edge of Clock, IORQ High		85	nsec		
RD	$t_{DL\Phi(RD)}$	RD Delay From Rising Edge of Clock, RD Low		85	nsec	C_L = 50pF	
	$t_{DL\overline{\Phi}(RD)}$	RD Delay From Falling Edge of Clock, RD Low		95	nsec		
	$t_{DH\Phi(RD)}$	RD Delay From Rising Edge of Clock, RD High		85	nsec		
	$t_{DH\overline{\Phi}(RD)}$	RD Delay From Falling Edge of Clock, RD High		85	nsec		
WR	$t_{DL\Phi(WR)}$	WR Delay From Rising Edge of Clock, WR Low		65	nsec	C_L = 50pF	
	$t_{DL\overline{\Phi}(WR)}$	WR Delay From Falling Edge of Clock, WR Low		80	nsec		
	$t_{DH\overline{\Phi}(WR)}$	WR Delay From Falling Edge of Clock, WR High		80	nsec		
	$t_{w(\overline{WR}L)}$	Pulse Width, WR Low	1101		nsec		[10] $t_{w(\overline{WR}L)} = t_c - 30$
M1	$t_{DL(M1)}$	M1 Delay From Rising Edge of Clock, M1 Low		100	nsec	C_L = 50pF	
	$t_{DH(M1)}$	M1 Delay From Rising Edge of Clock, M1 High		100	nsec		
RFSH	$t_{DL(RF)}$	RFSH Delay From Rising Edge of Clock, RFSH Low		130	nsec	C_L = 50pF	
	$t_{DH(RF)}$	RFSH Delay From Rising Edge of Clock, RFSH High		120	nsec		
WAIT	$t_{s(WT)}$	WAIT Setup Time to Falling Edge of Clock	70		nsec		
HALT	$t_{D(HT)}$	HALT Delay Time From Falling Edge of Clock		300	nsec	C_L = 50pF	
INT	$t_{s(IT)}$	INT Setup Time to Rising Edge of Clock	80		nsec		
NMI	$t_{w(\overline{NM}L)}$	Pulse Width, NMI Low	80		nsec		
BUSRQ	$t_{s(BQ)}$	BUSRQ Setup Time to Rising Edge of Clock	50		nsec		
BUSAK	$t_{DL(BA)}$	BUSAK Delay From Rising Edge of Clock, BUSAK Low		100	nsec	C_L = 50pF	
	$t_{DH(BA)}$	BUSAK Delay From Falling Edge of Clock, BUSAK High		100	nsec		
RESET	$t_{s(RS)}$	RESET Setup Time to Rising Edge of Clock	60		nsec		
	$t_{F(C)}$	Delay to Float (MREQ, IORQ, RD and WR)		80	nsec		
	t_{mi}	M1 Stable Prior to IORQ (Interrupt Ack.)	1111		nsec		[11] $t_{mi} = 3t_c + t_{w(\Phi H)} + t_f - 45$

NOTES:

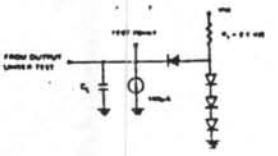
A. Data should be enabled onto the CPU data bus when RD is active. During interrupt acknowledge data should be enabled when M1 and IORQ are both active.

B. All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.

C. The RESET signal must be active for a minimum of 3 clock cycles.

D. Output Delay vs. Loaded Capacitance
TA = 70°C Vcc = +5V ±5%
Add 10nsec delay for each 50pf increase in load up to maximum of 200pf for data bus and 100pf for address & control lines.

E. Although static by design, testing guarantees $t_{w(\Phi H)}$ of 200 μsec maximum.



Load circuit for Output

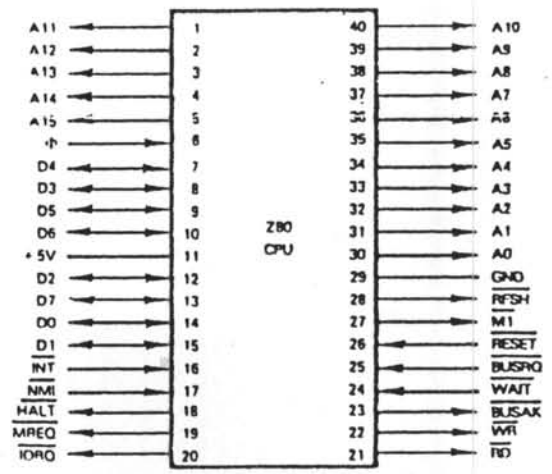
$\overline{RD}$ is a tristate signal which indicates that the CPU wishes to read data from either memory or an I/O device, as identified $\overline{MREQ}$ or $\overline{IORQ}$.

$\overline{WR}$ is a tristate control signal which indicates that the CPU wishes to write data to memory or an I/O device as indicated by $\overline{MREQ}$ and $\overline{IORQ}$. Some Z80 I/O devices have no $\overline{WR}$ input. These devices assume a Write operation when $\overline{IORQ}$ is low and $\overline{RD}$ is high. $\overline{RD}$ low specifies a Read operation.

The various ways in which the three control signals, $\overline{M1}$, $\overline{IORQ}$, and $\overline{RD}$, may be interpreted are summarized in Table 7-5, which occurs in the description of the Z80 PIO device.

$\overline{RFSH}$ is a control signal used to refresh dynamic memories. When $\overline{RFSH}$ is output low, the current $\overline{MREQ}$ signal should be used to refresh dynamic memory, as addressed by the lower seven bits of the Address Bus, A0 - A6.

Next we will describe CPU control signals.



PIN NAME	DESCRIPTION	TYPE
A0 - A15	Address Bus	Tristate, Output
D0 - D7	Data Bus	Tristate, Bidirectional
$\overline{M1}$	Identifies instruction fetch machine cycle	Output
$\overline{MREQ}$	Memory request — indicates that CPU is performing memory access	Tristate, Output
$\overline{IORQ}$	I/O request — indicates I/O operation in progress	Tristate, Output
$\overline{RD}$	CPU read from memory or I/O device	Tristate, Output
$\overline{WR}$	CPU write to memory or I/O device	Tristate, Output
$\overline{RFSH}$	Refresh dynamic memories	Output
$\overline{HALT}$	CPU Halt executed	Output
$\overline{WAIT}$	Wait state request	Input
$\overline{INT}$	Interrupt request	Input
$\overline{NMI}$	Nonmaskable interrupt request	Input
$\overline{RESET}$	Reset and initialize CPU	Input
$\overline{BUSRQ}$	Request for control of Address, Data and Control Busses	Input
$\overline{BUSAK}$	Bus acknowledge	Output
Φ	CPU clock	Input
+5V, GND	Power and Ground	

Figure 7-4. Z80 CPU Signals and Pin Assignments

intel

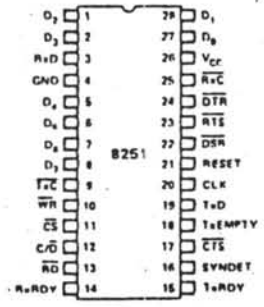
Silicon Gate MOS 8251

PROGRAMMABLE COMMUNICATION INTERFACE

- Synchronous and Asynchronous Operation
  - Synchronous:
    - 5-8 Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
  - Asynchronous:
    - 5-8 Bit Characters
    - Clock Rate — 1, 16 or 64 Times Baud Rate
    - Break Character Generation
    - 1, 1½, or 2 Stop Bits
    - False Start Bit Detection
- Baud Rate —DC to 56k Baud (Sync Mode)
  DC to 9.6k Baud (Async Mode)
- Full Duplex, Double Buffered, Transmitter and Receiver
- Error Detection — Parity, Overrun, and Framing
- Fully Compatible with 8080 CPU
- 28-Pin DIP Package
- All Inputs and Outputs Are TTL Compatible
- Single 5 Volt Supply
- Single TTL Clock

The 8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) Chip designed for data communications in microcomputer systems. The USART is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM Bi-Sync). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPT. The chip is constructed using N-channel silicon gate technology.

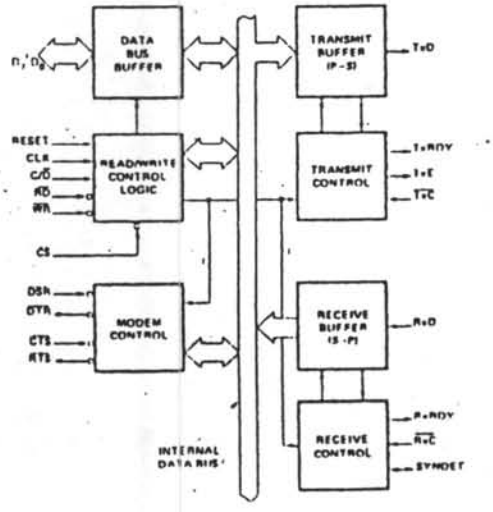
PIN CONFIGURATION



Pin Name	Pin Function
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock
TxD	Transmitter Data
RxC	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)

Pin Name	Pin Function
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET	Sync Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
Vcc	+5 Volt Supply
GND	Ground

BLOCK DIAGRAM



8251 BASIC FUNCTIONAL DESCRIPTION

General

The 8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter designed specifically for the 8080 Microcomputer System. Like other I/O devices in the 8080 Microcomputer System its functional configuration is programmed by the systems software for maximum flexibility. The 8251 can support virtually any serial data technique currently in use (including IBM "bi-sync").

In a communication environment an interface device must convert parallel format system data into serial format for transmission and convert incoming serial format data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear "transparent" to the CPU, a simple input or output of byte-oriented system data.

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8251 to the 8080 system Data Bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions of the 8080 CPU. Control words, Command words and Status information are also transferred through the Data Bus Buffer.

Read/Write Control Logic

This functional block accepts inputs from the 8080 Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for device functional definition.

RESET (Reset)

A "high" on this input forces the 8251 into an "Idle" mode. The device will remain at "Idle" until a new set of control words is written into the 8251 to program its functional definition.

CLK (Clock)

The CLK input is used to generate internal device timing and is normally connected to the Phase 2 (TTL) output of the 8224 Clock Generator. No external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver or Transmitter clock inputs for synchronous mode (4 times for asynchronous mode).

$\overline{WR}$ (Write)

A "low" on this input informs the 8251 that the CPU is outputting data or control words, in essence, the CPU is writing out to the 8251.

$\overline{RD}$ (Read)

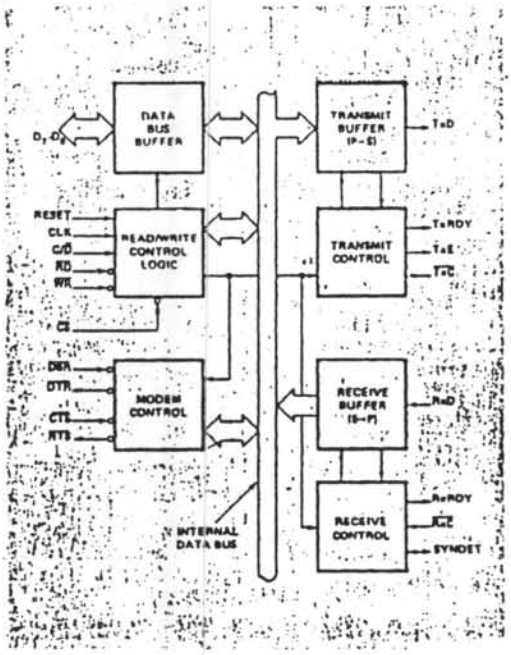
A "low" on this input informs the 8251 that the CPU is inputting data or status information, in essence, the CPU is reading from the 8251.

C/$\overline{D}$ (Control/Data)

This input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs informs the 8251 that the word on the Data Bus is either a data character, control word or status information.
1 = CONTROL 0 = DATA

$\overline{CS}$ (Chip Select)

A "low" on this input enables the 8251. No reading or writing will occur unless the device is selected.



C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	8251 → DATA BUS
0	1	0	0	DATA BUS → 8251
1	0	1	0	STATUS → DATA BUS
1	1	0	0	DATA BUS → CONTROL
X	X	X	1	DATA BUS → 3-STATE

Modem Control

The 8251 has a set of control inputs and outputs that can be used to simplify the interface to almost any Modem. The modem control signals are general purpose in nature and can be used for functions other than Modem control, if necessary.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input signal is general purpose in nature. Its condition can be tested by the CPU using a Status Read operation. The $\overline{DSR}$ input is normally used to test Modem conditions such as Data Set Ready.

$\overline{DTR}$ (Data Terminal Ready)

The $\overline{DTR}$ output signal is general purpose in nature. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{DTR}$ output signal is normally used for Modem control such as Data Terminal Ready or Rate Select.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output signal is general purpose in nature. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{RTS}$ output signal is normally used for Modem control such as Request to Send.

$\overline{CTS}$ (Clear to Send)

A "low" on this input enables the 8251 to transmit data (serial) if the Tx EN bit in the Command byte is set to a "one."

Transmitter Buffer

The Transmitter Buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Transmitter Control

The Transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function.

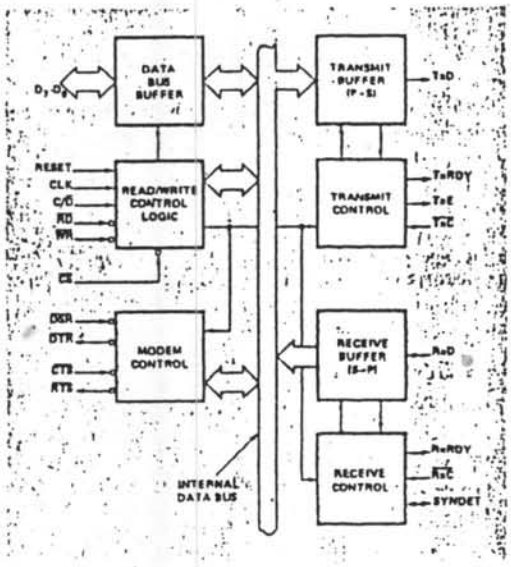
TxRDY (Transmitter Ready)

This output signals the CPU that the transmitter is ready to accept a data character. It can be used as an interrupt to the system or for the Polled operation the CPU can check TxRDY using a status read operation. TxRDY is automatically reset when a character is loaded from the CPU.

TxE (Transmitter Empty)

When the 8251 has no characters to transmit, the TxE output will go "high". It resets automatically upon receiving a character from the CPU. TxE can be used to indicate the end of a transmission mode, so that the CPU "knows" when to "turn the line around" in the half-duplexed operational mode.

In SYNChronous mode, a "high" on this output indicates that a character has not been loaded and the SYNC character or characters are about to be transmitted automatically as "fillers".



$\overline{TxC}$ (Transmitter Clock)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the frequency of $\overline{TxC}$ is equal to the actual Baud Rate (1X). In Asynchronous transmission mode, the frequency of $\overline{TxC}$ is a multiple of the actual Baud Rate. A portion of the mode instruction selects the value of the multiplier; it can be 1x, 16x or 64x the Baud Rate.

For Example:

If Baud Rate equals 110 Baud,
$\overline{TxC}$ equals 110 Hz (1x)
$\overline{TxC}$ equals 1.76 kHz (16x)
$\overline{TxC}$ equals 7.04 kHz (64x).
If Baud Rate equals 9600 Baud,
$\overline{TxC}$ equals 614.4 kHz (64x).

The falling edge of $\overline{TxC}$ shifts the serial data out of the 8251.

Receiver Buffer

The Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU. Serial data is input to the RxD pin.

Receiver Control

This functional block manages all receiver-related activities.

RxRDY (Receiver Ready)

This output indicates that the 8251 contains a character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU or for Polled operation the CPU can check the condition of RxRDY using a status read operation. RxRDY is automatically reset when the character is read by the CPU.

$\overline{RxC}$ (Receiver Clock)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the frequency of $\overline{RxC}$ is equal to the actual Baud Rate (1x). In Asynchronous Mode, the frequency of $\overline{RxC}$ is a multiple of the actual Baud Rate. A portion of the mode instruction selects the value of the multiplier; it can be 1x, 16x or 64x the Baud Rate.

For Example: If Baud Rate equals 300 Baud,
$\overline{RxC}$ equals 300 Hz (1x)
$\overline{RxC}$ equals 4800 Hz (16x)
$\overline{RxC}$ equals 19.2 kHz (64x).
If Baud Rate equals 2400 Baud,
$\overline{RxC}$ equals 2400 Hz (1x)
$\overline{RxC}$ equals 38.4 kHz (16x)
$\overline{RxC}$ equals 153.6 kHz (64x).

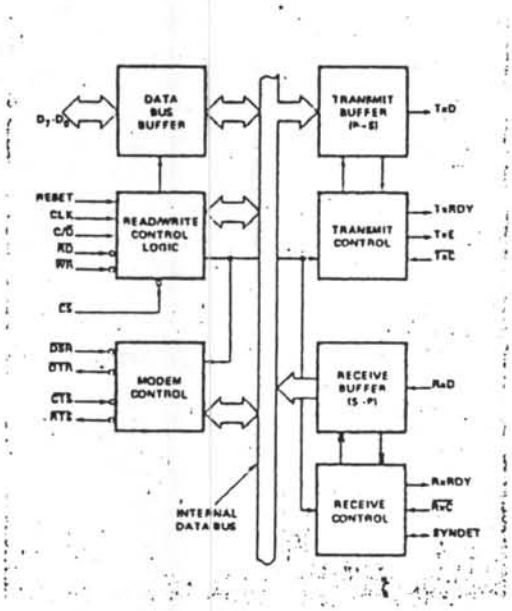
Data is sampled into the 8251 on the rising edge of $\overline{RxC}$.

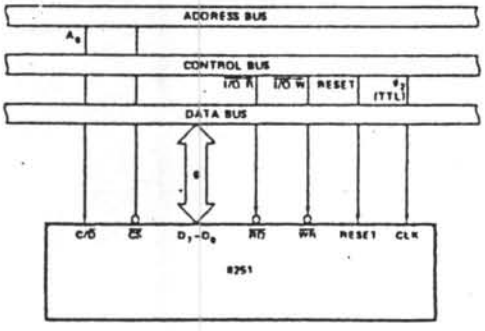
NOTE: In most communications systems, the 8251 will be handling both the transmission and reception operations of a single link. Consequently, the Receive and Transmit Baud Rates will be the same. Both $\overline{TxC}$ and $\overline{RxC}$ will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

SYNDET (SYNC Detect)

This pin is used in SYNChronous Mode only. It is used as either input or output, programmable through the Control Word. It is reset to "low" upon RESET. When used as an output (Internal Sync mode), the SYNDET pin will go "high" to indicate that the 8251 has located the SYNC character in the Receive mode. If the 8251 is programmed to use double Sync characters (bi-sync), then SYNDET will go "high" in the middle of the last bit of the second Sync character. SYNDET is automatically reset upon a Status Read operation.

When used as an input, (external SYNC detect mode), a positive going signal will cause the 8251 to start assembling data characters on the falling edge of the next $\overline{RxC}$. Once in SYNC, the "high" input signal can be removed. The duration of the high signal should be at least equal to the period of $\overline{RxC}$.





8251 Interface to 8080 Standard System Bus

DETAILED OPERATION DESCRIPTION

General

The complete functional definition of the 8251 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize the 8251 to support the desired communications format. These control words will program the: BAUD RATE, CHARACTER LENGTH, NUMBER OF STOP BITS, SYNCHRONOUS or ASYNCHRONOUS OPERATION, EVEN/ODD PARITY etc. In the Synchronous Mode, options are also provided to select either internal or external character synchronization.

Once programmed, the 8251 is ready to perform its communication functions. The TxRDY output is raised "high" to signal the CPU that the 8251 is ready to receive a character. This output (TxRDY) is reset automatically when the CPU writes a character into the 8251. On the other hand, the 8251 receives serial data from the MODEM or I/O device, upon receiving an entire character the RxRDY output is raised "high" to signal the CPU that the 8251 has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU read operation.

The 8251 cannot begin transmission until the TxEN(Transmitter Enable) bit is set in the Command Instruction and it has received a Clear To Send (CTS) input. The TxD output will be held in the marking state upon Reset.

Programming the 8251

Prior to starting data transmission or reception, the 8251 must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the 8251 and must immediately follow a Reset operation (internal or external).

The control words are split into two formats:

1. Mode Instruction
2. Command Instruction

Mode Instruction

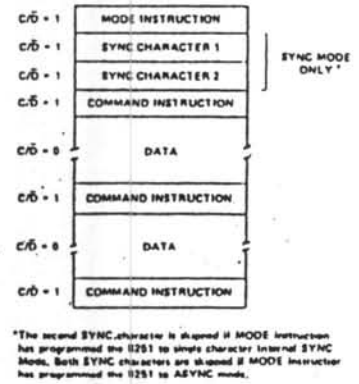
This format defines the general operational characteristics of the 8251. It must follow a Reset operation (internal or external). Once the Mode instruction has been written into the 8251 by the CPU, SYNC characters or Command instructions may be inserted.

Command Instruction

This format defines a status word that is used to control the actual operation of the 8251.

Both the Mode and Command instructions must conform to a specified sequence for proper device operation. The Mode Instruction must be inserted immediately following a Reset operation, prior to using the 8251 for data communication.

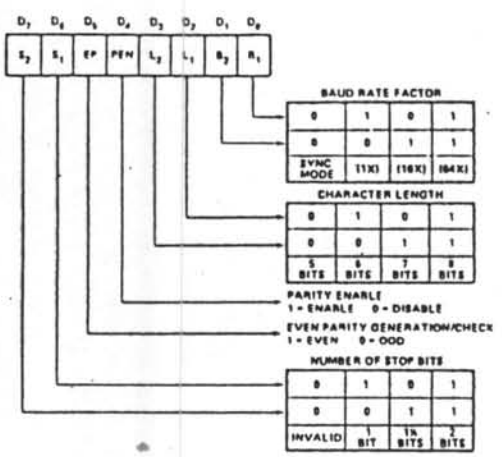
All control words written into the 8251 after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the 8251 at any time in the data block during the operation of the 8251. To return to the Mode Instruction format a bit in the Command Instruction word can be set to initiate an Internal Reset operation which automatically places the 8251 back into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters.



Typical Data Block

Mode Instruction Definition

The 8251 can be used for either Asynchronous or Synchronous data communication. To understand how the Mode Instruction defines the functional operation of the 8251 the designer can best view the device as two separate components sharing the same package. One Asynchronous the other Synchronous. The format definition can be changed "on the fly" but for explanation purposes the two formats will be isolated.



Mode Instruction Format, Asynchronous Mode

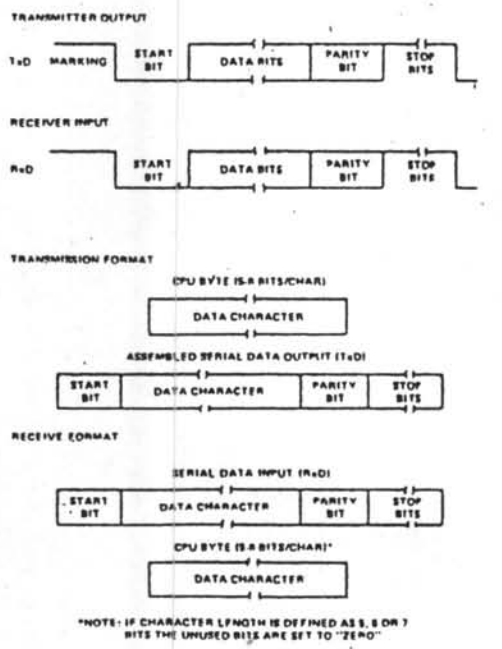
Asynchronous Mode (Transmission)

Whenever a data character is sent by the CPU the 8251 automatically adds a Start bit (low level) and the programmed number of Stop bits to each character. Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of $\overline{TxC}$ at a rate equal to 1, 1/16, or 1/64 that of the $\overline{TxC}$, as defined by the Mode Instruction. BREAK characters can be continuously sent to the TxD if commanded to do so.

When no data characters have loaded into the 8251 the TxD output remains "high" (marking) unless a Break (continuously low) has been programmed.

Asynchronous Mode (Receive)

The RxD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center. If a low is detected again, it is a valid START bit, and the bit counter will start counting. The bit counter locates the center of the data bits, the parity bit (if it exists) and the stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of $\overline{RxC}$. If a low level is detected as the STOP bit, the Framing Error flag will be set. The STOP bit signals the end of a character. This character is then loaded into the parallel I/O buffer of the 8251. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the OVERRUN flag is raised (thus the previous character is lost). All of the error flags can be reset by a command instruction. The occurrence of any of these errors will not stop the operation of the 8251.



Asynchronous Mode

Synchronous Mode (Transmission)

The TxD output is continuously high until the CPU sends its first character to the 8251 which usually is a SYNC character. When the $\overline{CTS}$ line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of $\overline{TxC}$. Data is shifted out at the same rate as the $\overline{TxC}$.

Once transmission has started, the data stream at TxD output must continue at the $\overline{TxC}$ rate. If the CPU does not provide the 8251 with a character before the 8251 becomes empty, the SYNC characters (or character if in single SYNC word mode) will be automatically inserted in the TxD data stream. In this case, the TxEMPTY pin is raised high to signal that the 8251 is empty and SYNC characters are being sent out. The TxEMPTY pin is internally reset by the next character being written into the 8251.

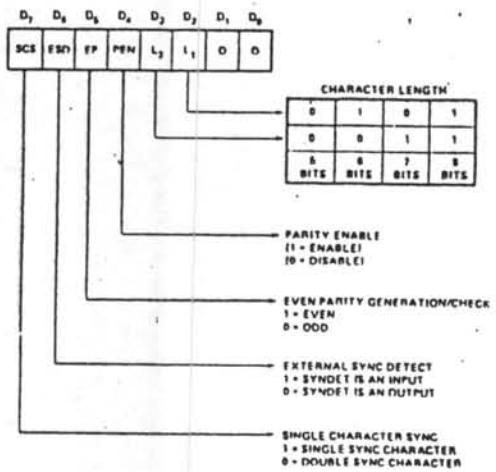
Synchronous Mode (Receive)

In this mode, character synchronization can be internally or externally achieved. If the internal SYNC mode has been programmed, the receiver starts in a HUNT mode. Data on the RxD pin is then sampled in on the rising edge of $\overline{RxC}$. The content of the Rx buffer is continuously compared with the first SYNC character until a match occurs. If the 8251 has been programmed for two SYNC characters, the subsequent received character is also compared; when both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a STATUS READ.

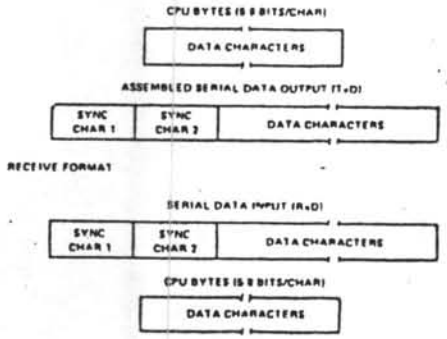
In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin. The high level can be removed after one $\overline{RxC}$ cycle.

Parity error and overrun error are both checked in the same way as in the Asynchronous Rx mode.

The CPU can command the receiver to enter the HUNT mode if synchronization is lost.



Mode Instruction Format, Synchronous Mode

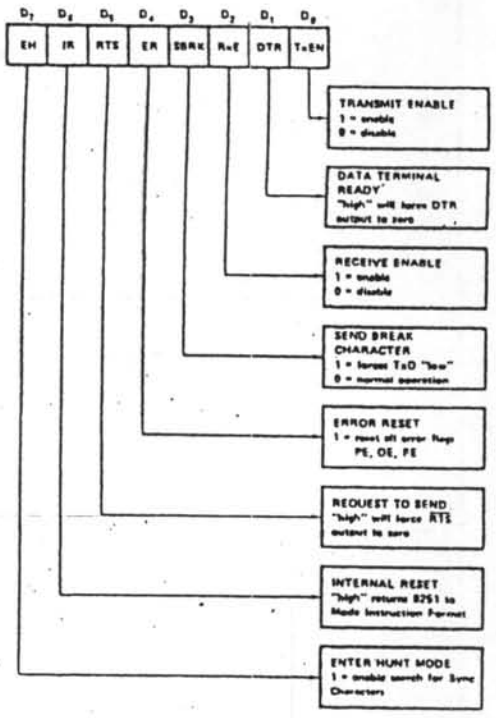


Synchronous Mode, Transmission Format

COMMAND INSTRUCTION DEFINITION

Once the functional definition of the 8251 has been programmed by the Mode Instruction and the Sync Characters are loaded (if in Sync Mode) then the device is ready to be used for data communication. The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset and Modem Controls are provided by the Command Instruction.

Once the Mode Instruction has been written into the 8251 and Sync characters inserted, if necessary, then all further "control writes" (C/$\overline{D}$ = 1) will load the Command Instruction. A Reset operation (internal or external) will return the 8251 to the Mode Instruction Format.



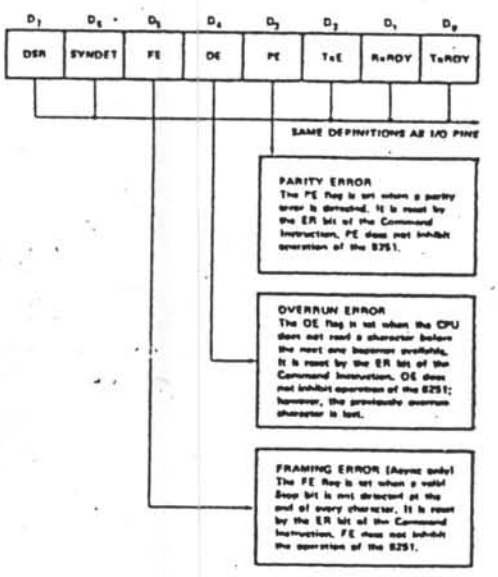
Command Instruction Format

STATUS READ DEFINITION

In data communication systems it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The 8251 has facilities that allow the programmer to "read" the status of the device at any time during the functional operation.

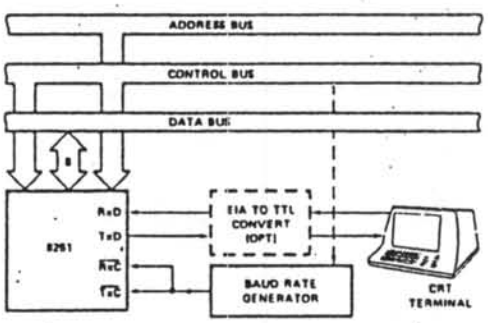
A normal "read" command is issued by the CPU with the C/D input at one to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins so that the 8251 can be used in a completely Polled environment or in an Interrupt driven environment.

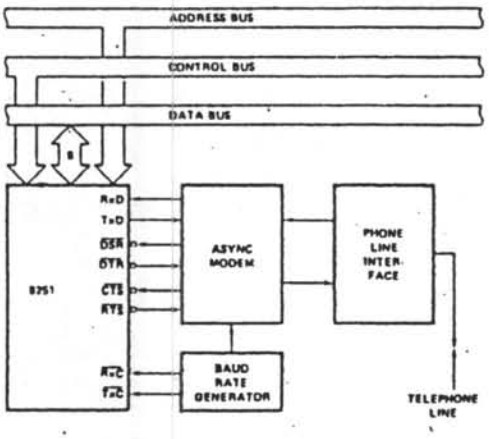


Status Read Format

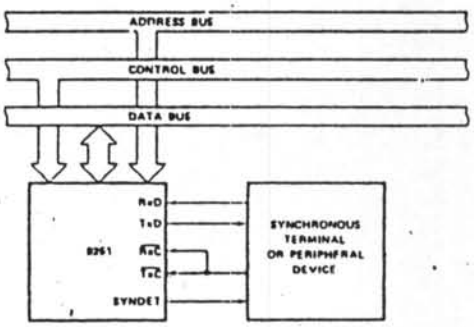
APPLICATIONS OF THE 8251



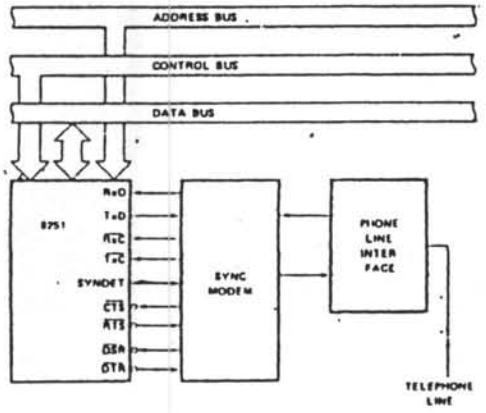
Asynchronous Serial Interface to CRT Terminal, DC-9600 Baud



Asynchronous Interface to Telephone Lines



ynchronous Interface to Terminal or Peripheral Device



Synchronous Interface to Telephone Lines

SILICON GATE MOS 8251

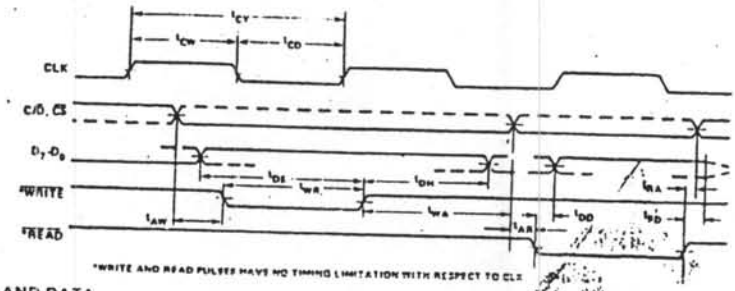
D.C. Characteristics: T_A = 0°C to 70°C; V_{CC} = +5V ±5%; V_{SS} = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage			.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			.4	V	I_{OL} = 2.0mA (DB_{0-7}), 1.6mA (Others)
V_{OH}	Output High Voltage	2.4			V	I_{OH} = 150μA (DB_{0-7}), 100μA (Others)
I_{CC}	Power Supply Current		80		mA	
I_{LI}	Input Load Current		10		μA	V_{IN} = 0V to 5.25V
I_{LOL}	Output Leakage Current (DB Low)		-100		μA	V_{OUT} = 0.4V
I_{LOH}	Output Leakage Current (DB High)		+10		μA	V_{OUT} = V_{CC}

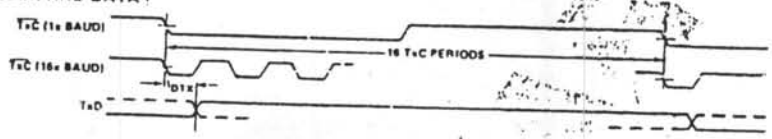
A.C. Characteristics: T_A = 0°C to 70°C; V_{CC} = +5V ±5%; V_{SS} = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{CY}	Clock Period	480			ns	
t_{CW}	Clock Pulse Width	220			ns	
t_{CD}	Clock Pulse Delay		260		ns	
t_R, t_F	Clock Rise and Fall Time		50		ns	
t_{WR}	Write Pulse Width	400			ns	
t_{DS}	Data Set-Up Time for $\overline{WRITE}$	300			ns	
t_{DH}	Data Hold Time for $\overline{WRITE}$	20			ns	
t_{DD}	Data Delay from $\overline{READ}$		350		ns	C_L = 150pF
t_{FD}	$\overline{READ}$ to Data Floating		160		ns	C_L = 150pF
t_{AW}	Address Stable before $\overline{WRITE}$	0			ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$		40		ns	
t_{AR}	Address Stable before $\overline{READ}$		0		ns	
t_{RA}	Address Hold Time for $\overline{READ}$		0		ns	
t_{DTx}	TxD Delay from Rising Edge of TxC		300		ns	
t_{SRx}	Rx Data Set-Up Time to Sampling Pulse		500		ns	
t_{HRx}	Rx Data Hold Time to Sampling Pulse		6		CLK Period	
f_{Tx}	Transmitter Input Clock Frequency 1X Baud Rate 16X and 64X Baud Rate		 56 615		 KHz KHz	
f_{Rx}	Receiver Input Clock Frequency 1X Baud Rate 16X and 64X Baud Rate		 56 615		 KHz KHz	
t_{Tx}	TxRDY Delay from Center of Data Bit		6		CLK Period	C_L = 50pF
t_{Rx}	RxRDY Delay from Center of Data Bit		6		CLK Period	
t_{IS}	Internal SYNDET Delay from Center of Data Bit		6		CLK Period	
t_{ES}	External SYNDET Set-Up Time before Rising Edge of RxC		6		CLK Period	

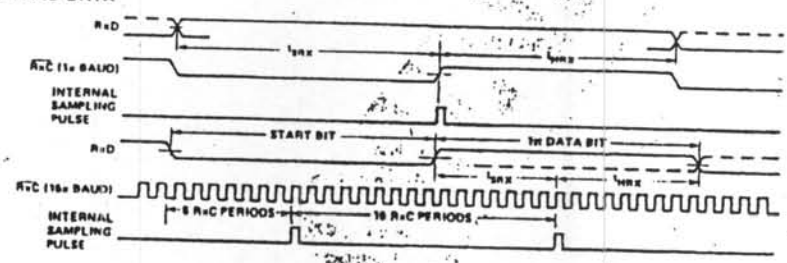
READ AND WRITE TIMING



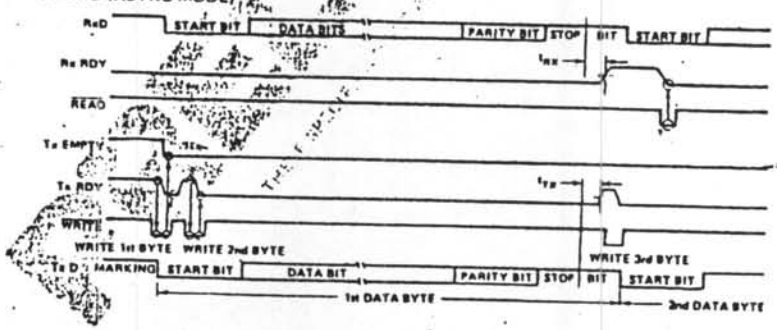
TRANSMITTER CLOCK AND DATA



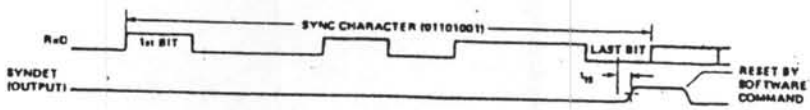
RECEIVER CLOCK AND DATA



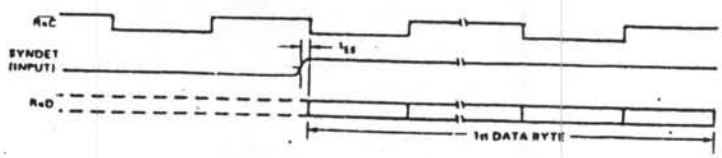
Tx RDY AND Rx RDY TIMING (ASYNC MODE)



INTERNAL SYNC DETECT



EXTERNAL SYNC DETECT



intel

2716*
16K (2K x 8) UV ERASABLE PROM

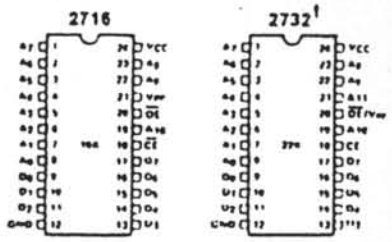
- Fast Access Time
  - 350 ns Max. 2716-1
  - 390 ns Max. 2716-2
  - 450 ns Max. 2716
  - 490 ns Max. 2716-5
  - 650 ns Max. 2716-6
- Single +5V Power Supply
- Low Power Dissipation
  - 525 mW Max. Active Power
  - 132 mW Max. Standby Power
- Pin Compatible to Intel® 2732 EPROM
- Simple Programming Requirements
  - Single Location Programming
  - Programs with One 50 ms Pulse
- Inputs and Outputs TTL Compatible during Read and Program
- Completely Static

The Intel™ 2716 is a 16,384-bit ultraviolet erasable and electrically programmable read-only memory (EPROM). The 2716 operates from a single 5-volt power supply, has a static standby mode, and features fast single address location programming. It makes designing with EPROMs faster, easier and more economical.

The 2716, with its single 5-volt supply and with an access time up to 350 ns, is ideal for use with the newer high performance +5V microprocessors such as Intel's 8085 and 8086. A selected 2716-5 and 2716-6 is available for slower speed applications. The 2716 is also the first EPROM with a static standby mode which reduces the power dissipation without increasing access time. The maximum active power dissipation is 525 mW while the maximum standby power dissipation is only 132 mW, a 75% savings.

The 2716 has the simplest and fastest method yet devised for programming EPROMs – single pulse TTL level programming. No need for high voltage pulsing because all programming controls are handled by TTL signals. Program any location at any time—either individually, sequentially or at random, with the 2716's single address location programming. Total programming time for all 16,384 bits is only 100 seconds.

PIN CONFIGURATION



†Refer to 2732 data sheet for specifications

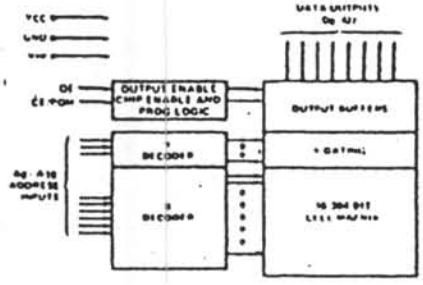
PIN NAMES

A_0 - A_{10}	ADDRESSES
$\overline{CE}$/PGM	CHIP ENABLE/PROGRAM
$\overline{OE}$	OUTPUT ENABLE
O_0 - O_7	OUTPUTS

MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM



*PART(S) ALSO AVAILABLE IN EXTENDED TEMPERATURE RANGE FOR MILITARY AND INDUSTRIAL GRADE APPLICATONS.

Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051.

PROGRAMMING

The programming specifications are described in the Data Catalog PROM/ROM Programming Instructions Section.

Absolute Maximum Ratings*

Temperature Under Bias	-10°C to +80°C
Storage Temperature	-65°C to +125°C
All Input or Output Voltages with Respect to Ground	+6V to -0.3V
V_{PP} Supply Voltage with Respect to Ground During Program	+26.5V to -0.3V

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Conditions During Read

	2716	2716-1	2716-2	2716-5	2716-6
Temperature Range	0°C – 70°C	0°C – 70°C	0°C – 70°C	0°C – 70°C	0°C – 70°C
V_{CC} Power Supply[1,2]	5V ±5%	5V ±10%	5V ±5%	5V ±5%	5V ±5%
V_{PP} Power Supply[2]	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}

READ OPERATION

D.C. and Operating Characteristics

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[3]	Max.		
I_{LI}	Input Load Current			10	μA	V_{IN} = 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 5.25V
I_{PP1}[2]	V_{PP} Current			5	mA	V_{PP} = 5.25V
I_{CC1}[2]	V_{CC} Current (Standby)		10	25	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}
I_{CC2}[2]	V_{CC} Current (Active)		57	100	mA	$\overline{OE}$ = $\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	-0.1		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -400 μA

NOTES: 1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for T_A = 25°C and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested.

A.C. Characteristics

Symbol	Parameter	Limits (ns)										Test Conditions
		2716		2716-1		2716-2		2716-5		2716-6		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address to Output Delay		450		350		390		450		450	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{CE}	$\overline{CE}$ to Output Delay		450		350		390		490		650	$\overline{OE}$ = V_{IL}
t_{OE}	Output Enable to Output Delay		120		120		120		160		200	$\overline{CE}$ = V_{IL}
t_{DF}	Output Enable High to Output Float	0	100	0	100	0	100	0	100	0	100	$\overline{CE}$ = V_{IL}
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		0		0		$\overline{CE}$ = $\overline{OE}$ = V_{IL}

A.C. Characteristics

Symbol	Parameter	Limits (ns)										Test Conditions
		2716		2716-1		2716-2		2716-5		2716-6		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{ACC}	Address to Output Delay		450		350		390		450		450	$\overline{CE} = \overline{OE} = V_{IL}$
t_{CE}	$\overline{CE}$ to Output Delay		450		350		390		490		650	$\overline{OE} = V_{IL}$
t_{OE}	Output Enable to Output Delay		120		120		120		160		200	$\overline{CE} = V_{IL}$
t_{DF}	Output Enable High to Output Float	0	100	0	100	0	100	0	100	0	100	$\overline{CE} = V_{IL}$
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	0		0		0		0		0		$\overline{CE} = \overline{OE} = V_{IL}$

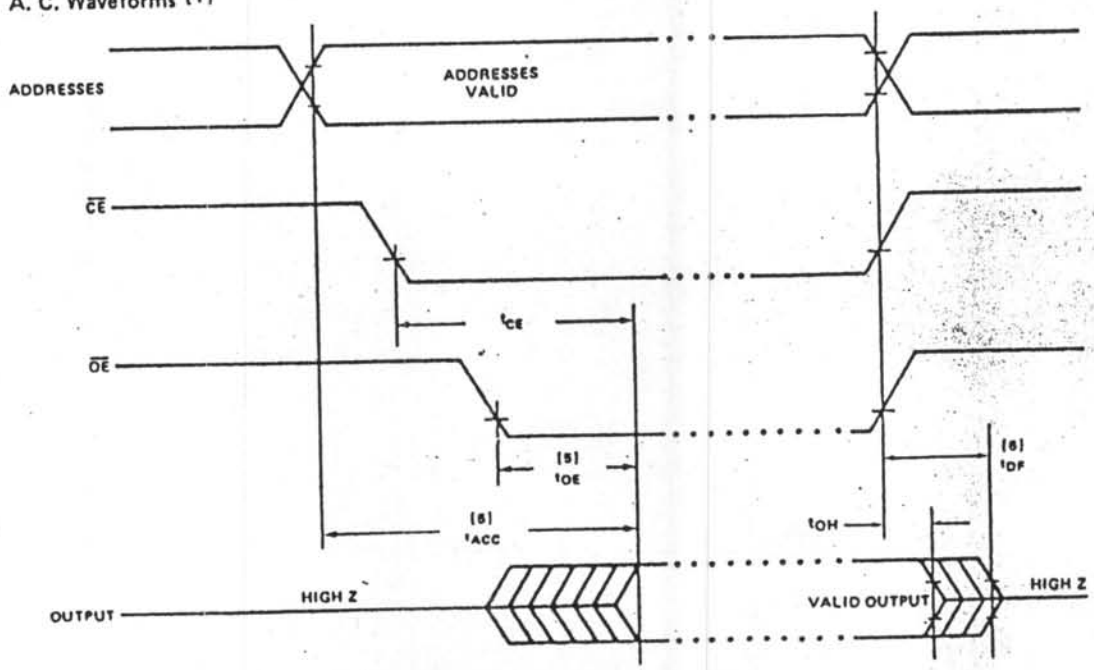
Capacitance [4] $T_A = 25°C$, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit	Conditions
C_{IN}	Input Capacitance	4	6	pF	$V_{IN} = 0V$
C_{OUT}	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

A.C. Test Conditions:

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

A. C. Waveforms [1]



NOTE:
1. V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after Vpp.
2. Vpp may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_A = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and is not 100% tested.
5. This parameter is only sampled and is not 100% tested.
6. OE may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of CE without impact on t_{ACC}.
7. t_{DF} is specified from OE or CE, whichever occurs first.

ERASURE CHARACTERISTICS

The erasure characteristics of the 2716 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000—4000Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical 2716 in approximately 3 years, while it would take approximatley 1 week to cause erasure when exposed to direct sunlight. If the 2716 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels are available from Intel which should be placed over the 2716 window to prevent unintentional erasure.

The recommended erasure procedure (see Data Catalog PROM/ROM Programming Instruction Section) for the 2716 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 μW/cm^2 power rating. The 2716 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

DEVICE OPERATION

The five modes of operation of the 2716 are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are a +5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other two modes.

TABLE I. MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

READ MODE

The 2716 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs 120 ns (t_{OE}) after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 2716 has a standby mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. The 2716 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedence state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

Because 2716's are usually used in larger memory arrays, Intel has provided a 2 line control function that accomodates this use of multiple memory connections. The two line control function allows for:

a) the lowest possible memory power dissipation, and
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAMMING (See Programming Instruction Section for Waveforms.)

Initially, and after each erasure, all bits of the 2716 are in the "1" state. Data is introduced by selectively programming "0's" into the desired bit locations. Although only "0's" will be programmed, both "1's" and "0's" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The 2716 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 msec. active high, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time — either individually, sequentially, or at random. The program pulse has a maximum width of 55 msec. The 2716 must not be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Programming of multiple 2716s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled 2716s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$/PGM input programs the paralleled 2716s.

PROGRAM INHIBIT

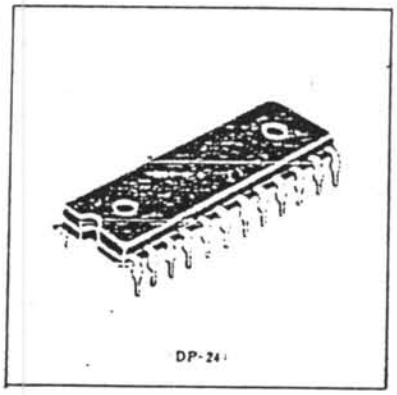
Programming of multiple 2716s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel 2716s may be common. A TTL level program pulse applied to a 2716's $\overline{CE}$/PGM input with V_{PP} at 25V will program that 2716. A low level $\overline{CE}$/PGM input inhibits the other 2716 from being programmed.

PROGRAM VERIFY

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify may be performed wth V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at 5V.

HM6116LP-2
HM6116LP-3, HM6116LP-4

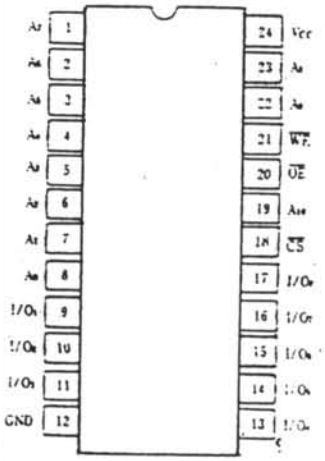
2048-word×8-bit High Speed Static CMOS RAM



■特長

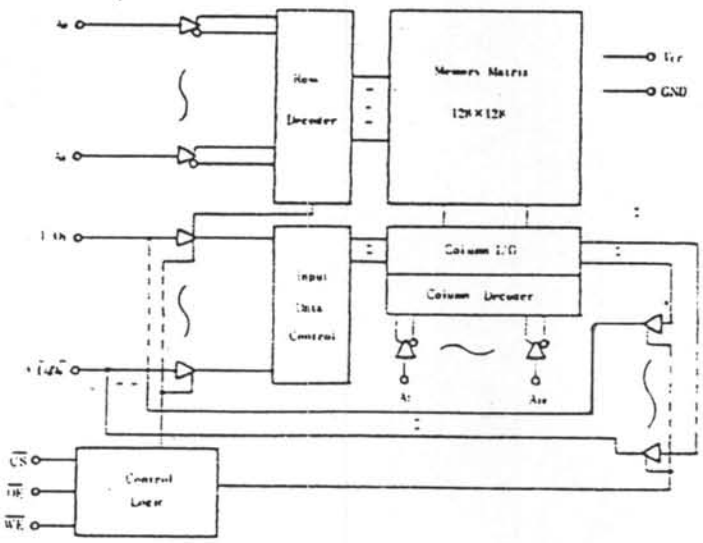
○5V単一電源です。
○高速です。
　アクセス時間　HM6116LP-2……120ns(max)
　　HM6116LP-3……150ns(max)
　　HM6116LP-4……200ns(max)
○低消費電力です。
　スタンバイ時　20μW (typ)
　動作時　160mW(typ)
○完全なスタティックメモリです。
　クロック，タイミングストローブを必要としません。
○全ての入，出力がTTLコンパチブルです。
○アクセスとサイクル時間が同じです。
○バッテリバックアップ動作が可能です。
○ピン配置が標準16K EPROM/マスクROMコンパチブルです。

■ピン配置



(上面図)

■ブロックダイアグラム

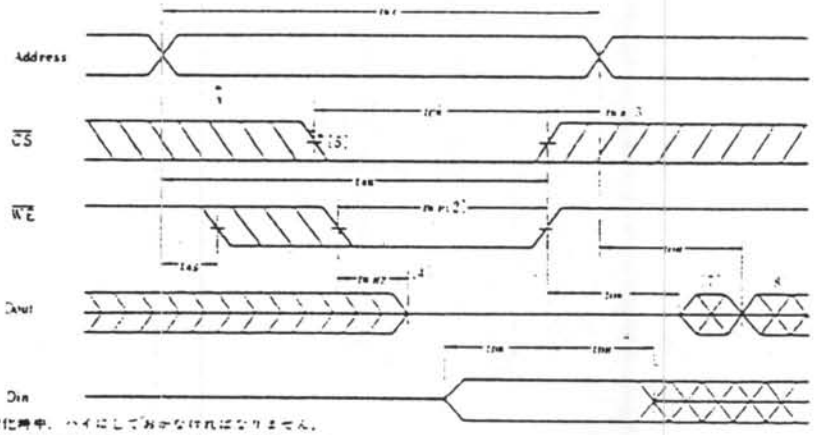


■絶対最大定格

項目	記号	定格値	単位
端子電圧*	V_T	−0.5〜+7.0	V
許容損失	P_T	1.0	W
動作温度	T_{opr}	0〜+70	℃
保存温度(バイアス印加時)	T_{bias}	−10〜+85	℃
保存温度	T_{stg}	−55〜+125	℃

*GNDに対しての値

ライトサイクル(2) 注) 1, 6



注) 1. WEはアドレス変化期中、ハイにしておかなければなりません。
2. 書込みはCS、WEが共にLのオーバラップ期間twに行われます。
3. twはCSまたはWEのいずれか早い立上りパルスからwcの時間で決定します。
4. I/O端子が出力状態にある場合、出力に対して逆位相の入力信号を印加してはなりません。
5. CSのLの遷移がWEのL遷移あるいはWE遷移に同じに生じる場合、出力は低インピーダンス状態にとどまります。
6. OEは常にHです。OE = V_{IH}
7. Doutはこのサイトーイクルの書込みデータと同位相です。
8. Doutは次のアドレスの読出しデータです。
9. CSがこの期間中Lの場合、I/O端子は出力状態になります。この時出力に対して逆位相のデータ入力信号を印加してはなりません。

■容量(Ta=25℃, f=1MHz)

項目	記号	測定条件	typ	max	単位
入力容量	C_{in}	V_{in}=0V	3	5	pF
I/O端子容量	$C_{I/O}$	$V_{I/O}$=0V	5	7	pF

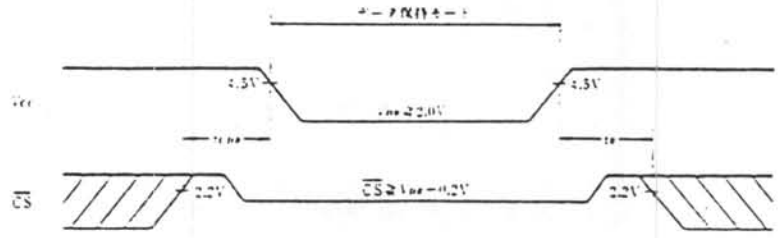
注) このパラメータは全品測定されたものではなく、サンプル検査です。

■低電源電圧時データ保持特性(Ta=0～+70℃)

項目	記号	測定条件	min	typ	max	単位
データ保持電源電圧	V_{DR}	$\overline{CS} \geq V_{CC}-0.2V$, $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$	2.0	—	—	V
データ保持電流	I_{CCDR}	V_{CC}=3.0V, $\overline{CS} \geq 2.8V$, $V_{IN} \geq 2.8V$ or $V_{IN} \leq 0.2V$	—	—	50	μA
チップセレクトデータ保持時間	t_{CDR}	下図参照	0	—	—	ns
動作回復時間	t_R		* t_{RC}	—	—	ns

* t_{RC} = リードサイクル時間

● 低電源電圧データ保持波形



●ライトサイクル

項目		記号	HM6116LP-2		HM6116LP-3		HM6116LP-4		単位
			min	max	min	max	min	max	
ライト	サイクル時間	t_{WC}	120	—	150	—	200	—	ns
ライト	実効時間	t_{CW}	70	—	90	—	120	—	ns
チップ	選択動作時間	t_{AW}	105	—	120	—	140	—	ns
アドレス	セットアップ時間	t_{AS}	20	—	20	—	20	—	ns
ライト	パルス幅	t_{WP}	70	—	90	—	120	—	ns
アドレス	保持時間	t_{WR}	5	—	10	—	10	—	ns
出力ディスエーブル	イネーブル・出力遅延時間	t_{OWZ}	0	40	0	50	0	60	ns
$\overline{WE}$・出力	フローティング	t_{WHZ}	0	50	0	60	0	60	ns
入力データ	セットアップ時間	t_{DW}	35	—	40	—	60	—	ns
入力データ	保持時間	t_{DH}	5	—	10	—	10	—	ns
$\overline{WE}$・出力	セットアップ時間	t_{OW}	5	—	10	—	10	—	ns

■タイミング波形

●リードサイクル(1

注) 1, 5

●リードサイクル(2

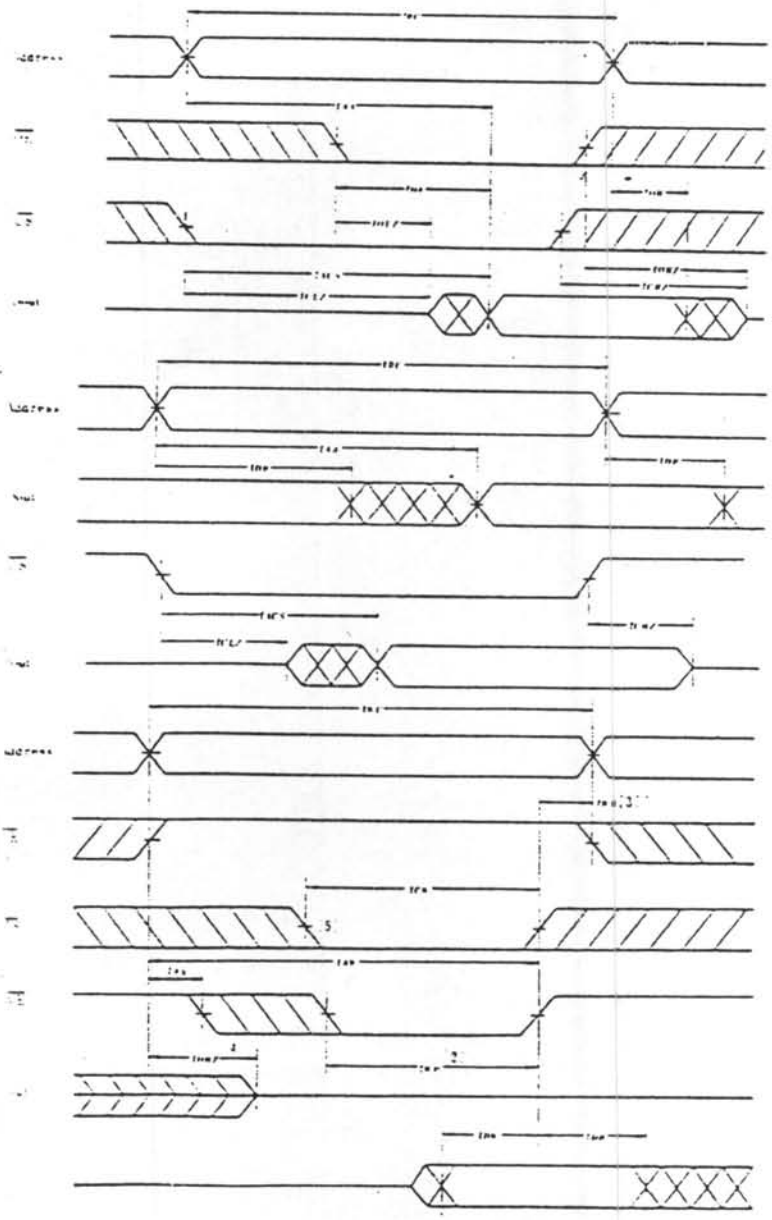
注) 1, 2, 4, 5

●リードサイクル(3

注) 1, 3, 4, 5

●ライトサイクル(1

注) 1



注: 1. $\overline{WE}$ はリードサイクル時ハイレベルにしておく。
2. $\overline{CS}$ = V_{IL}
3. アドレスは $\overline{CS}$ の立下がりと同時、あるいは先行して確定する。
4. $\overline{OE}$ = V_{IL}
5. $\overline{CS}$ が立下がり時、アドレス入力は高インピーダンス状態にしてはならない。

■機能表

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	モード	電源電流	I/O端子	参照サイクル
H	X	X	非選択時	I_{SB}, I_{SB1}	高インピーダンス	リードサイクル(1)~(3)
L	L	H	リード	I_{CC}	Dout	ライトサイクル(1)~(3)
L	H	L	ライト	I_{CC}	Din	ライトサイクル(1)
L	L	L	ライト	I_{CC}	Din	ライトサイクル(2)

■推奨DC動作条件 (Ta=0~+70℃)

項目	記号	min	typ	max	単位
電源電圧	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
入力電圧	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	−1.0*	—	0.8	V

* パルス幅：50 ns, DC：V_{IL} min=−0.3V

■DCおよび動作特性 (V_{CC}=5V±10%, GND=0V, Ta=0~+70℃)

項目	記号	測定条件	HM6116LP-2 min	HM6116LP-2 typ*	HM6116LP-2 max	HM6116LP-3/-4 min	HM6116LP-3/-4 typ*	HM6116LP-3/-4 max	単位
入力漏洩電流	I_{LI}	V_{CC}=5.5V, V_{IN}=GND to V_{CC}	—	—	2	—	—	2	μA
出力漏洩電流	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=GND to V_{CC}	—	—	2	—	—	2	μA
動作時電源電流	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	—	35	70	—	30	60	mA
	I_{CC1}**	V_{IN}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA	—	30	—	—	25	—	mA
平均動作電流	I_{CC2}	最小サイクル, duty=100%	—	35	70	—	30	60	mA
スタンバイ時電源電流	I_{SB}	$\overline{CS}$=V_{IH}	—	4	12	—	4	12	mA
	I_{SB1}	$\overline{CS}$≧V_{CC}−0.2V, V_{IN}≧V_{CC}−0.2V or V_{IN}≦0.2V	—	4	100	—	4	100	μA
出力電圧	V_{OL}	I_{OL}=4mA	—	—	0.4	—	—	—	V
		I_{OL}=2.1mA	—	—	—	—	—	0.4	V
	V_{OH}	I_{OH}=−1.0mA	2.4	—	—	2.4	—	—	V

* V_{CC}=5.0V, Ta=25℃における参考値
** 参考値

■AC特性 (V_{CC}=5V±10%, Ta=0~+70℃)

●AC特性測定条件

○入力パルスレベル：0.8~2.4 V
○入力上昇/下降時間：10 ns
○入、出力タイミング参照レベル：1.5 V
○出荷負荷：1 TTLゲート+C_L=100 pF
(スコープ、ジグ容量を含む)

●リードサイクル

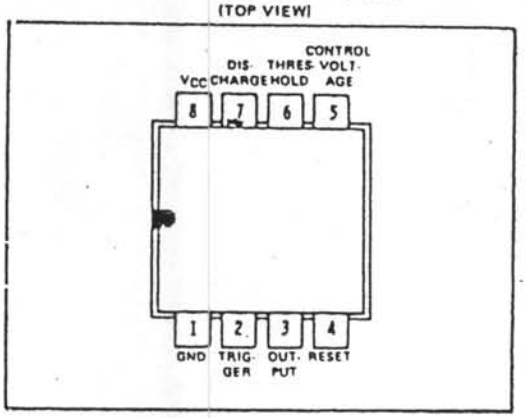
項目	記号	HM6116LP-2 min	HM6116LP-2 max	HM6116LP-3 min	HM6116LP-3 max	HM6116LP-4 min	HM6116LP-4 max	単位
リードサイクル時間	t_{RC}	120	—	150	—	200	—	ns
アドレスアクセス時間	t_{AA}	—	120	—	150	—	200	ns
チップセレクトアクセス時間	t_{ACS}	—	120	—	150	—	200	ns
$\overline{CS}$・出力セット時間	t_{CLZ}	10	—	15	—	15	—	ns
出力イネーブル・出力遅延時間	t_{OE}	—	80	—	100	—	120	ns
出力イネーブル・出力遅延時間(低インピーダンス時)	t_{OLZ}	10	—	15	—	15	—	ns
$\overline{CS}$・出力フローティング	t_{CHZ}	0	40	0	50	0	60	ns
出力ディスエイブル・出力遅延時間	t_{OHZ}	0	40	0	50	0	60	ns
出力保持時間	t_{OH}	10	—	15	—	15	—	ns

TYPES SN52555, SN72555
PRECISION TIMERS

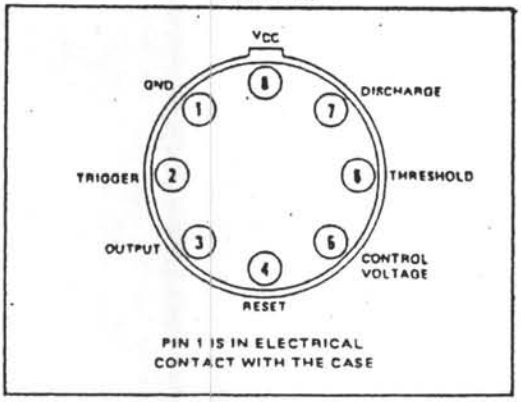
BULLETIN NO. DL-S 7312053, SEPTEMBER 1973

- Timing from Microseconds to Hours
- Astable or Monostable Operation
- Adjustable Duty Cycle
- Up to 200-mA Sink or Source Output Current
- TTL Compatible Output
- Designed to be Interchangeable with Signetics SE555/NE555

JP OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



L PLUG-IN PACKAGE
(TOP VIEW)



PIN 1 IS IN ELECTRICAL CONTACT WITH THE CASE

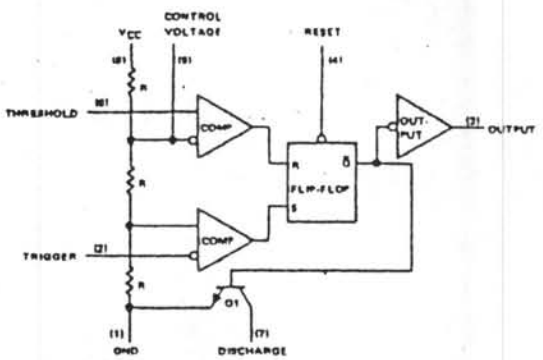
description

The SN52555 and SN72555 are monolithic timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle may be independently controlled with two external resistors and a single external capacitor.

The threshold and trigger levels are normally two-thirds and one-third, respectively, of V_{CC}. These levels can be altered by use of the control voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. When the threshold input rises above the threshold level, the flip-flop is reset and the output goes low. The reset input can override all other inputs and can be used to initiate a new timing cycle. When the reset input goes low, the flip-flop is reset and the output goes low. When the output is low, a low-impedance path is provided between the discharge terminal and ground.

The output circuit is capable of sinking or sourcing current up to 200 milliamperes. Operation is specified for supplies of 5 to 15 volts. With a 5-volt supply, output levels are compatible with TTL inputs.

functional block diagram



electrical characteristics at 25°C free-air temperature, V_{CC} = 5 V to 15 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN52555			SN72555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Threshold voltage level as a percentage of supply voltage				66.7			66.7		%
Threshold current (see Note 3)				0.1	0.25		0.1	0.25	μA
Trigger voltage level	V_{CC} = 15 V		4.8	5	5.2		5		V
	V_{CC} = 5 V		1.45	1.67	1.9		1.67		
Trigger current				0.5			0.5		μA
Reset voltage level			0.4	0.7	1	0.4	0.7	1	V
Reset current				0.1			0.1		mA
Control voltage (open-circuit)	V_{CC} = 15 V		9.6	10	10.4	9	10	11	V
	V_{CC} = 5 V		2.9	3.3	3.8	2.6	3.3	4	
Low-level output voltage	V_{CC} = 15 V	I_{OL} = 10 mA		0.1	0.15		0.1	0.25	V
		I_{OL} = 50 mA		0.4	0.5		0.4	0.75	
		I_{OL} = 100 mA		2	2.2		2	2.5	
		I_{OL} = 200 mA		2.5			2.5		
	V_{CC} = 5 V	I_{OL} = 5 mA		0.1	0.25				
		I_{OL} = 8 mA					0.16	0.35	
High-level output voltage	V_{CC} = 15 V	I_{OH} = −100 mA	13	13.3		12.75	13.3		V
		I_{OH} = −200 mA		12.5			12.5		
	V_{CC} = 5 V	I_{OH} = −100 mA	3	3.3		2.75	3.3		
Supply current	Output low, No load	V_{CC} = 15 V		10	12		10	15	mA
		V_{CC} = 5 V		3	5		3	6	
	Output high, No load	V_{CC} = 15 V		9	11		9	14	
		V_{CC} = 5 V		2	4		2	5	

NOTE 3: This parameter influences the maximum value of the timing resistors R_A and R_B. For example when V_{CC} = 5 V the maximum value is $R = R_A + R_B = 20\ M\Omega$.

operating characteristics, V_{CC} = 5 V and 15 V

PARAMETER	TEST CONDITIONS†		SN52555			SN72555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial accuracy of timing interval	R_A = 1 kΩ to 100 kΩ,	T_A = 25°C		0.5	2		1		%
Temperature coefficient of timing interval	R_B = 0 to 100 kΩ,	T_A = MIN to MAX		30			50		ppm/°C
Supply voltage sensitivity of timing interval	C = 0.1 μF	T_A = 25°C		0.005	0.02		0.01		%/V
Output pulse rise time	C_L = 15 pF,	T_A = 25°C		100			100		ns
Output pulse fall time				100			100		ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

THERMAL INFORMATION

DISSIPATION DERATING CURVE

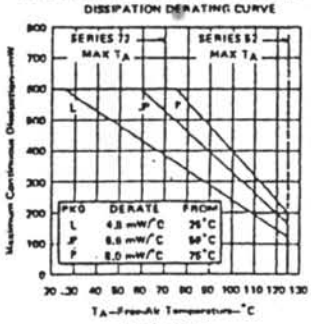
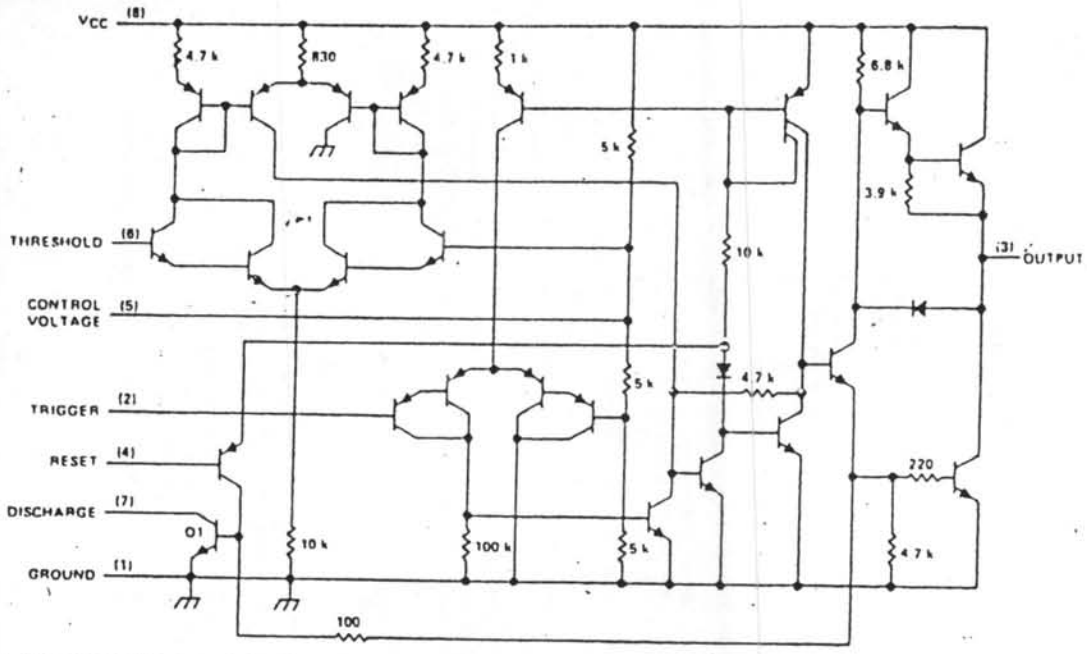


FIGURE 1

schematic



Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	18 V
Input voltage (control voltage, reset, threshold, trigger)	V_{CC}
Output current	±225 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	600 mW
Operating free-air temperature range: SN52555	−55°C to 125°C
SN72555	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JP or L package	300°C
Lead temperature 1/16 inch from case for 10 seconds: P package	260°C

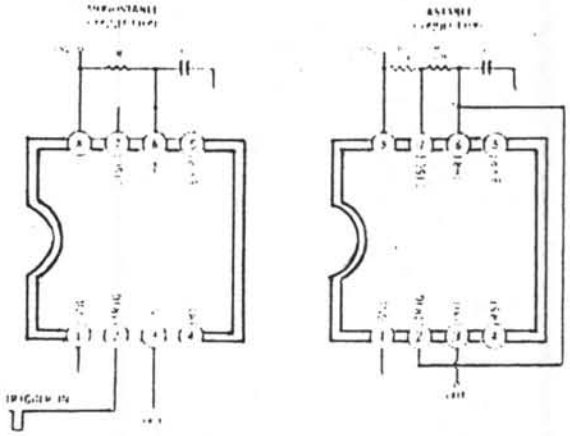
NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curve, Figure 1.

recommended operating conditions

	SN52555			SN72556			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5		18	4.5		18	V
Input voltage, V_I (control voltage, reset, threshold, trigger)			V_{CC}			V_{CC}	V
Output Current, I_O			±200			±200	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

555

TIMER—ASTABLE OR MONOSTABLE



This circuit may be used for astable or monostable in timing applications from microseconds to hours. Complete details for its use appear in Chapter 4.

As a monostable, the circuit is triggered by bringing the Trigger input momentarily below 2 volts. The output pulse width is determined by R and C, and the curves are shown in Fig. 4-26. R can vary from 1K to 3.3 megohms. C can range from 500 pF up. TTL fan-out is more than ten.

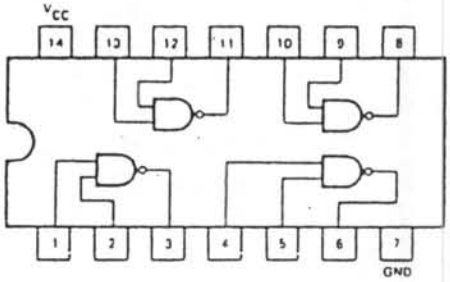
As an astable, the circuit is free running. The charging time is determined by R_a and R_b in series with C. The discharging time is determined by C and R_b. Design curves appear in Fig. 4-16. The minimum value of R_a is 1K; the maximum value of $R_a + R_b$ is 3.3 megohms. TTL fan-out is more than ten.

The RST input (pin 4) will drive the output low if it is grounded. If unused, it should be tied to +5 volts. The Bypass input should be bypassed to ground with a suitable capacitor (0.1 μF upward) in critical timing applications.

The output is high during the monostable on time and low otherwise. The output is high during the astable charging time and low during the discharge time.

Operating current . . . . . 3 milliamperes

QUAD 2-INPUT NAND GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS00X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS00X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type: W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

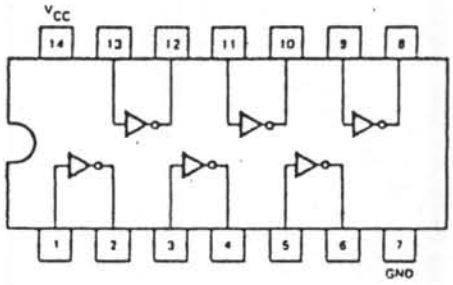
SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			0.8	1.6	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			2.4	4.4	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output		5.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		5.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

HEX INVERTER



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS04X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS04X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type: W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS (Note 1)
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IL}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = 2.0 V
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = 2.0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			1.2	2.4	mA	V_{CC} = MAX, V_{IN} = 0 V
I_{CCL}	Supply Current LOW			3.6	6.6	mA	V_{CC} = MAX, Inputs Open

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Turn Off Delay, Input to Output		5.0	10	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output		5.0	10	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

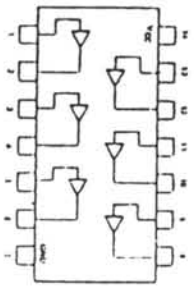
HEX BUFFER/DRIVER — 54/7407

SPEED/PACKAGE AVAILABILITY

54 F,W 74 A,F

PIN CONFIGURATION

A,F,W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L = 15pF, R_L = 110Ω			UNIT
PARAMETER	MIN	TYP	MAX	
Propagation delay time				
t_{PLH} Low-to-high		6	10	ns
t_{PHL} High-to-low		20	30	ns

Load circuit and typical waveforms are shown at the front of section

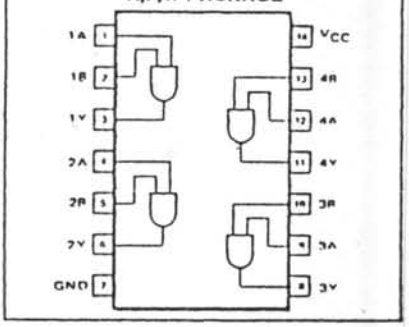
QUAD 2-INPUT AND GATE — 54/7408

SPEED/PACKAGE AVAILABILITY

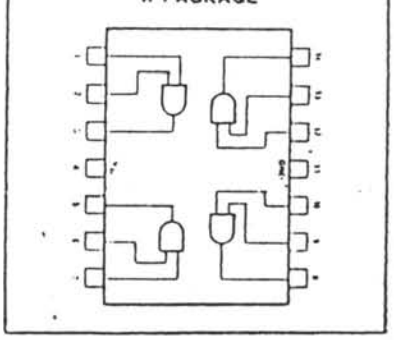
54	F,W	74	A,F
54H	F,W	74H	A,F
54LS	F,W	74LS	A,F
54S	F,W	74S	A,F

PIN CONFIGURATION

54/74,74H,54/74LS, 54/74S
A,F,W PACKAGE



54H
W PACKAGE

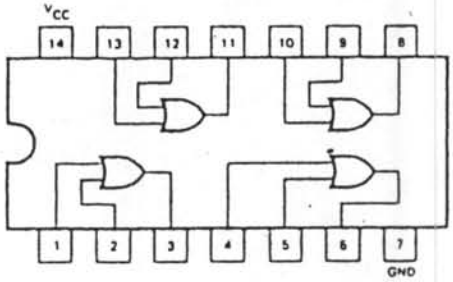


SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS	54/74 C_L = 15pF, R_L = 400Ω			54/74H C_L = 25pF, R_L = 280Ω			54/74LS C_L = 15pF, R_L = 2kΩ			54/74S C_L = 15pF, R_L = 280Ω			UNIT
PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation delay time													
t_{PLH} Low-to-high		17.5	27		7.6	12		8.5	15		4.5 (C_L = 50pF: 6)	7	ns
t_{PHL} High-to-low		12	19		8.8	12		8	20		5 (C_L = 50pF: 7.5)	7.5	ns

Load circuit and typical waveforms are shown at the front of section

QUAD 2-INPUT OR GATE



GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS32X	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS32X	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type: W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS (Note 1)
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH}
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	V_{CC} = MIN, I_{OL} = 4.0 mA, V_{IN} = V_{IL}
		74		0.35	0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA, V_{IN} = V_{IL}
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 3)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CCH}	Supply Current HIGH			3.1	6.2	mA	V_{CC} = MAX, Inputs Open
I_{CCL}	Supply Current LOW			4.9	9.8	mA	V_{CC} = MAX, V_{IN} = 0 V

AC CHARACTERISTICS: T_A = 25°C (See Chapter 1 for Waveforms)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH}	Turn Off Delay, Input to Output	3.0	7.0	11	ns	V_{CC} = 5.0 V
t_{PHL}	Turn On Delay, Input to Output	3.0	7.0	11	ns	C_L = 15 pF

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

SN54LS42/SN74LS42

ONE-OF-TEN DECODER

DESCRIPTION – The LSTTL/MSI SN54LS42/SN74LS42 is a Multipurpose Decoder designed to accept four BCD inputs and provide ten mutually exclusive outputs. The LS42 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

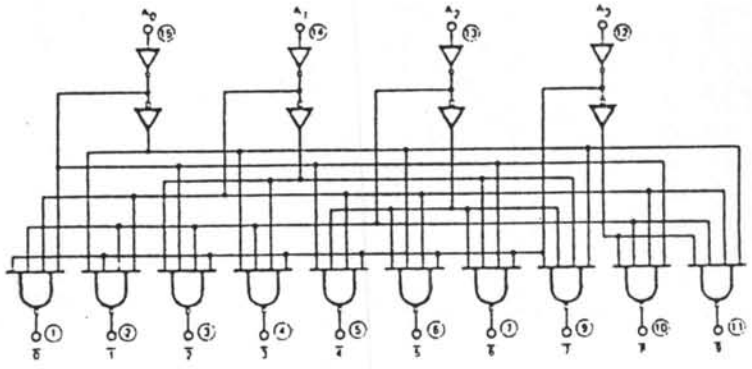
- MULTI-FUNCTION CAPABILITY
- MUTUALLY EXCLUSIVE OUTPUTS
- DEMULTIPLEXING CAPABILITY
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$A_0 - A_3$	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{0}$ to $\overline{9}$	Outputs, Active LOW (Note b)	10 U.L.	5(2.5) U.L.

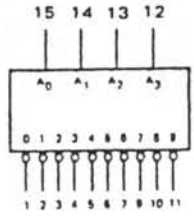
NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION – The LS42 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with active LOW input enables.

The logic design of the LS42 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input A_3 produces a useful inhibit function when the LS42 is used as a one-of-eight decoder. The A_3 input can also be used as the Data input in an 8-output demultiplexer application.

TRUTH TABLE

A_0	A_1	A_2	A_3	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +15 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5 V
Output Current (dc) (Output LOW)	+50 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
SN54LS42X	4.5 V	5.0 V	5.5 V	−55°C to +125°C
SN74LS42X	4.75 V	5.0 V	5.25 V	0°C to +70°C

X = package type: W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Threshold Voltage for All Inputs
		74			0.8		
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.4		V	V_{CC} = MIN, I_{OH} = −400 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.4			
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = MIN, V_{IN} = V_{IH} or
		74		0.35	0.5	V	I_{OL} = 8.0 mA; V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current (Note 4)		−15		−100	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			7.0	12	mA	V_{CC} = MAX

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
4. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay (2 Levels)		11 18	18 25	ns	Fig. 2	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay (3 Levels)		12 19	20 27	ns	Fig. 1	

AC WAVEFORMS

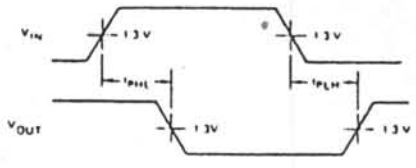


Fig. 1

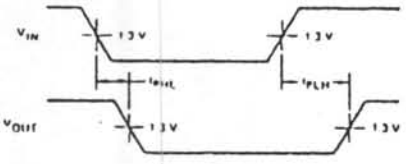


Fig. 2

COMPUTER AND TERMINAL INTERFACE

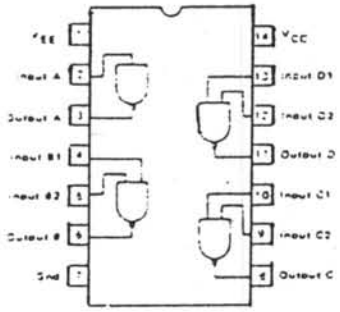
LINE DRIVERS AND RECEIVERS
for Modem/Terminal Applications

Voltage Mode

RS-232C SPECIFICATION

DRIVER

MC1488 – Quad; output current limiting.

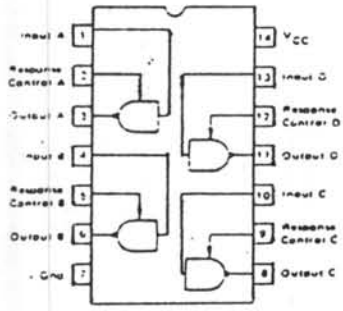


All devices:
T_A = 0 to 70°C
Package:
L Suffix – Case 632

V_{OH} @ V_{CC}/V_{EE} = +9.0 V Volts Min	V_{OL} @ V_{CC}/V_{EE} = +9.0 V Volts Max	I_{OS} mA	t_{PHL} @ C_L = 15 pF ns Max
5.0	-5.0	+6.0 to 12	175

RECEIVERS

MC1489 – Quad; 0.25 V input hysteresis.
MC1489A – Quad; 1.1 V input hysteresis.

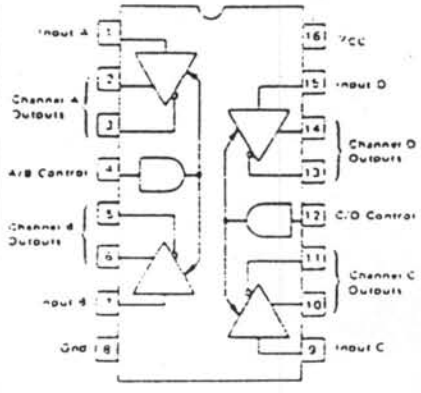


Device Number	Input V_{IHL} Volts	Input V_{ILH} Volts	t_{PHL} @ R_L = 390 Ω ns Max
MC1489	1.0 to 1.5	0.75 to 1.25	50
MC1489A	1.75 to 2.25	0.75 to 1.25	50

RS-422/423 SPECIFICATION

DRIVER

MC3487 – Quad; three-state outputs.

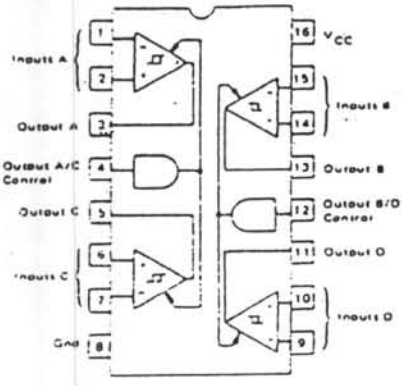


Both devices:
T_A = 0 to 70°C
Packages:
L Suffix – Case 620
P Suffix – Case 648

V_{OH} @ I_{OH} = 50 mA Volts Min	V_{OL} @ I_{OL} = 48 mA Volts Max	V_{OD}(Differential) @ R_L = 100 Ω Volts Min	t_{PLH}/t_{PHL} ns Typ
2.0	0.5	2.0	15

RECEIVER

MC3486 – Quad; three-state outputs and input hysteresis.



$V_{TH(D)}$ @ V_{ICM} = +7.0 V Volts Max	I_{ID} @ V_{ID} = +10 V V_{CC} = 0 to 5.25 V mA Max	t_{PHL}/t_{PLH} ns Typ	$t_{P(Control)}$ ns Typ
0.2	+3.25	20/25	25

Advance Information

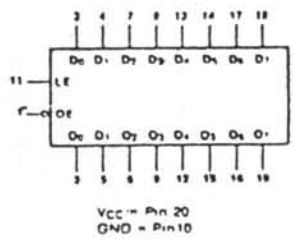
SN54LS373/SN74LS373

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS

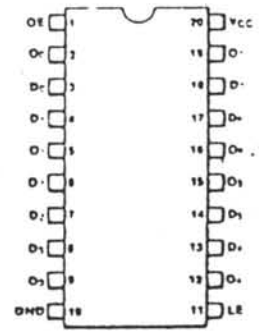
DESCRIPTION — The 54LS/74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the set-up times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedence state.

- EIGHT LATCHES IN A SINGLE PACKAGE
- 3-STATE OUTPUTS FOR BUS INTERFACING
- HYSTERESIS ON LATCH ENABLE
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY CMOS AND TTL COMPATABLE

LOGIC SYMBOL



CONNECTION DIAGRAM
DIP (TOP VIEW)

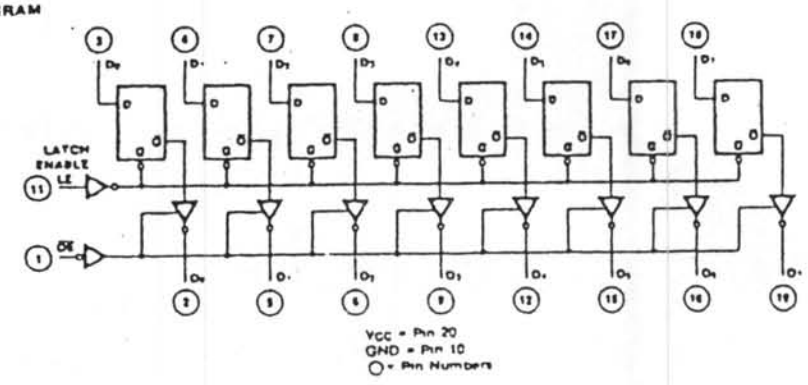


PIN NAMES		LOADING (Note a)	
		HIGH	LOW
D_0 - D_7	Data Inputs	0.5 U.L.	0.25 U.L.
LE	Latch Enable (Active HIGH) input	0.5 U.L.	0.25 U.L.
$\overline{OE}$	Output Enable (Active LOW) input	0.5 U.L.	0.25 U.L.
O_0 - O_7	Outputs (Note b)	65 (25) U.L.	15 (7.5) U.L.

NOTES
a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

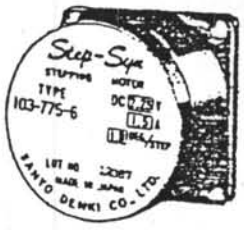
b) The Output LOW drive factor is 7.5 U.L. for Military and 25 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



(1) STEPPING MOTOR

	MODEL NUMBER	STEP ANGLE (DEG)	EXCITING METHOD	VOLT (V)	CURRENT (A/φ)	HOLDING TORQUE (kg-cm)	ROTOR INERTIA (kg-cm²)	WEIGHT (kg)	DRIVE UNIT Fig	E	C	R
	103-775-6	1.8	2/1-2	2.25	1.5	1.7	0.057	0.38	1	24	1	—
	103-770-1	1.8	2/1-2	5.1	1.0	4.3	0.105	0.57	1	24	2	—
	103-770-2	1.8	2/1-2	1.3	3.9	4.3	0.105	0.57	1	24	1	—
	103-770-3	1.8	2/1-2	24	0.22	4.3	0.105	0.57				
	103z708-4	1.8	2/1-2	12	0.7	3.9	0.105	0.57	1	12	0.3	—
	103z708-5	1.8	2/1-2	6	1.2	3.6	0.105	0.57	1	24	1	—
	103z710-1	1.8	2/1-2	5.4	1.5	6	0.220	1.1	1	24	2	—
	103z710-2	1.8	2/1-2	3	2.7	6	0.220	1.1	1	24	2	—
	103-721-1	5	2/1-2	5.4	1.5	3	0.210	1.1	1	24	3	—
	103-715-1	1.8	2/1-2	4.7	1.8	8	0.220	1.1	1	24	2	—
	103-715-2	1.8	2/1-2	1.7	4.7	8	0.220	1.1	1	24	2	—
	103-746-1	1.8	2/1-2	3.4	2.9	10.8	0.322	1.35	1	24	2	—
	103-746-2	1.8	2/1-2	2.2	4.6	10.8	0.322	1.35	1	24	2	—
	103-731-1	1.8	2/1-2	6	1.0	5	0.090	0.56	1	24	2	—
	103-735-1	1.8	2/1-2	3.9	1.1	2.3	0.055	0.37	1	24	2	—
	103-724-1	5	2/1-2	6	1.2	2	0.105	0.57	1	24	2	—
	103-807-4	1.8	2/1-2	12	0.8	12	0.560	1.4	1	12	1	—
	103-807-5	1.8	2/1-2	5	1.9	12	0.560	1.4	1	24	2	—
	103-807-6	1.8	2/1-2	2.9	3.05	10.8	0.520	1.4				
	103-807-7	1.8	2/1-2	1.8	4.8	10.8	0.520	1.4				
	103-809-2	1.8	2/1-2	2.5	2.1	7.2	0.530	1.5	1	24	5	—
	103-810-1	1.8	2/1-2	3	4	17	0.900	2.5	1	24	5	—
	103-815-2	1.8	2/1-2	2.5	4.6	21.6	1.125	2.5	1	24	5	—
	103-845-1	1.8	2/1-2	5	4	35	1.550	4.5	1	48	8	—
	103-845-2	1.8	2/1-2	3	6.7	35	1.550	4.5	1	48	8	—
	103-880-11	2	2/1-2	4.8	1.4	8	0.500	1.5	1	24	3	—
	103-883-1	2	2/1-2	3.8	2.8	14	0.96	2.5	1	25	5	—
	103-860-11	2.5	2/1-2	3	4	17	0.900	2.5	1	24	5	—
	103-865-3	2.5	2/1-2	3	5	28	1.550	4.5	1	24	5	—
	103-8911-16	1.8	2/1-2	2.3	6.1	45	3.900	3.6	1	24	4	—
	103-8911-26	1.8	2/1-2	1.7	8	45	3.900	3.6	1	24	4	—
	103-8920-26	1.8	2/1-2	5.3	3.4	60	6.100	5.7	1	24	2	—
	103-8930-26	1.8	2/1-2	3.6	6.1	81	8.000	6.6	1	24	8	—
	103-8930-36	1.8	2/1-2	1.8	12.7	81	8.000	6.6	1	24	10	—
	103-901-1	0.72	2/1-2	2.0	2.5	145	37.700	18	1	24	10	—
LOW COST STEPPER	103-308-1	90	1	16	0.7	0.220	0.0042	0.16	2	16	—	33
LOW COST STEPPER	103-705-6	90	1	24	0.2	0.450	0.022	0.43	3	24	—	—
LOW COST STEPPER	103-703-1	7.5	2	12	0.12	0.190	0.0095	0.20	1	12	0.1	—
LOW COST STEPPER	103-703-3	7.5	2	24	0.085	0.200	0.0095	0.20				
LOW COST STEPPER	103-7801-2	7.5	2	3.5	1.5	1.6	0.130	0.57	1	24	1	—

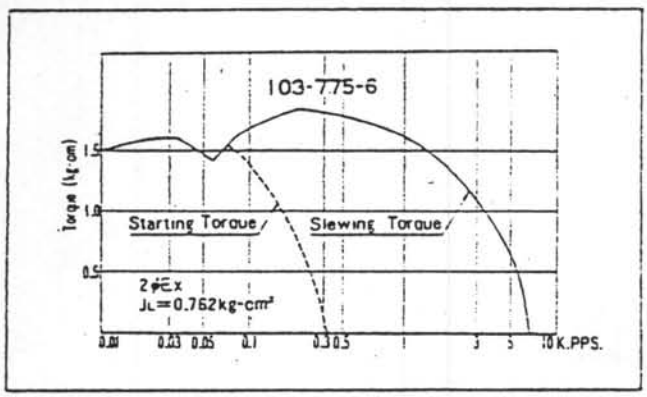


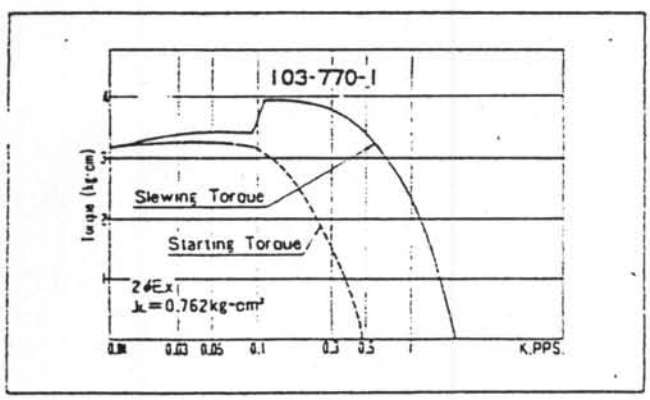
103-775-6

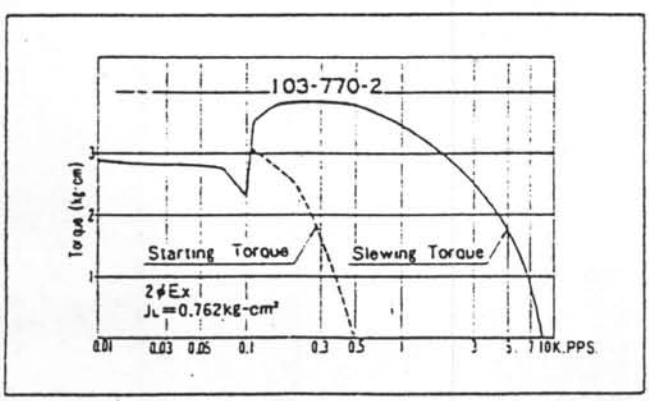
103-770-1

MODEL No.	ANGLE	ACCURACY		VOLT	CURRENT	RESISTANCE	INDUCTANCE	INPUT	HOLDING TORQUE	ROTOR INERTIA	WEIGHT	LEAD CODE	DIMENSIONS
		SPECIAL	STANDARD										
UNIT	(DEG)	(DEG)		(V)	(A/φ)	(Ω/φ)	(mH/φ)	(W)	(kg-cm)	(g-cm²)	(kg)		
103-775-6	1.8	±0.054	±0.09	2.25	1.5	1.5	1.75	7	1.7	57	0.38	81	PAGE 11
103-770-1	1.8	±0.054	±0.09	5.1	1.0	5.1	9.0	10	4.3	105	0.57	65	PAGE 11
103-770-2	1.8	±0.054	±0.09	1.3	3.9	0.33	0.53	10	4.3	105	0.57	65	PAGE 11
103-770-3	1.8	±0.054	±0.09	24	0.22	110	200	10.6	4.3	105	0.57	65	PAGE 11

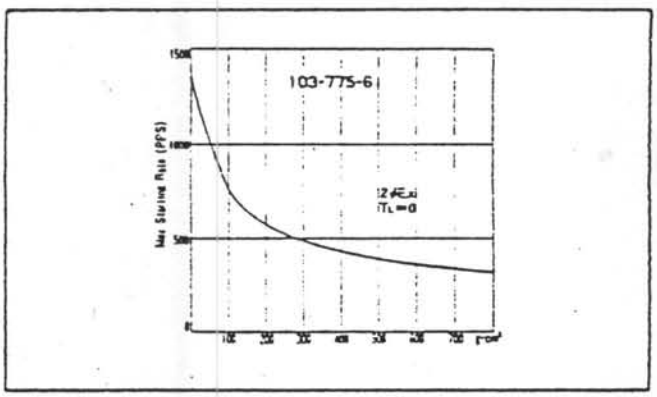
TORQUE VS. FREQUENCY

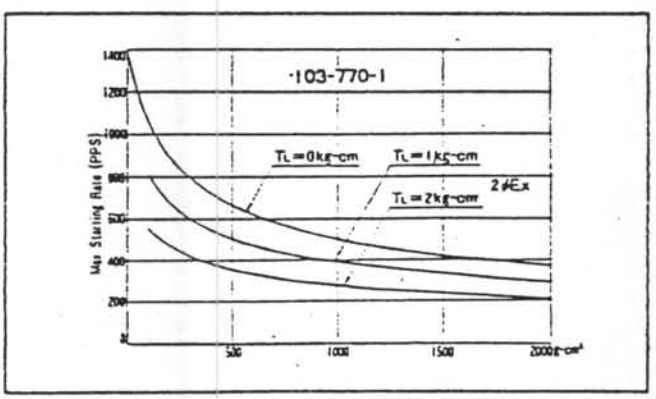


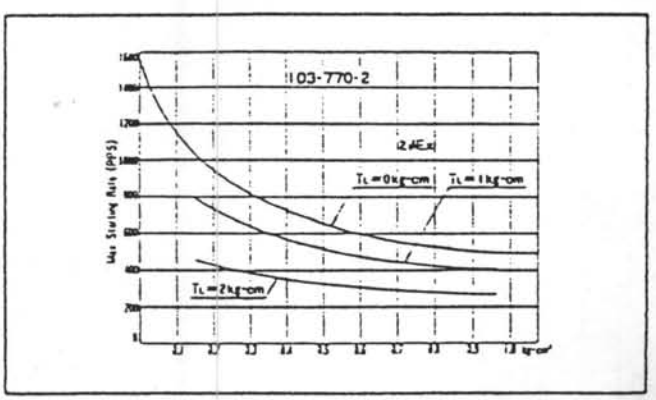




LOAD INERTIA VS. STARTING RATE

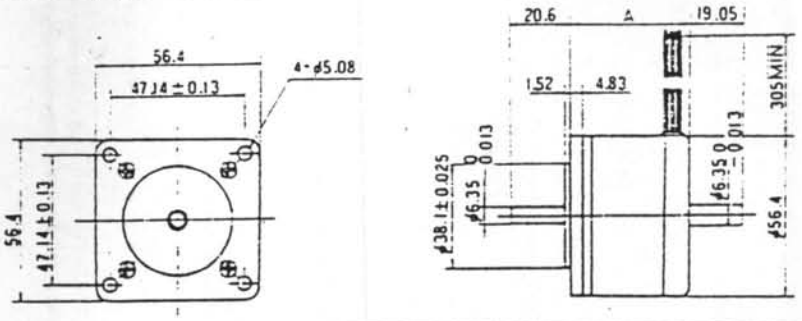






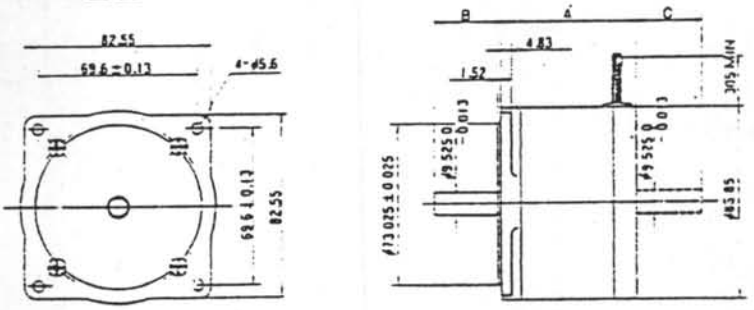
PERFORMANCE CURVES ARE BASED ON SANYO STANDARD DRIVING CIRCUITS

103-7□□ TYPE



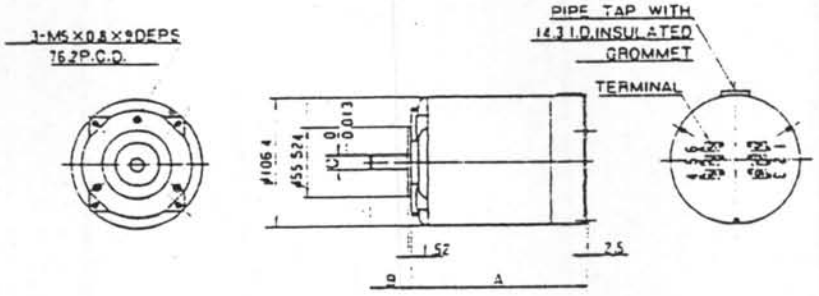
BASIC MOTOR TYPE	DIMENSION A
103-775-□□ 103-735-□□	37.5
103-770-□□ 103-724-□□□ 103Z708-□□	50.8
103-715-□□ 103Z710-□□ 103-721-□□	82.5
103-746-□□	101.6
103-731-□□	57

103-8□□ TYPE



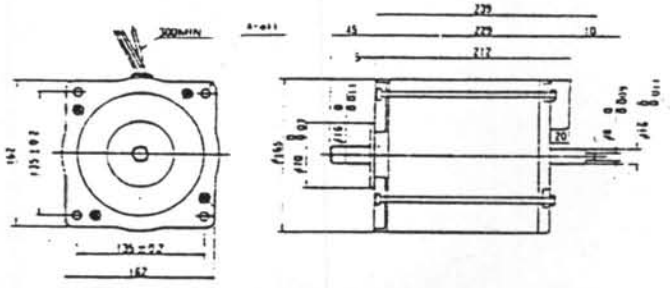
BASIC MOTOR TYPE	DIMENSION A	B	C
103-807-□□	62	30.2	28.5
103-809-□□	62	14.6	18.4
103-815-□□	93.5	30.2	30.2
103-810-□□ 103-860-□□	93.5	31.8	31.2
103-845-□□ 103-865-□□	135	25.4	25.4

103-89□□ TYPE



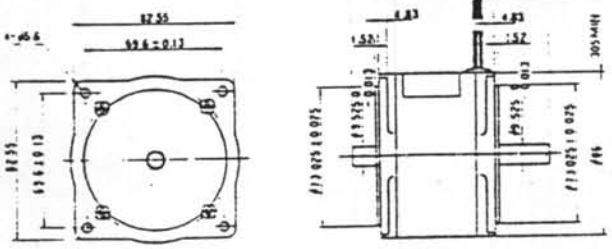
BASIC MOTOR TYPE	DIMENSION A	B	C
103-8911-□□	120	31.8	9.525
103-8920-□□	167.5	34.9	12.7
103-8930-□□	181.9	35	15.875

103-901 TYPE

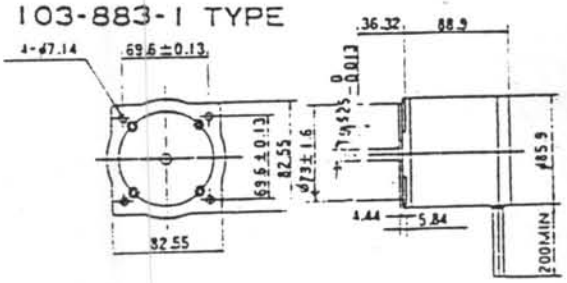


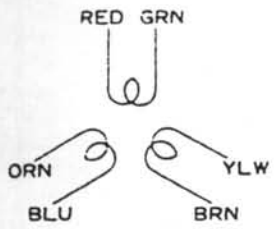
BASIC MOTOR TYPE	

103-880-11 TYPE

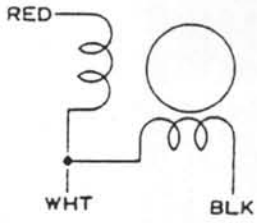


103-883-1 TYPE

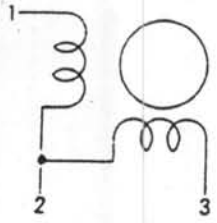




31

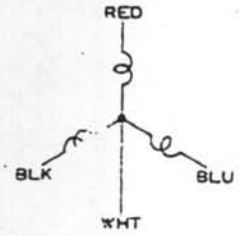


32



33

BRN : Brown
BLK : Black
WHT : White
ORN : Orange
RED : Red
YLW : Yellow
BLU : Blue
GRN : Green



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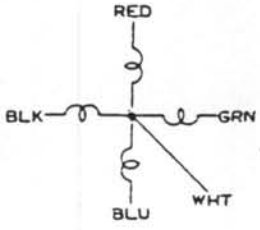
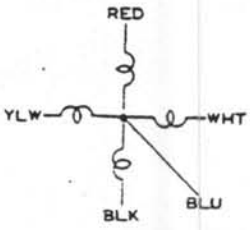
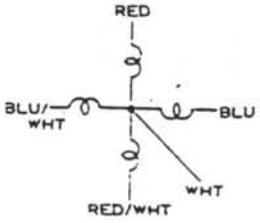


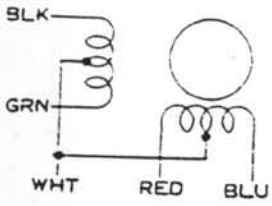
51



52



53



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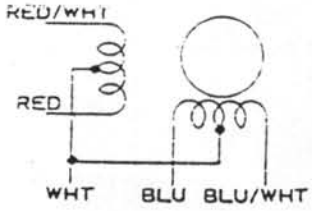

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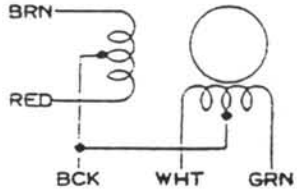
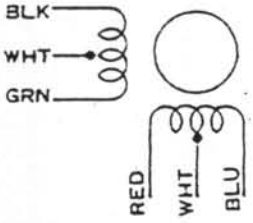


56



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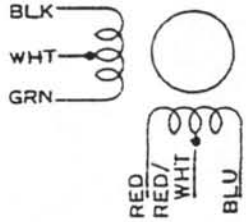

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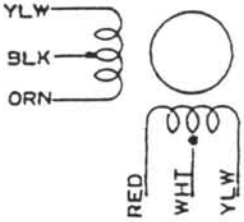
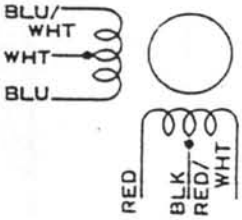
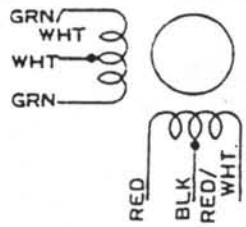


63



64



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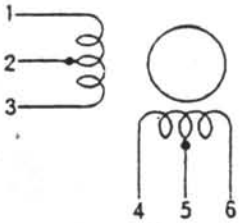

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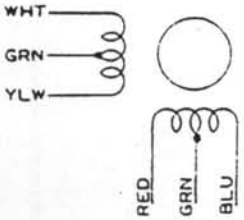
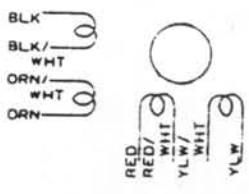


67



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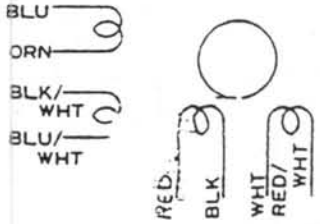


82

ภาคผนวก ข.

```
TYPE PLOT.Z80
        ORG     100H
        JP      INIT232
BUFFER  DB      80
        DS      82
KEY     DB      1BH,'PLEASE KEY COMMAND',0DH,0AH,'$'
WAIT    DB      1BH,'PLEASE WAIT UNTIL FINISHED',0DH,0AH,'$'

XMIT    PUSH    AF      ;DATA TRANSMISSION ROUTINE
XCOM    IN      A,023H
        AND     001H
        JP      Z,XCOM
        POP     AF
        OUT     022H,A
        RET
DSPL    PUSH    HL      ;CRT CHARACTER DISPLAY ROUTINE
        PUSH    DE
        PUSH    BC
        PUSH    AF
        LD      C,9
        CALL    5
        POP     AF
        POP     BC
        POP     DE
        POP     HL
        RET
WCHAR   PUSH    HL      ;WRITE  CONTROL CHARACTER TO CRT
        PUSH    DE
        PUSH    BC
        PUSH    AF
        LD      E,A
        LD      C,2
        CALL    5
        POP     AF
        POP     BC
        POP     DE
        POP     HL
        RET
GETSCRN PUSH    HL      ;GET COMMAND FROM CRT
        PUSH    DE
        PUSH    BC
        PUSH    AF
        LD      C,10
        CALL    5
        POP     AF
        POP     BC
        POP     DE
        POP     HL
        RET
```

```
INIT232 XOR     A       ;INITIALIZE IC 8251
        OUT     023H,A
        OUT     023H,A
        OUT     023H,A
        LD      A,040H
        OUT     023H,A
        LD      A,0CFH
        OUT     023H,A
        LD      A,027H
        OUT     023H,A
        IN      A,022H
        LD      A,27
        CALL    WCHAR
        LD      A,13
        CALL    WCHAR
        LD      A,10
        CALL    WCHAR
BEGIN   LD      DE,KEY
        CALL    DSPL
BGN     LD      DE,BUFFER
        CALL    GETSCRN
        LD      HL,BUFFER+2
        LD      A,(HL)
        CP      'E'     ;EXIT ?
        JP      NZ,SEND
EXIT    JP      0       ;EXIT
SEND    LD      A,0DH
        CALL    WCHAR
        LD      A,0AH
        CALL    WCHAR
        LD      HL,BUFFER       ;PREPARE TO SEND COMMAND
        INC     HL
        LD      C,(HL)
        INC     HL
TRAN    LD      A,(HL)  ;SEND COMMAND TO PLOTTER
        CALL    XMIT
        DEC     C
        JP      Z,PATCH
        INC     HL
        JP      TRAN
PATCH   LD      A,003H  ;SEND PATCHING CHARACTER
        CALL    XMIT
        CALL    XMIT
        CALL    XMIT
        LD      DE,WAIT
        CALL    DSPL
        JP      BGN
        END     100H
```

```
PLOTTER MONITOR
        ORG     0
STATUS  LD      SP,00FF0H
        JP      BEGIN
STAREA  DB      'PU MO PD PA0400,0300 PD MU0200 '
        DB      'MR0300 MD0200 ML0300 PU MO',1AH
INIT232 XOR     A       ;INITIALIZE IC# 8251
        OUT     005H,A
        OUT     005H,A
        OUT     005H,A
        LD      A,040H
        OUT     005H,A
        LD      A,0CFH
        OUT     005H,A
        LD      A,027H
        OUT     005H,A
        IN      A,004H
        RET
REC     IN      A,005H  ;CHECK FOR RECEIVE READY
        AND     002H
        JP      Z,REC
        IN      A,004H
        RET
FRNTPNL IN      A,010H  ;CHECK FRONT PANEL
        BIT     6,A
        JP      Z,SLFTEST
LFTT    IN      A,010H
        BIT     0,A
        JP      Z,LFT
        BIT     1,A
        JP      Z,RGT
UPP     IN      A,010H
        BIT     2,A
        JP      Z,UP
        BIT     3,A
        JP      Z,DWN
        RET
SLFTEST LD      A,(CNTRL)       ;SELFTEST ROUTINE
        RES     2,A
        LD      (CNTRL),A
        OUT     020H,A
        LD      IX,STAREA
        CALL    INTRPRT
        LD      A,(CNTRL)
        SET     2,A
        LD      (CNTRL),A
        OUT     020H,A
        JP      LFTT
LFT     IN      A,010H  ; 'LEFT' BUTTON PUSHED
        BIT     4,A
        JP      Z,GRND
        CALL    TRNLFT
        JP      UPP
```

```
RGT     IN      A,010H  ; 'RIGHT' BUTTON PUSHED
        BIT     4,A
        JP      Z,GRND
        CALL    TRNRGT
        JP      UPP
UP      IN      A,010H  ; 'UP' BUTTON PUSHED
        BIT     5,A
        JP      Z,GRND
        CALL    TRNUP
        JP      GRND
DWN     IN      A,010H  ; 'DOWN' BUTTON PUSHED
        BIT     5,A
        JP      Z,GRND
        CALL    TRNDWN
        JP      GRND
GRND    RET
TRNLFT  NOP             ;MOVE PEN -X DIRECTION
        LD      DE,STATEX
        LD      HL,STATEX+1
        CALL    RLCA
        LD      A,(STATEX)
        OUT     080H,A
        CALL    DELAY
        RET
TRNRGT  NOP             ;MOVE PEN +X DIRECTION
        LD      DE,STATEX
        LD      HL,STATEX+1
        CALL    RRCA
        LD      A,(STATEX)
        OUT     080H,A
        CALL    DELAY
        RET
TRNUP   NOP             ;MOVE PEN +Y DIRECTION
        LD      DE,STATEY
        LD      HL,STATEY+1
        CALL    RLCA
        LD      A,(STATEY)
        OUT     040H,A
        CALL    DELAY
        RET
TRNDWN  NOP             ;MOVE PEN -Y DIRECTION
        LD      DE,STATEY
        LD      HL,STATEY+1
        CALL    RRCA
        LD      A,(STATEY)
        OUT     040H,A
        CALL    DELAY
        RET
```

```
RRCA    LD      A,(DE)
        RRD
        RRCA
        RRCA
        RRCA
        RRCA
        LD      (DE),A
        RET
RLCA    LD      A,(DE)
        RRCA
        RRCA
        RRCA
        RRCA
        RLD
        LD      (DE),A
        RET
DELAY   PUSH    BC          ; 5 MILLISEC. DELAY FOR STEPPING MOTOR
        PUSH    AF
        LD      A,5
DLY0    LD      C,124
DLY1    DEC     C
        JP      NZ,DLY1
        DEC     A
        JP      NZ,DLY0
        POP     AF
        POP     BC
        RET
DLPEN   PUSH    BC          ;TIME DELAY FOR PEN LIFT
        PUSH    AF
        LD      A,250
DLP0    LD      C,248
DLP1    DEC     C
        JP      NZ,DLP1
        DEC     A
        JP      NZ,DLP0
        POP     AF
        POP     BC
        RET
CP16    PUSH    HL          ;16 BITS COMPARE ROUTINE
        PUSH    DE
        OR      A
        SBC     HL,DE
        POP     DE
        POP     HL
        RET
```

```
ASXDEC  PUSH    HL          ;CONVERT ASCII STRING TO HEX
        PUSH    DE          ;STRING BEGINNING ADDRESSED BY REG. IX
        PUSH    BC
        PUSH    AF
        LD      B,4
        LD      HL,0
LOOP    ADD     HL,HL
        PUSH    HL
        ADD     HL,HL
        ADD     HL,HL
        POP     DE
        ADD     HL,DE
        LD      A,(IX)
        SUB     A,30H
        LD      E,A
        LD      D,0
        ADD     HL,DE
        INC     IX
        DJNZ    $-17
        LD      (HEX),HL
        POP     AF
        POP     BC
        POP     DE
        POP     HL
        RET
INTRPRT LD      A,(IX)  ;CHECK FOR COMMAND
        CP      'P'
        JP      Z,PP
        CP      'M'
        JP      Z,MOD
        CP      ' '
        JP      NZ,CTRZ
        INC     IX
        JP      INTRPRT
CTRZ    CP      01AH
        JP      Z,EXIT
        CP      003H
        JP      Z,EXIT
        LD      A,(CNTRL)
        RES     1,A
        OUT     020H,A
        HALT
EXIT    RET
PP      INC     IX
        LD      A,(IX)
        CP      'U'
        JP      Z,PUU
        CP      'D'
        JP      Z,PDD
        CP      'A'
        JP      Z,PAA
        JP      CTRZ
```

```
MOO     INC     IX
        LD      A,(IX)
        CP      'O'
        JP      Z,MOR
        CP      'L'
        JP      Z,MLL
        CP      'R'
        JP      Z,MRR
        CP      'U'
        JP      Z,MUU
        CP      'D'
        JP      Z,MDD
        JP      CTRZ
PUU     CALL    PU
        JP      NXT
PDD     CALL    PD
        JP      NXT
PAA     LD      HL,0
        LD      (XS),HL
        LD      (YS),HL
        CALL    PA
        JP      NXT
MLL     CALL    ML
        JP      NXT
MRR     CALL    MR
        JP      NXT
MUU     CALL    MU
        JP      NXT
MDD     CALL    MD
        JP      NXT
MOR     CALL    MO
NXT     INC     IX
        JP      INTRPRT
PU      LD      A,(CNTRL)       ;PEN UP ROUTINE
        SET     0,A
        OUT     020H,A
        LD      (CNTRL),A
        CALL    DLPEN
        RET
PD      LD      A,(CNTRL)       ;PEN DOWN ROUTINE
        RES     0,A
        OUT     020H,A
        LD      (CNTRL),A
        CALL    DLPEN
        RET
MO      IN      A,010H  ;MOVE TO ORIGIN ROUTINE
        BIT     4,A
        JP      NZ,WEST
        JP      STH
```

```
WEST    CALL    TRNLFT
STH     IN      A,010H
        BIT     5,A
        JP      NZ,SOUTH
        AND     030H
        JP      NZ,MO
        CALL    TRNUP
        CALL    TRNUP
        CALL    TRNUP
        CALL    TRNRGT
        CALL    TRNRGT
        CALL    TRNRGT
        JP      ORGN
SOUTH   CALL    TRNDWN
        JP      MO
ORGN    RET
ML      INC     IX          ;ML COMMAND
        CALL    ASXDEC
ML1     LD      HL,(HEX)
        LD      DE,0
        CALL    CP16
        JP      Z,STILL
        IN      A,010H
        BIT     4,A
        JP      Z,STILL
        CALL    TRNLFT
        LD      HL,(HEX)
        DEC     HL
        LD      (HEX),HL
        JP      ML1
MR      INC     IX          ;MR COMMAND
        CALL    ASXDEC
MR1     LD      HL,(HEX)
        LD      DE,0
        CALL    CP16
        JP      Z,STILL
        IN      A,010H
        BIT     4,A
        JP      Z,STILL
        CALL    TRNRGT
        LD      HL,(HEX)
        DEC     HL
        LD      (HEX),HL
        JP      MR1
```

```
MU      INC     IX      ;MU COMMAND
        CALL    ASXDEC
MU1     LD      HL,(HEX)
        LD      DE,0
        CALL    CP16
        JP      Z,STILL
        IN      A,010H
        BIT     5,A
        JP      Z,STILL
        CALL    TRNUP
        LD      HL,(HEX)
        DEC     HL
        LD      (HEX),HL
        JP      MU1
MD      INC     IX      ;MD COMMAND
        CALL    ASXDEC
MD1     LD      HL,(HEX)
        LD      DE,0
        CALL    CP16
        JP      Z,STILL
        IN      A,010H
        BIT     5,A
        JP      Z,STILL
        CALL    TRNDWN
        LD      HL,(HEX)
        DEC     HL
        LD      (HEX),HL
        JP      MD1
STILL   RET
BEGIN   NOP             ;INITIALIZE PLOTTER STATUS
        LD      A,0FFH
        LD      (CNTRL),A
        LD      HL,0A956H
        LD      (STATEX),HL
        LD      (STATEY),HL
        LD      A,(CNTRL)
        OUT     020H,A
        LD      A,(STATEX)
        OUT     080H,A
        LD      A,(STATEY)
        OUT     040H,A
        CALL    PU
        CALL    MO
        CALL    INIT232
FRONT   CALL    FRNTPNL
RS232   LD      HL,CMAREA       ;ANY INPUT FROM MICROCOMPUTER ?
        IN      A,005H
        AND     002H    ;IF 'NO' JUMP TO FRONT
        JP      Z,FRONT         ;IF 'YES' PUT IT INTO CMAREA
        LD      C,3
        IN      A,004H
PUT     LD      (HL),A
        CP      003H
        JP      Z,COUNT
        LD      C,3
CONT    INC     HL
        CALL    REC
        JP      PUT
```

```
.COUNT  DEC     C
        JP      NZ,CONT
        LD      IX,CMAREA
        CALL    INTRPRT
        CALL    INIT232
        JP      FRONT
DEST    PUSH    HL
        INC     IX
        CALL    ASXDEC.
        LD      HL,(HEX)
        LD      (DESX),HL
        INC     IX
        CALL    ASXDEC.
        LD      HL,(HEX)
        LD      (DESY),HL
        POP     HL
        RET
DELXY   PUSH    HL
        PUSH    DE
        PUSH    AF
        LD      HL,(DESX)
        LD      DE,(XS)
        OR      A
        SBC     HL,DE
        JP      P,DEL1
        LD      HL,(XS)
        LD      DE,(DESX)
        OR      A
        SBC     HL,DE
DEL1    LD      (DELX),HL
        LD      HL,(DESY)
        LD      DE,(YS)
        OR      A
        SBC     HL,DE
        JP      P,DEL2
        LD      HL,(YS)
        LD      DE,(DESY)
        OR      A
        SBC     HL,DE
DEL2    LD      (DELY),HL
        POP     AF
        POP     DE
        POP     HL
        RET
```

```
PREPARE LD      HL,(DELX)   ;PREPARE VARIBLE FOR GENERATE ROUTINE
        LD      DE,(DELY)
        CALL    CP16.
        JP      P,SLOP
        LD      (SLOPE),HL
        LD      (DEVIDER),DE
CHFLG   LD      HL,(DELX)
        LD      DE,(DELY)
        CALL    CP16.
        JP      Z,STFLAG
        LD      A,0
        LD      (FLAG),A
        RET
STFLAG  LD      HL,(DELX)
        LD      A,H
        OR      L
        JP      Z,STLL
        LD      A,1
        LD      (FLAG),A
        RET
STLL    POP     AF
        RET
SLOP    LD      (SLOPE),DE
        LD      (DEVIDER),HL
        JP      CHFLG
SETDRC  PUSH    HL
        PUSH    DE
        LD      A,0
        LD      HL,(DESX)
        LD      DE,(XS)
        CALL    CP16
        JP      P,SDR1.
        LD      HL,(DESY)
        LD      DE,(YS)
        CALL    CP16
        JP      P,SDR2
        LD      HL,(DELX)
        LD      DE,(DELY)
        CALL    CP16.
        JP      P,SD7
        JP      SD8.
SDR1    LD      HL,(DESY)
        LD      DE,(YS)
        CALL    CP16
        JP      P,SDR11
SDR12   LD      HL,(DELX)
        LD      DE,(DELY)
        CALL    CP16
        JP      P,SD3
        JP      SD4
        JP      P,SD3
        JP      SD4
```

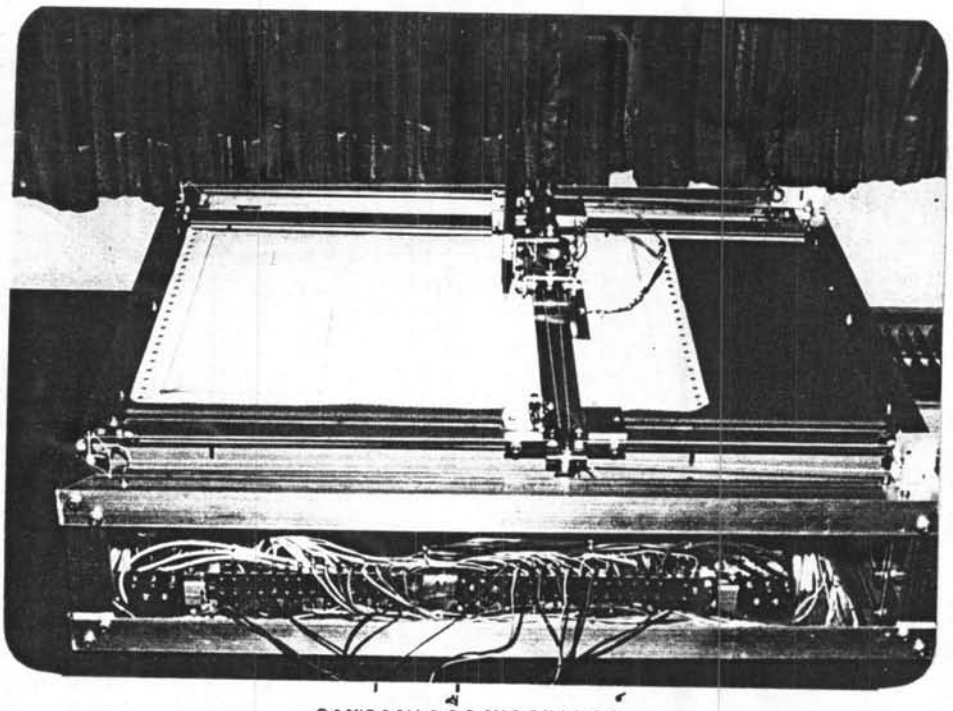
```
SDR11   LD      HL,(DELX)
        LD      DE,(DELY)
        CALL    CP16
        JP      P,SD1
        JP      SD2
SDR2    LD      HL,(DELX)
        LD      DE,(DELY)
        CALL    CP16
        JP      P,SD5
        JP      SD6
SD8     INC     A
SD7     INC     A
SD6     INC     A
SD5     INC     A
SD4     INC     A
SD3     INC     A
SD2     INC     A
SD1     INC     A
        LD      (PAT),A
        POP     DE
        POP     HL
        RET
APT     LD      A,(PAT)
        CP      1
        JP      Z,AA1
        CP      2
        JP      Z,AA2
        CP      3
        JP      Z,AA1
        CP      4
        JP      Z,AA4
        CP      5
        JP      Z,AA5
        CP      6
        JP      Z,AA2
        CP      7
        JP      Z,AA5
        JP      AA4
AA1     CALL    TRNRGT
        RET
AA2     CALL    TRNUP
        RET
AA4     CALL    TRNDWN
        RET
AA5     CALL    TRNLFT
        RET
```

```
BPT     LD      A,(PAT)
        CP      1
        JP      Z,BB1
        CP      2
        JP      Z,BB2
        CP      3
        JP      Z,BB3
        CP      4
        JP      Z,BB4
        CP      5
        JP      Z,BB5
        CP      6
        JP      Z,BB6
        CP      7
        JP      Z,BB7
        JP      BB8
BB1     CALL    TRNUP
        CALL    TRNRGT
        RET
BB2     CALL    TRNRGT
        CALL    TRNUP
        RET
BB3     CALL    TRNDWN
        CALL    TRNRGT
        RET
BB4     CALL    TRNRGT
        CALL    TRNDWN
        RET
BB5     CALL    TRNUP
        CALL    TRNLFT
        RET
BB6     CALL    TRNLFT
        CALL    TRNUP
        RET
BB7     CALL    TRNDWN
        CALL    TRNLFT
        RET
BB8     CALL    TRNLFT
        CALL    TRNDWN
        RET
PA      NOP       ; PA ROUTINE
        CALL    DEST
        CALL    DELXY
        CALL    PREPARE
        LD      HL,(DEVIDER)
        LD      (CTDWN),HL
        CALL    SETDRC
```

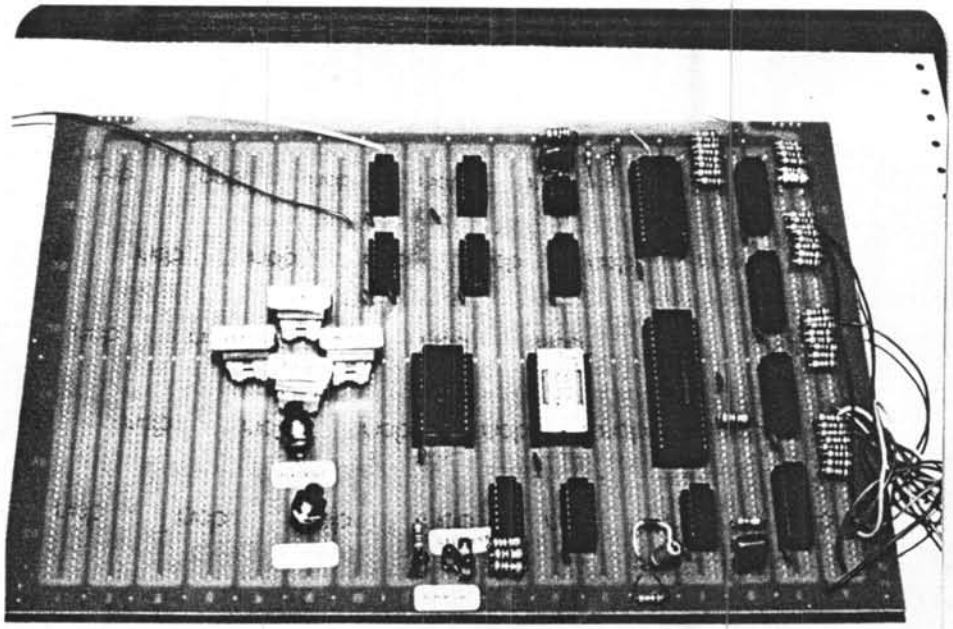
```
GENER   LD      HL,0    ;GENERATE STAIR STEP
        LD      (LAST),HL
        LD      B,1
        LD      HL,(SLOPE)
        LD      (NEXT),HL
        LD      (SUM),HL
GNR0    NOP
        LD      HL,(SUM)
        LD      DE,(DEVIDER)
        CALL    CP16
        JP      P,GNR2
        CALL    APT
        LD      C,0
        LD      B,1
        JP      JUNC
JUNC    LD      A,(FLAG)
        CP      1
        JP      Z,INIT
        LD      HL,(NEXT)
        LD      (LAST),HL
        LD      DE,(SLOPE)
        ADD     HL,DE
        LD      (NEXT),HL
        LD      DE,(LAST)
        ADD     HL,DE
        LD      (SUM),HL
        JP      CROSS
CROSS   LD      A,0
        LD      (FLAG),A
        LD      HL,(NEXT)
        LD      DE,(DEVIDER)
        CALL    CP16
        JP      M,FINISH
        LD      HL,(LAST)
        LD      DE,(DEVIDER)
        CALL    CP16
        JP      P,FINISH
        LD      A,1
        LD      (FLAG),A
        LD      C,0
        JP      FINISH
GNR2    LD      A,(FLAG)
        CP      1
        JP      NZ,GNR3
        DEC     C
        JP      Z,GNR3
        DEC     B
        JP      Z,GNR6
        CALL    APT
        LD      B,1
        JP      JUNC
```

```
INIT    LD      BC,(DENOMINATOR)
        LD      HL,(NUMERATOR)
        OR      A
        SBC     HL,BC
        LD      (LAST),HL
        LD      HL,(LAST)
        LD      DE,(SLOPE)
        ADD     HL,DE
        LD      (NEXT),HL
        LD      HL,(NEXT)
        LD      DE,(LAST)
        ADD     HL,DE
        LD      (SUM),HL
        JP      CROSS
GNR3    LD      B,0
        DEC     C
        JP      Z,GNR7
        CALL    BPT
        LD      C,1
        JP      JUNC
GNR7    CALL    APT
        LD      C,1
        JP      JUNC
GNR6    CALL    BPT
        LD      B,1
        JP      JUNC
FINISH  LD      HL,(CTDWN)
        PUSH    BC
        DEC     HL
        LD      A,H
        LD      B,L
        OR      B
        POP     BC
        JP      Z,FN
        LD      (CTDWN),HL
        JP      GNR0
FN      RET

CMAREA  EQU     800H
STATEX  EQU     850H
STATEY  EQU     852H
CNTRL   EQU     854H
HEX     EQU     856H
LAST    EQU     858H
NEXT    EQU     85AH
SUM     EQU     85CH
SLOPE   EQU     85EH
DENOMER EQU     860H
FLAG    EQU     862H
DESX    EQU     864H
DESY    EQU     866H
DELX    EQU     868H
DELY    EQU     86AH
CTDWN   EQU     86CH
PAT     EQU     86EH
XS      EQU     870H
YS      EQU     872H

        END
```

ภาคผนวก ค.

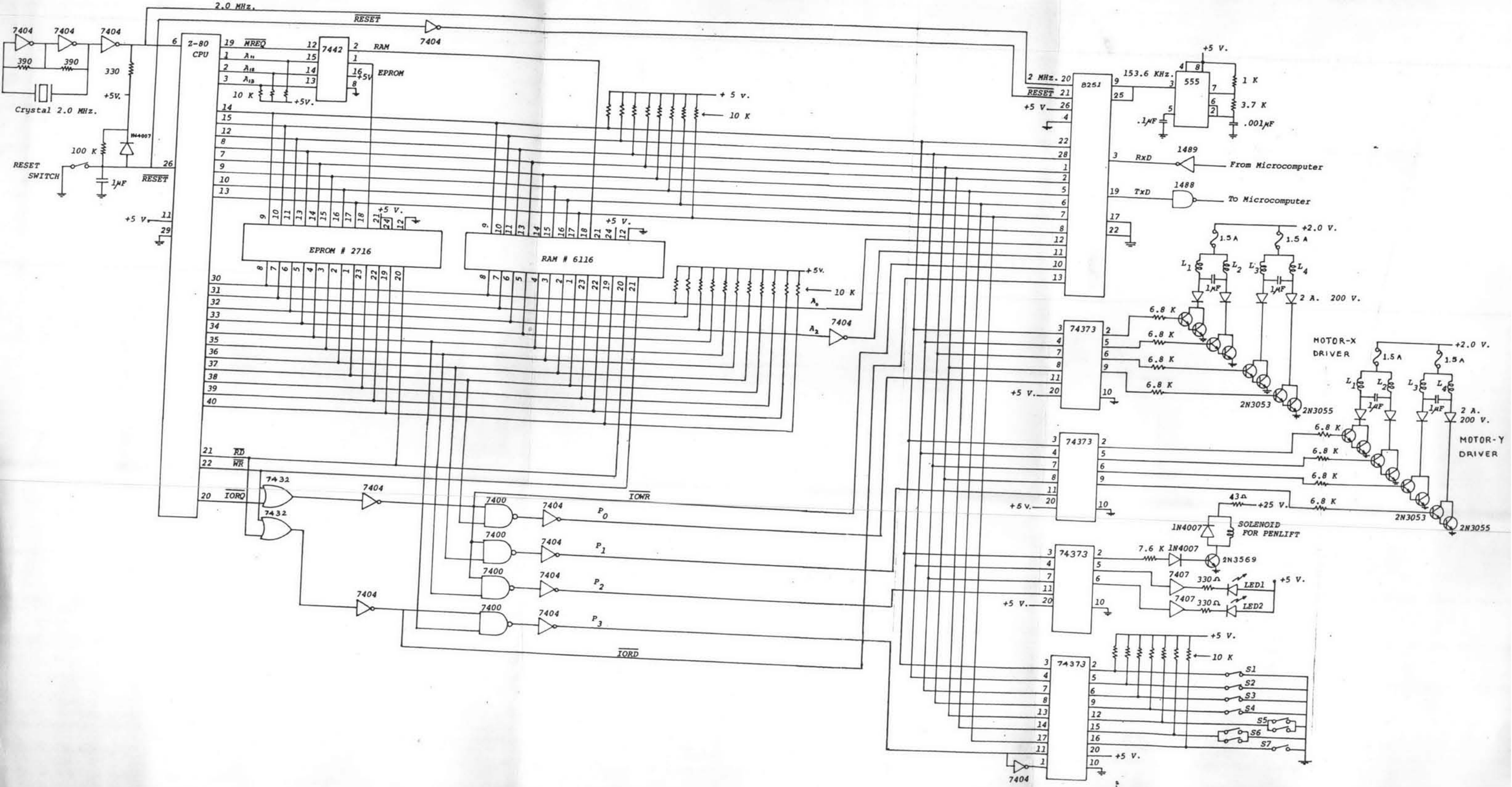


ภาพถ่ายเครื่องพลอทเตอร์



ภาพถ่ายไมโครโปรเซสเซอร์และอุปกรณ์ที่ใช้ควบคุม

ภาคผนวก ง.
วงจรที่ใช้ควบคุมการทำงานของพลอตเตอร์


7404
7404
7404
390
390
330
+5V.
Crystal 2.0 MHz.
100 K
IN4007
RESET SWITCH
1μF
RESET
+5 V.
2.0 MHz.
RESET
7404
Z-80 CPU
MREQ
A11
A12
A13
7442
RAM
EPROM
+5V.
10 K
+5V.
EPROM # 2716
RAM # 6116
+ 5 v.
10 K
+5V.
10 K
A0
A2
7404
IOWR
IORD
RD
WR
IORQ
7432
7432
7404
7400
7404
P0
P1
P2
P3
2 MHz.
RESET
+5 V
8251
153.6 KHz.
555
1 K
3.7 K
.1μF
.001μF
1489
RxD
From Microcomputer
1488
TxD
To Microcomputer
+2.0 V.
1.5 A
L1
L2
L3
L4
1μF
2 A. 200 V.
74373
6.8 K
2N3053
2N3055
MOTOR-X DRIVER
MOTOR-Y DRIVER
43Ω
+25 V.
1N4007
SOLENOID FOR PENLIFT
7.6 K
2N3569
7407
330Ω
LED1
LED2
S1
S2
S3
S4
S5
S6
S7

ประวัติผู้เขียน

นายสืบสกุล พิภพมงคล เกิดเมื่อวันที่ ๔ มกราคม พ.ศ. ๒๕๐๒ ที่กรุงเทพฯ สำเร็จการศึกษาวิศวกรรมศาสตรบัณฑิต สาขาวิศวกรรมไฟฟ้า จากจุฬาลงกรณ์มหาวิทยาลัย เมื่อปี พ.ศ. ๒๕๒๓ เข้าศึกษาต่อชั้นปริญญามหาบัณฑิตสาขาวิชาคอมพิวเตอร์ศาสตร์ ที่ภาควิชาวิศวกรรมคอมพิวเตอร์ จุฬาลงกรณ์มหาวิทยาลัยในปีเดียวกัน