การพัฒนาเครื่องวัดเฟเซอร์ตามมาตรฐาน IEEE C37.118

นายปณัท ถวิลทรัพย์

วิทยานิพนธ์นี้เป็นส่วนหนึ่งของการศึกษาตามหลักสูตรปริญญาวิศวกรรมศาสตรมหาบัณฑิต
สาขาวิชาวิศวกรรมไฟฟ้า ภาควิชาวิศวกรรมไฟฟ้า
คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย
ปีการศึกษา 2555

DEVELOPMENT OF PHASOR MEASUREMENT UNIT CONFORMED TO IEEE C37.118 STANDARD

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A Thesis Submitted in Partial Fulfillment of the Requirements

for the Degree of Master of Engineering Program in Electrical Engineering

Department of Electrical Engineering

Faculty of Engineering

Chulalongkorn University

Academic Year 2012

Thesis Title	DEVELOPMENT OF PHASOR MEASUREMENT UNIT CONFORMED TO IEEE C37.118 STANDARD
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ปณัท ถวิลทรัพย์ : การพัฒนาเครื่องวัดเฟเซอร์ตามมาตรฐาน IEEE C37.118. (DEVELOPMENT OF PHASOR MEASUREMENT UNIT CONFORMED TO IEEE C37.118 STANDARD) อ.ที่ปรึกษาวิทยานิพนธ์หลัก : ผศ.ดร.วันเฉลิม โปรา, 59 หน้า.

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ปีการศึกษา 2555

5370275421 : MAJOR ELECTRICAL ENGINEERING

KEYWORDS : PHASOR MEASUREMENT UNIT / PMU / SYNCHROPHASOR / IEEE C37.118

PANUT TAVILSUP : DEVELOPMENT OF PHASOR MEASUREMENT UNIT CONFORMED TO IEEE C37.118 STANDARD. ADVISOR : ASST. PROF. WANCHALERM PORA, Ph.D., 59 pp.

Phasor is an electrical complex value containing of magnitude root mean square value and phase angle in polar form represents instantaneous electrical sinusoidal waveform. We propose an idea to develop phasor measurement device that conformed accuracy to IEEE C37.118 standard for 50 Hz power system without communication part.

Department : Electrical Engineering Student's Signature .....

Field of Study : Electrical Engineering Advisor's Signature .....

Academic Year : 2012

ACKNOWLEDGEMENTS

I would like to express my gratitude to my advisor, Asst. Prof. Dr. Wanchalerm Pora, for his patient guidance and excellent advice for my thesis research.

Special thanks to my colleagues at ESID Laboratory for the interesting and helpful discussions on many engineering topics. Moreover, thank to Texas Instrument Company for an amount of ADC chip they gave for my research.

Finally, I am grateful to my parents for their support and encouragement to complete my study.

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CHAPTER I

PREFACE

1.1 Prologue

Phasor Measurement Unit (PMU) is a measuring device for magnitude and phase monitoring in power system applications; sometime it is called “Synchrophasor” because it has the common time reference for phase measuring on all observation sites. The time reference is generally selected to be time pulse of GPS receiver which is synchronized to Global Positioning System (GPS) clock, and available on Time-Pulse pin in some GPS receivers.

PMU is normally used as a sampling unit in Supervisory Control And Data Acquisition (SCADA) system; It send out instantaneous phasor with its sampling time to data concentrator, to collect data for applications such as adaptive relaying, state estimation, transmission and generation modeling verification, fault location, wide-area protection, and improved control [3].

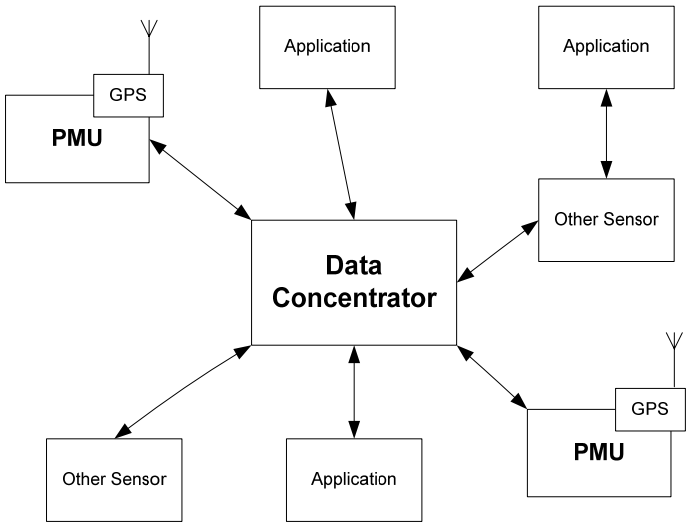

Figure 1-1: Position of PMU in SCADA.

This research conforms to the IEEE C37.118 in [4] only the accuracy limit, signal capability ranges, and reporting rates. Something is changed for convenient researching but restorable: angle unit is changed from radian unit to degree unit, phasor is redefined to be zero degree when rising edge of the time reference occurs at positive zero-crossing, and no communication part as in the standard.

1.2 Research Objective

This research is planned to implement phasor measuring device for future power system applications with a standard to control and define it quality which is called IEEE C37.118.

1.3 Research Boundary

Implemented PMU shell not output phasor with error that exceed accuracy limit of 1% TVE, and be able to send out 10 phasors or 25 phasors per second. Input signal capability range should conform to following content.

Magnitude : 10 % … 120 % of 220 V_{RMS}.

Frequency : ± 5 Hz from 50 Hz.

Phase : ± π radians.

1.4 Research Interests

1.4.1 To achieve knowledge and experience on GPS and its applications.

1.4.2 To improve knowledge and technical skill on hardware design.

1.4.3 To achieve knowledge and technical skill on Printed Circuit Board layout-design.

1.4.4 To achieve knowledge and experience on ARM microcontroller.

1.4.5 To improve knowledge and technical skill on C programming language.

1.5 Paper Review on Synchrophasor Design Based on a DSP-Microcontroller

The paper in [8] describes a design of synchrophasor by using TMS320LF2407 a Digital Signal Processing (DSP) chip from Texas Instruments (TI) with hardware connection as is shown in figure 1-2.

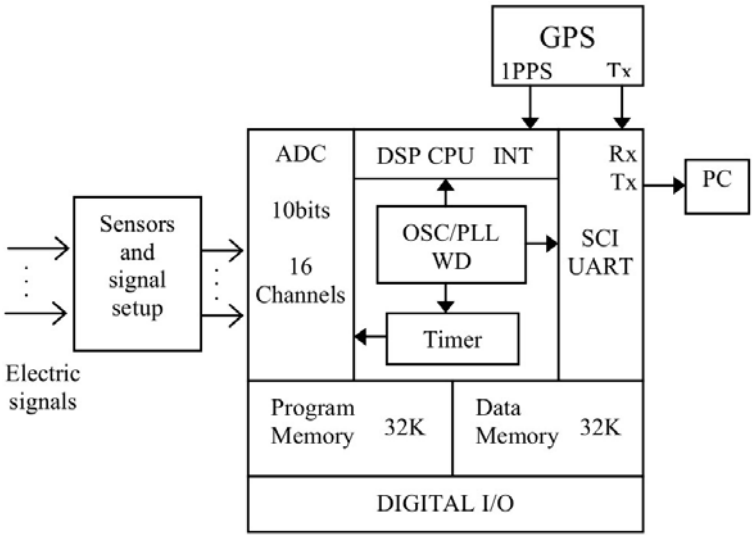

Figure 1-2: Hardware Design of the Reviewed Paper.

In detail, signal voltage is divided by sensor to the digital voltage range (0 to 3.3 V) before sampled by 10-bit internal ADC. Phasor is calculated by applying DFT to a group of 16 samples with a window of one period size. Note that their prototype was tested with 60 Hz of 220 V_{RMS}.

For result, the maximum magnitude error was of 2 V or 0.39% of the total range, and the maximum angle error was 2 degrees or 2.2% of the total range. The paper only tells that their result was acceptable for their application.

CHAPTER II

RELEVANT IMPORTANT THEORIES

This chapter is only about important theories that have direct relation to this research but independent to any hardware.

2.1 Phasor

Phasor is a complex value that represents instantaneous sinusoidal waveform of $x(t)$ which has a definition in [2] as is shown in equation (1).

$$x(t) = X_{max}\cos(\omega t + \theta) \tag{1}$$

Where X_{max} is a maximum magnitude of $x(t)$.

To understand the definition, figure 2-1 should be the simplest illustration of a phasor.

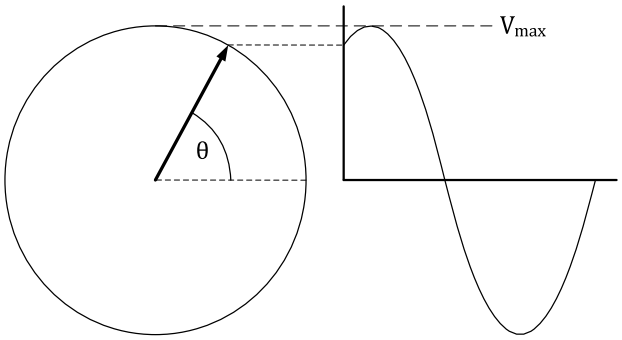

Figure 2-1: Phasor Vector.

Phasor can be represented in exponential form, polar form, and rectangular form as description in equation (2), (3) and (4) respectively.

$$X = \frac{X_{max}}{\sqrt{2}}e^{j\theta} \tag{2}$$

$$X = \frac{X_{max}}{\sqrt{2}}\angle\theta \tag{3}$$

$$X = \frac{X_{max}}{\sqrt{2}}(\cos\theta + \mathrm{j}\sin\theta) = X_r + jX_i \quad (4)$$

Where $\frac{X_{max}}{\sqrt{2}}$ is a RMS magnitude value of sinusoidal $x(t)$,

θ is a phase angle in degree unit,

X_r is a real part of phasor,

X_i is an imaginary part of phasor.

Equation (5) and (6) are auxiliary equation for conversion process between polar form and rectangular form; polar form shall be the main form for this research.

$$\frac{X_{max}}{\sqrt{2}} = \sqrt{{X_r}^2 + {X_i}^2} \quad (5)$$

$$\theta = \tan^{-1}\frac{X_i}{X_r} \quad (6)$$

Note that in [4], Root Mean Square (RMS) value is a general form for magnitude representation and phase angle is defined to be 0 radian when the maximum of $x(t)$ occurs at the rising edge of GPS time pulse.

2.2 Root Mean Square (RMS)

RMS value is used to present magnitude of phasor in this research which is made of samples as is described in [10] as equation (7).

$$M_{RMS} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} {M_i}^2} \quad (7)$$

Where M_i is a value of sample number i,

N is a quantity of sample.

2.3 Total Vector Error (TVE)

TVE was defined in [4] as a percentage of an estimated phasor that differ from its theoretical value as is shown in equation (8).

$$TVE = \sqrt{\frac{(X_{er}-X_r)^2+(X_{ei}-X_i)^2}{X_r{}^2+X_i{}^2}} \times 100\% \quad (8)$$

Where X_{er} and X_{ei} are an estimated real part and an estimated imaginary part of a phasor respectively.

CHAPTER III

HARDWARE DESIGN

This chapter describes used component inside PMU, and its relevant theories with the same order as figure 3-1.

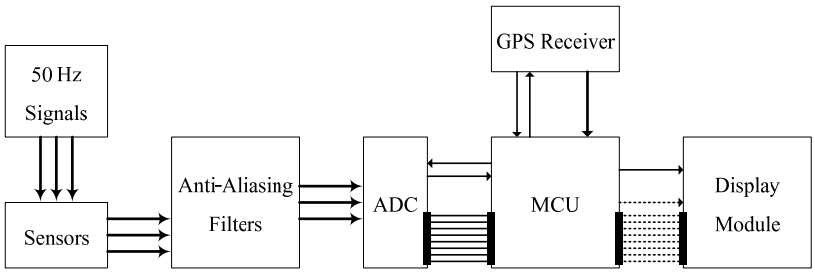

Figure 3-1: PMU Over-View.

3.1 Sensors

The voltage sensors are simply designed by using voltage divider method as is shown in figure 3-2. V_{SP1}, V_{SP2}, and V_{SP3} are acronyms of voltage source phase-1, phase-2, and phase-3 respectively as well as R_{S1P1} and R_{S2P3} that are acronyms of resistor sensor-1 for phase-1 and resistor sensor-2 for phase-3 respectively. V_{P1}, V_{P2}, and V_{P3} are step-down voltages to the V_N for PMU.

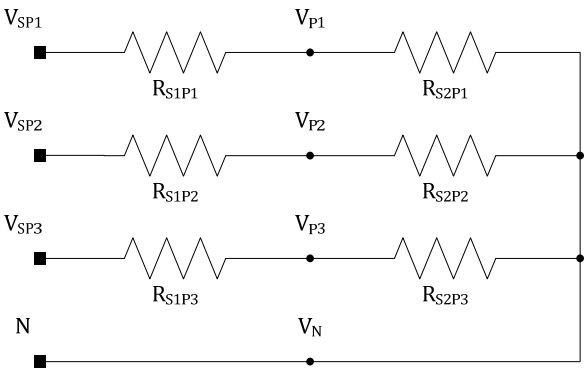

Figure 3-2: Voltage Sensor Circuit.

R_{S1} and R_{S2} of all phase are chosen to be 300 kΩ and 8.2 kΩ respectively, to keep 120 % of 220 V_{RMS} in the input range of the ADC which is ± 10 V.

3.2 Anti-Aliasing Filter

In sampling process, input signal must be sampled with at least twice of its frequency as known as the Nyquist Rate to prevent distortion result, but components of the input signal that has frequency between input frequency and sampling frequency could be accounted as lower frequency component and causes distortion effect which is called aliasing. To mitigate this, low-pass filter is used to scale those components down. And this section shall give information of filter design with theory from [6].

As phase-shift causes TVE increasing, the low-pass filters are limited to 2nd-order as a theme of phase-shift limiting, and can be designed in 2 topologies: Sallen-Key topology has advantages on separate gain setting, high gain accuracy, and low quality factor, while Multiple Feedback topology is commonly used in filters that need high quality factor and high gain. Thus, Sallen-Key topology is used in the reason of its advantages. 2nd-order filter has general form of the transfer function as represented in equation (9).

$$M(s) = \frac{G}{1+a_1 s+b_1 s^2} \tag{9}$$

Where G is DC gain for signal in pass-band,

a_1 and b_1 are the filter coefficients.

In general, circuit of the filter is connected as a template circuit that is shown in Figure 3-3 and has a transfer function as is represented in equation (10).

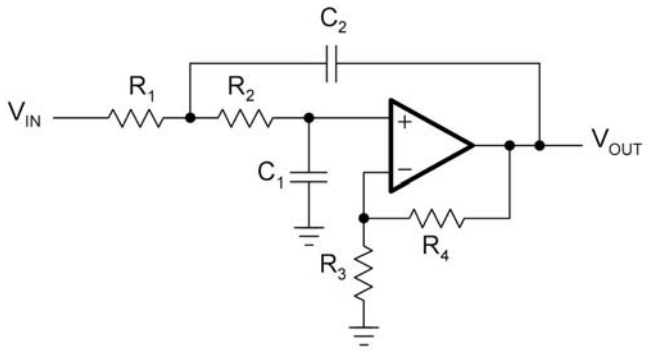

Figure 3-3: 2nd-Order Active Low-Pass Filter of Sallen-Key Topology (Standard Form).

$$M(s) = \frac{G}{1+\omega_c[C_1(R_1+R_2)+(1-G)R_1C_2]s+\omega_c{}^2R_1R_2C_1C_2s^2} \quad (10)$$

Where the filter coefficients are defined as equation (11) and (12)

$$a_1 = [C_1(R_1 + R_2) + (1 - G)R_1C_2]\omega_c \quad (11)$$

$$b_1 = R_1R_2C_1C_2\omega_c{}^2 \quad (12)$$

To find the values of resistors and capacitors, the filter coefficients must be specified which could be found in [6] or any active filter book; component results can be calculated by using equation (13), (14) and (15).

$$C_2 \geq \frac{4b_1}{a_1{}^2-4(1-A_0)b_1}C_1 \quad (13)$$

$$R_1 = \frac{a_1C_2-\sqrt{a_1{}^2C_2{}^2-4[C_1C_2+(1-G)C_2{}^2]b_1}}{2[C_1C_2+(1-G)C_2{}^2]\omega_c} \quad (14)$$

$$R_2 = \frac{a_1C_2+\sqrt{a_1{}^2C_2{}^2-4[C_1C_2+(1-G)C_2{}^2]b_1}}{2C_1C_2\omega_c} \quad (15)$$

When DC gain (G) is 1, the transfer function (10) becomes (16), and the filter circuit template in figure 3-3 is changed to the filter circuit template in figure 3-4.

$$M(s) = \frac{1}{1+\omega_cC_1(R_1+R_2)s+\omega_c{}^2R_1R_2C_1C_2s^2} \quad (16)$$

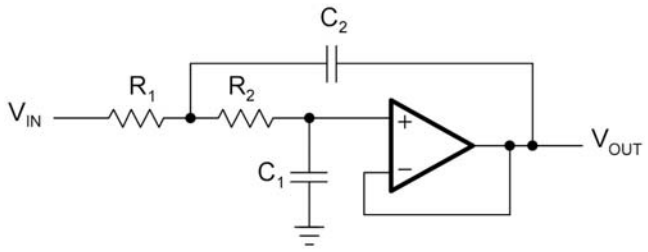

Figure 3-4: 2nd-Order Active Low-Pass Filter of Sallen-Key Topology (Unity Gain).

The filter coefficients of the unity gain are (17) and (18).

$$a_1 = C_1(R_1 + R_2)\omega_c \tag{17}$$

$$b_1 = R_1 R_2 C_1 C_2 {\omega_c}^2 \tag{18}$$

To find the values of resistors and capacitors; component results can be calculated by using equation (19), (20) and (21).

$$C_2 \geq \frac{4b_1}{{a_1}^2} C_1 \tag{19}$$

$$R_1 = \frac{a_1 C_2 - \sqrt{{a_1}^2 {C_2}^2 - 4b_1 C_1 C_2}}{2C_1 C_2 \omega_c} \tag{20}$$

$$R_2 = \frac{a_1 C_2 + \sqrt{{a_1}^2 {C_2}^2 - 4b_1 C_1 C_2}}{2C_1 C_2 \omega_c} \tag{21}$$

From the general form of the transfer function in (10) or (16), the Butterworth coefficients are the same: $a_1 = \sqrt{2}$, and $b_1 = 1$. The transfer function becomes (22).

$$M\left(j\frac{\omega}{\omega_c}\right) = \frac{1}{1 + \sqrt{2} j \frac{\omega}{\omega_c} - \left(\frac{\omega}{\omega_c}\right)^2} \tag{22}$$

Magnitude and phase responses can be estimated and plotted by using the following formulas: (23) and (24).

$$M(\omega) = -\sqrt{1 + \left(\frac{\omega}{\omega_c}\right)^4} \tag{23}$$

$$\theta(\omega) = -\tan^{-1} \frac{\sqrt{2}\frac{\omega}{\omega_c}}{1 - \left(\frac{\omega}{\omega_c}\right)^2} \tag{24}$$

Where $M(\omega)$ is magnitude attenuation at ω,

$\theta(\omega)$ is phase-shift at ω.

Since input signals are normally divided from power line and their range are large (divided to ADC in the range of ± 10 V), the filters have been selected to be unity gain (G = 1) and the circuit is connected as figure 3-4. For cut-off frequency, equation (24) is used to estimate cut-off frequency that causes shifted phase lower than 0.1 degrees; the result is 50 kHz. With equation (19), (20), and (21), and commercial component values in real market, component values are selected be: C_1 is 1.2 nF, C_2 is 4.7 nF, R_1 is 180 Ω, and R_2 is 10 kΩ, and it causes phase to shift with 0.081108 degrees or around 4.5 μs at 50 Hz of signal delay. This delay is only a half of sample's period which is 10 μs; ADC samples signal only one sample before time matched signal arrived.

Assuming for the worst case, the error of the resistors reached maximum value at 1 %, and the error of the capacitors reached maximum value at 10%; the cut-off frequency is changed as the shifted phase angle also. With equation (24) and the error of the components, the maximum difference of the shifted phase at 50 Hz is 0.009003 degrees but 0.018015 degrees for ± 5 Hz tolerance. The estimated maximum error shall be included to the TVE calculation.

3.3 Analog to Digital Converter (ADC)

Analog to digital converter in this research is ADS8556; it was sampled from Texas Instrument (TI) Company. One chip contains 6 Successive Approximation Register (SAR) ADCs that can simultaneously sample 6 input signals with 16-bit resolution on sampling & hold circuits as internal component block diagram in figure 3-5.

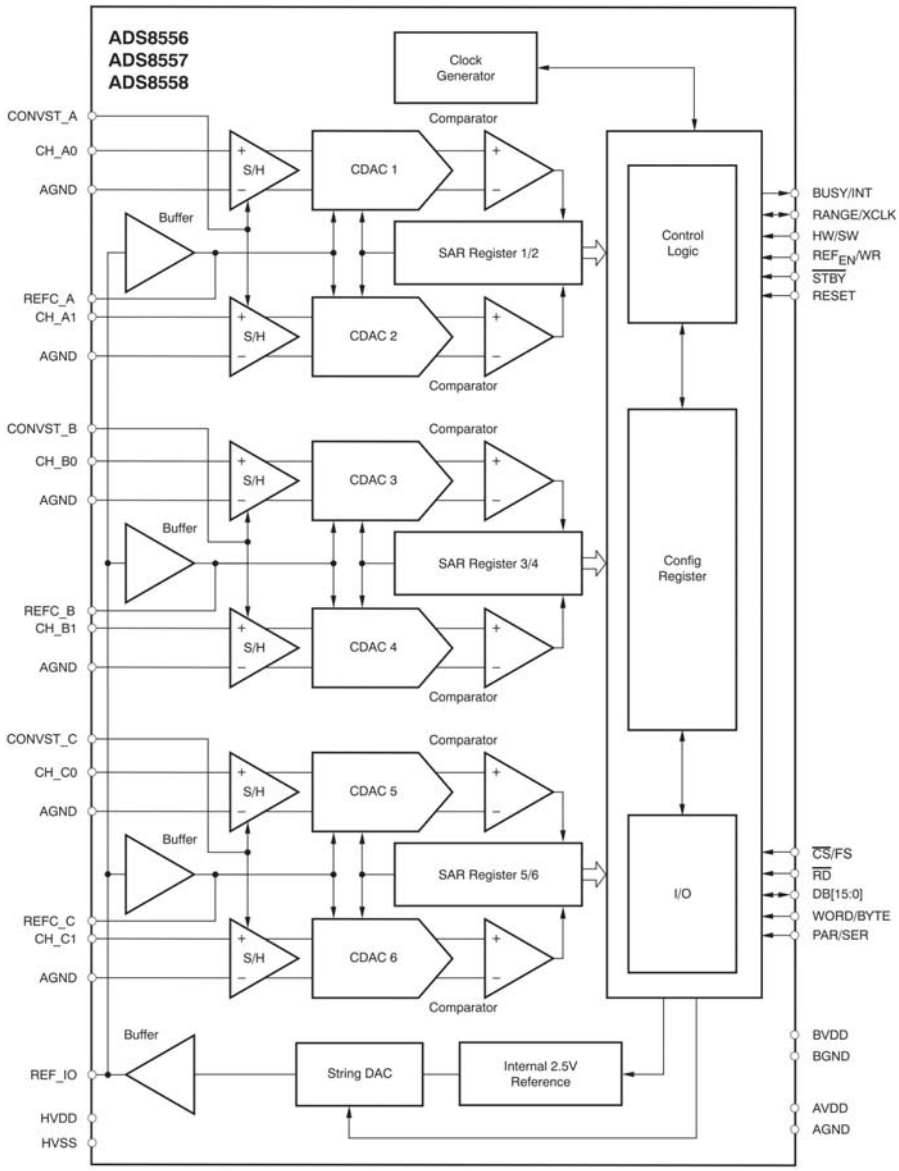

Figure 3-5: ADS8556 Block Diagram.

SAR is a type of ADC, fastest conversion among other types. The simplest way to understand its algorithm is to imagine a voltage range of an ADC as a bottom-state and a top-state, and divide it a half. Then pick a voltage level within the range. If a picked voltage level is equal or greater than half of the range, Most Significant Bit (MSB) becomes logic 1 and the half-voltage level is changed to be the bottom-state of the range as a new range, otherwise the MSB becomes logic 0 and the half-voltage level is changed to be the top-state of the range as a new range. After a new range is assigned, repeat the procedure but change the MSB to a lower bit and a lower bit, until the Least Significant Bit (LSB) is met and defined.

For example, a 4-bit SAR ADC is assigned to convert a voltage level of 7 Volts with a positive 0 to 10 Volts of ADC voltage range. Half of the range is 5 Volts, 7 are greater than 5, and then the MSB become logic 1. The next range is now 5 to 10 Volts and the half is 7.5 Volts, 7 are less than 7.5, then the 3rd-bit become logic 0. The next range is now 5 to 7.5 Volts and the half is 6.25 Volts, 7 are greater than 6.25, the 2nd-bit now become logic 1. The last range is 6.25 to 7.5 Volts and the half is 6.875 Volts, 7 are greater than 6.875, the LSB is logic 1. Thus, the conversion result of this 4-bit SAR ADC is 1011. To check the result, equation (25) needs to be used.

$$V_C = N_D \times \frac{R_F}{2^B} \tag{25}$$

When V_C is a sampling input-voltage level,

N_D is a digital-output of an ADC in decimal,

R_F is the full-voltage range of an ADC,

B is the bit-resolution of an ADC.

Thus the example above has sampling voltage $V_C = 11 \times \frac{10}{2^4} = 6.875$ Volts, and the error is 1.7857%; higher bit resolution shall give error lower than this.

3.4 Micro Controller Unit (MCU)

MCU is the main computation of the PMU and it was selected to be STM32L152VB, a chip from STmicroelectronic Company. For this research, it was configured to run at the maximum speed which is 32 MHz of clock. Figure 3-6 shows internal component of the chip as a block diagram.

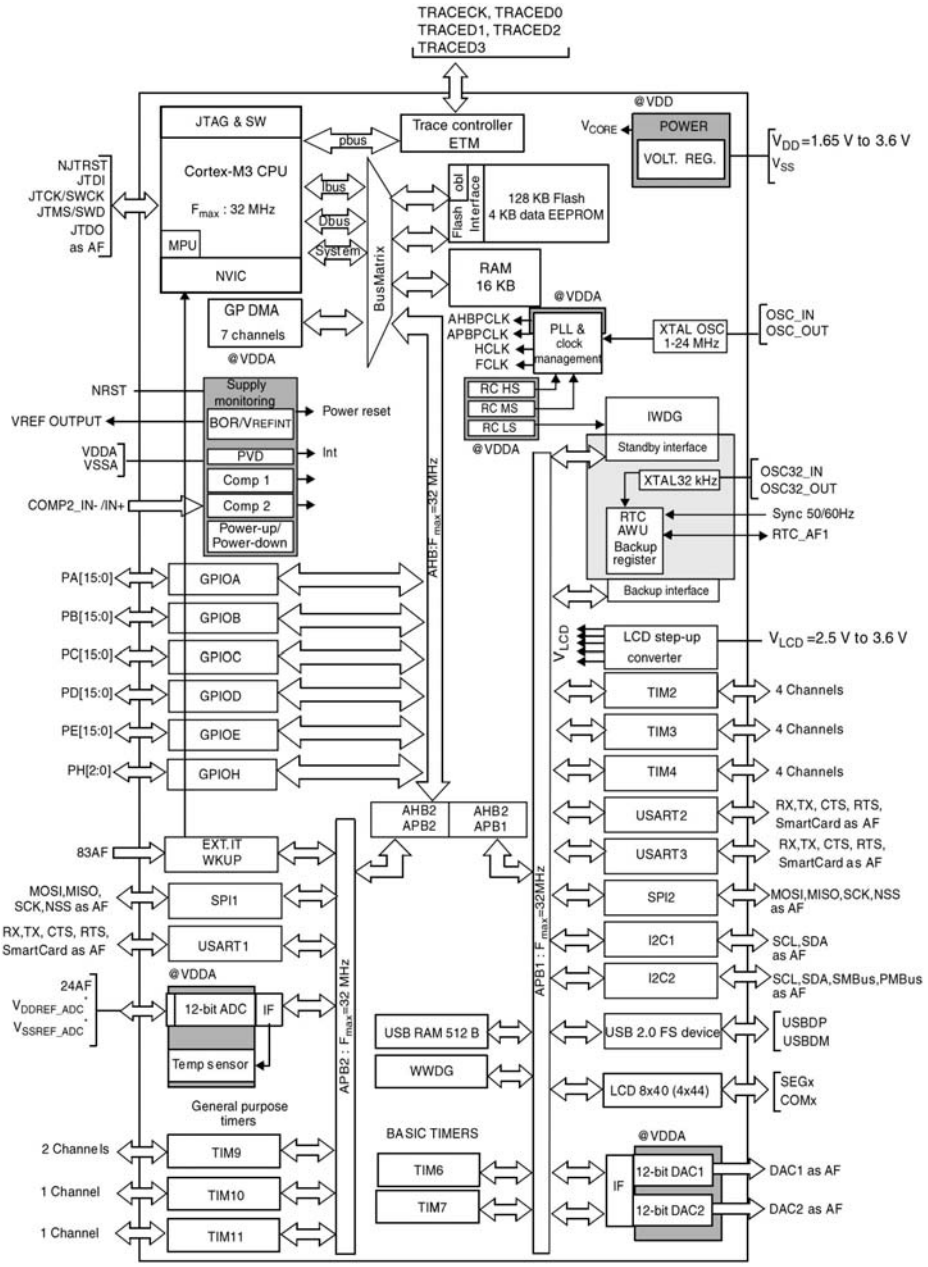

Figure 3-6: STM32L152 Block Diagram.

3.5 GPS and Communication

Global Positioning System (GPS) as described in [5] and [9], it was developed by the U.S. Department of Defense as NAVSTAR-GPS or NAVigation System with Timing And Ranging Global Positioning System. It was also developed by many groups such as the Russian Aerospace Defence Forces as GLONASS which is an acronym for Globalnaya Navigatsionnaya Sputnikovaya Sistema or Global Navigation Satellite System. In this research, the GPS receivers are only capable to receive data from satellites of NAVSTAR-GPS which operate on 6 different orbital planes; the orbits are around 20,180 km above the Earth's surface.

3.5.1 Positioning

GPS satellites normally propagate its position and coordinated universal time (UTC) with 2 carrier frequencies: L1 at 1,575.42 MHz for civilian use, and L2 at 1,227.60 MHz with encrypted code for military use. Each satellite has at least one atomic clock that has maximum error of one second every 30,000 to 1,000,000 years.

To determine position of a receiver, S is an instantaneous distant between satellite and receiver, t be a travel time, and c be the speed of light as is shown in equation (26).

$$S = t \cdot c \tag{26}$$

If there are 2 satellites in the sky, position of the receiver shall be determined as figure 3-7.

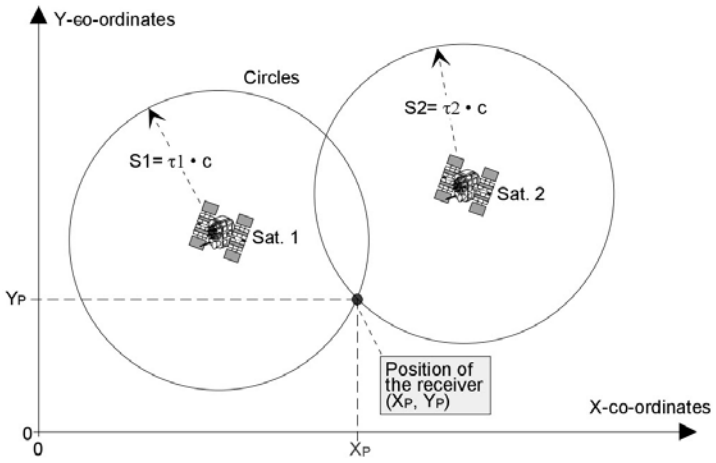

Figure 3-7: Positioning with 2 Satellites.

In reality, precise positioning has to be done on 3-Dimensional (3D) space with 4 unknown variables: longitude (X), latitude (Y), height (Z), and time error (Δt).

LEA-6s form u-blox company is the GPS-chip that is used in this research, the best choice as possible to find in Thai markets. Low-cost GPS-chip with built-in antenna was used before; it took many hours to synchronize to GPS-satellites, or unable to synchronize at all in a day. LEA-6s is capable to use with active antenna; it took 1 minute maximum to synchronize to GPS-satellites as experienced. Figure 3-8 shows a block diagram of the receivers.

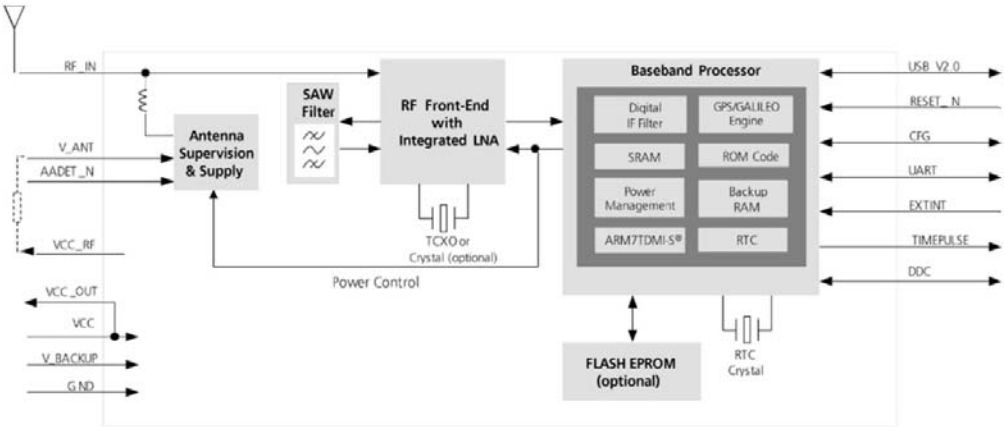

Figure 3-8: GPS Receiver Block Diagram.

3.5.2 Communication

Communication with LEA-6s is done by Universal Asynchronous Receiver/Transmitter (UART); LEA-6s sends out GPS data in National Marine Electronics Association (NMEA) protocol, receives command and configuration in UBX protocol.

NMEA protocol is a standard protocol for Global Navigation Satellite System (GNSS) application which is transmitted in serial interface (TTL or RS-232 voltage level) by using printable 8-bit ASCII characters. In the case of a TTL interface, a logical zero corresponds to 0 V and a logical one corresponds to the operating voltage of the system (3 V … 5 V). In the case of an RS-232 interface, a logical zero corresponds to a positive voltage (+3 V … +15 V) and a logical one a negative voltage (-3 V … -15 V). To understand NMEA protocol, figure 3-9 is very useful, see [5] for more information.

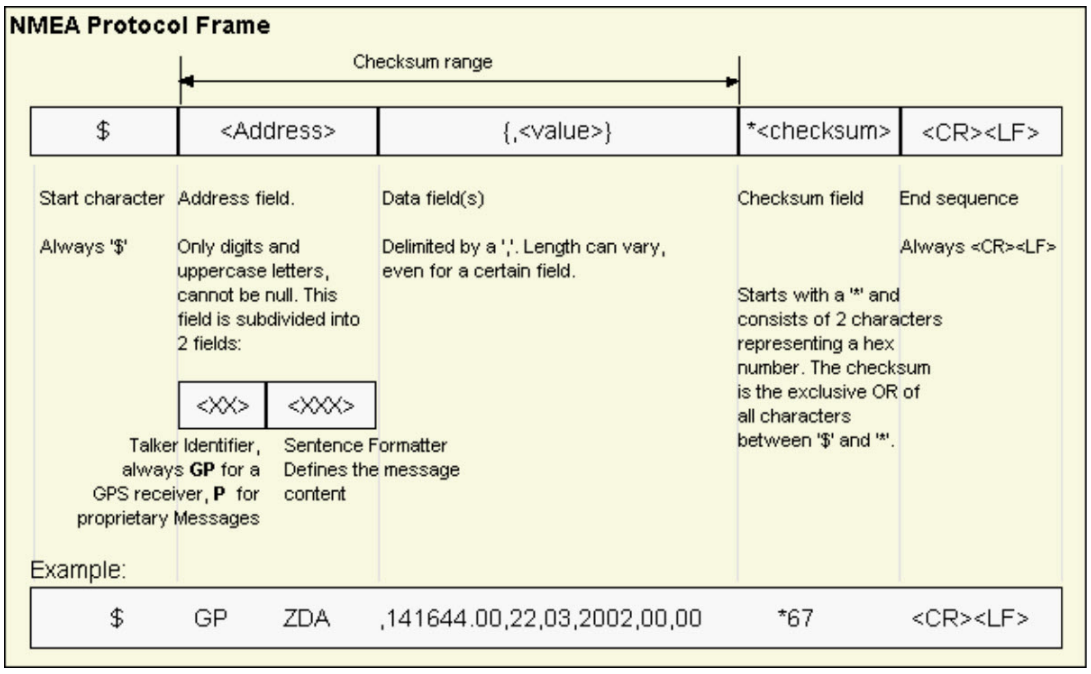

Figure 3-9: NMEA Protocol Frame.

For package example, table 1 shows an example of the Recommended Minimum Specific GNSS Data (RMC) package.

$GPRMC,130304.00,A,4717.115,N,00833.912,E,000.04,205.5,200601,01.3,W*7C<CR><LF>

Information	Description
$	Start character
GP	Information originating from a GPS appliance
RMC	Package identifier
130304.00	UTC time of reception
A	Package quality: A signifies valid (V = invalid)
4717.115	Latitude: 47° 17.115 min
N	Northerly latitude (N = north, S = south)
00833.912	Longitude: 8° 33.912 min
E	Easterly longitude (E = east, W = west)
000.04	Speed: 0.04 knots
205.5	Course: 205.5°
200601	Date: 20th June 2001
01.3	Adjusted declination: 1.3°
W	Westerly direction of declination (E = east)
*	Separator for the checksum
7C	Checksum for verifying the entire package
<CR><LF>	End of the package

Table 1: RMC Package Description.

To command GPS receiver, there is a UBX protocol which is a configuration protocol that is implemented by u-blox to use with their GPS-chips. To understand UBX protocol, it would cost times, see [7] for more information.

Serial-port-monitoring programs were brought to monitor and to test serial communication between “u-center” a GPS application program from u-blox to a GPS chip. Important commands that need to be monitored and used are baud-rate-change and package-disable which are listed in the table 2. Monitored commands are assigned to microcontroller for GPS-chip configuration; this is very useful for time saving. Messages are predictable and could be easier to learn from examples. Note that LEA-6s has no flash memory to store configured commands which are lost every time power is down, and needs to resent the commands every time power is on which causes no problem on MCU to do the procedure.

Commands	Monitored Message in Hexadecimal
Disable all GGA output	0xB5, 0x62, 0x06, 0x01, 0x08, 0x00, 0xF0, 0x00, 0x00, 0x00, 0x00, 0x00, 0x00, 0x01, 0x00, 0x24, 0xB5, 0x62, 0x06, 0x01, 0x02, 0x00, 0xF0, 0x00, 0xF9, 0x11
Disable all GLL output	0xB5, 0x62, 0x06, 0x01, 0x08, 0x00, 0xF0, 0x01, 0x00, 0x00, 0x00, 0x00, 0x00, 0x01, 0x01, 0x2B, 0xB5, 0x62, 0x06, 0x01, 0x02, 0x00, 0xF0, 0x01, 0xFA, 0x12
Disable all GSA output	0xB5, 0x62, 0x06, 0x01, 0x08, 0x00, 0xF0, 0x02, 0x00, 0x00, 0x00, 0x00, 0x00, 0x01, 0x02, 0x32, 0xB5, 0x62, 0x06, 0x01, 0x02, 0x00, 0xF0, 0x02, 0xFB, 0x13
Disable all GSV output	0xB5, 0x62, 0x06, 0x01, 0x08, 0x00, 0xF0, 0x03, 0x00, 0x00, 0x00, 0x00, 0x00, 0x01, 0x03, 0x39, 0xB5, 0x62, 0x06, 0x01, 0x02, 0x00, 0xF0, 0x03, 0xFC, 0x14
RMC to UART1 only	0xB5, 0x62, 0x06, 0x01, 0x08, 0x00, 0xF0, 0x04, 0x00, 0x01, 0x00, 0x00, 0x00, 0x01, 0x05, 0x45, 0xB5, 0x62, 0x06, 0x01, 0x02, 0x00, 0xF0, 0x04, 0xFD, 0x15
Disable all VTG output	0xB5, 0x62, 0x06, 0x01, 0x08, 0x00, 0xF0, 0x05, 0x00, 0x00, 0x00, 0x00, 0x00, 0x01, 0x05, 0x47, 0xB5, 0x62, 0x06, 0x01, 0x02, 0x00, 0xF0, 0x05, 0xFE, 0x16
Baud rate change 9600 to 115200	0xB5, 0x62, 0x06, 0x00, 0x14, 0x00, 0x01, 0x00, 0x00, 0x00, 0xD0, 0x08, 0x00, 0x00, 0x00, 0xC2, 0x01, 0x00, 0x03, 0x00, 0x03, 0x00, 0x00, 0x00, 0x00, 0x00, 0xBC, 0x5E, 0xB5, 0x62, 0x06, 0x00, 0x01, 0x00, 0x01, 0x08, 0x22

Table 2: LEA-6 Monitored Command.

As table 2, RMC is the only GPS package that is used in this research, outputs at UART1 of the GPS receiver and the baud rate is changed to 115,200 bps (bit per second).

3.6 Display Module

Display phasors on computer is the main plot of this research but sometime display on a display module would be more convenient to test the prototype. The display module is selected to be BL12864G a monochrome graphic Organic Light Emitter Diode (OLED) display module with the reasons of high contrast, good brightness, and an interesting display for learning.

The module is received data by the 8-bit parallel pins (DB0 … DB7) which are connected to 8-pin lower of port D (PD0 … PD 7) of the MCU as shown in figure 3-10. Command pins (/RES, WR, and RS) are controlled by 3-bit lower of port B (PB0, PB1, and PB3 respectively) of the MCU, and the DISP pin is forced to VDD to prevent sleep-mode entering. As experiment, the CS pin can be forced to GND and RD can be forced to VDD without caused any error.

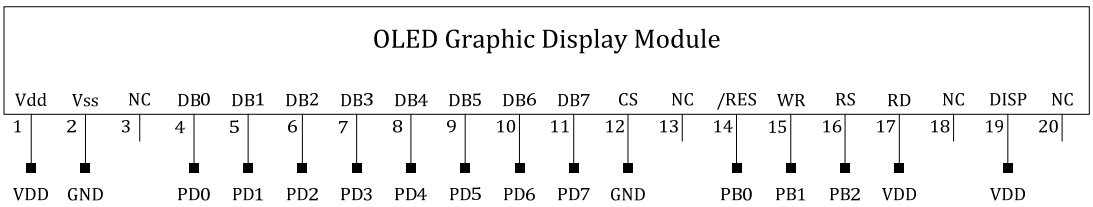

Figure 3-10: OLED Pin-Out Connection.

Graphic display is not a general character display that receives an ASCII code to display a character but it contains pixels as a dot matrix that is free to display as a digital image. Thus, every character has to be designed then be defined as a grope of hexadecimal value before it is sent to show as a character. Figure 3-11 shows a displaying example of 2 characters as “Px” in a dot matrix. The characters are defined to be 6 dots in width and 8 dots in length, or are known as 6x8 characters; ‘P’ is defined as a hexadecimal sequence of {0x00, 0x7F, 0x09, 0x09, 0x09, and 0x06} and ‘x’ is defined to be {0x00, 0x6C, 0x10, 0x10, 0x6C, and 0x00}. Note that the sequences are continuously sent through the 8-bit parallel pins; the addresses or pixel lines are shifted automatically.

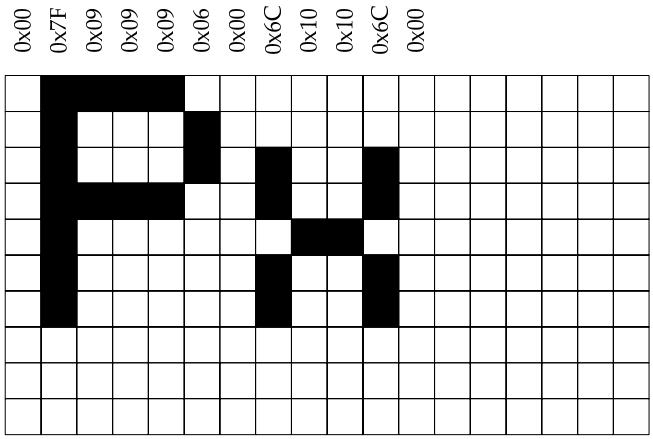

Figure 3-11: Graphic Display Example.

Figure 3-12 shows an actual displaying example of the module.

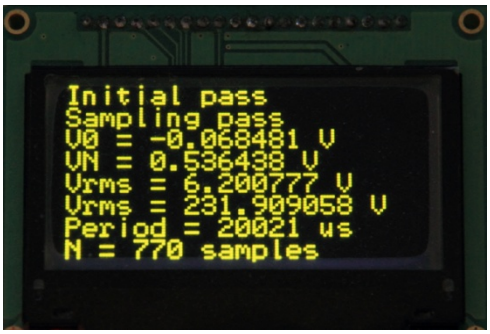

Figure 3-12: OLED Display Example.

CHAPTER IV

SOFTWARE DESIGN

In this research, implemented software is designed for MCU only. It manipulates MCU to control peripherals and do calculation. The procedure on PMU is to sample input signal, receives time data from GPS, estimates phasor, and then outputs phasor to display module or computer. Figure 4-1 is the main picture for this chapter which is modified for easy understands, and details will be given by the following contents.

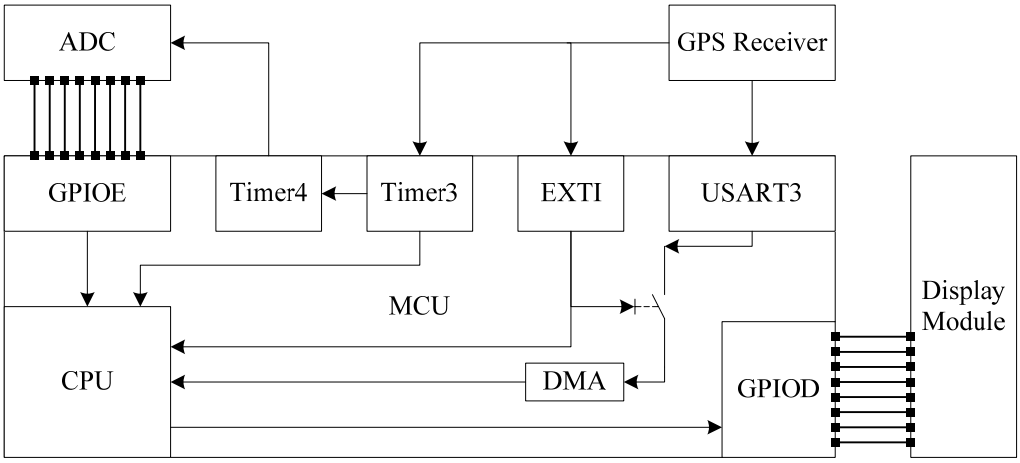

Figure 4-1: PMU Internal Block Diagram.

4.1 Initialization

The software is beginning with an initialization process as is represented in figure 4-2.

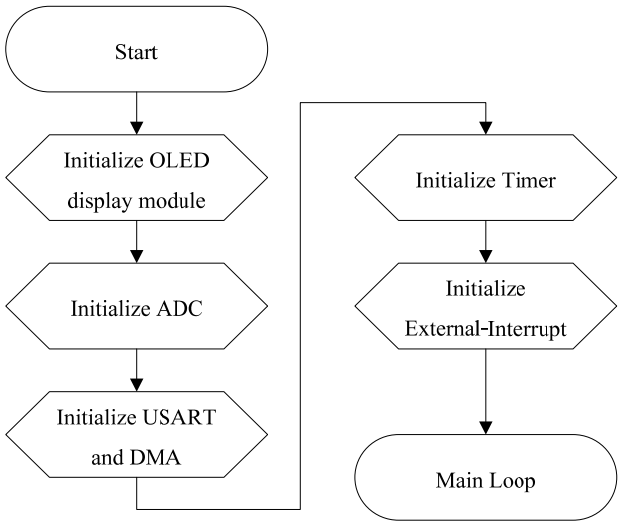

Figure 4-2: Initialization Flowchart.

4.2 Timer Behavior

There are 2 timers that are mainly used in the prototype; Timer3 is used as the time reference, and Timer4 is used as the DAC trigger. In figure 4-3, there are case of 1PPS exist and case of no 1PPS; details are describe by following content. Note that TIM3 and TIM4 are Timer3 (timer number 3) and Timer4 (timer number 4) respectively which were named after MCU's datasheet.

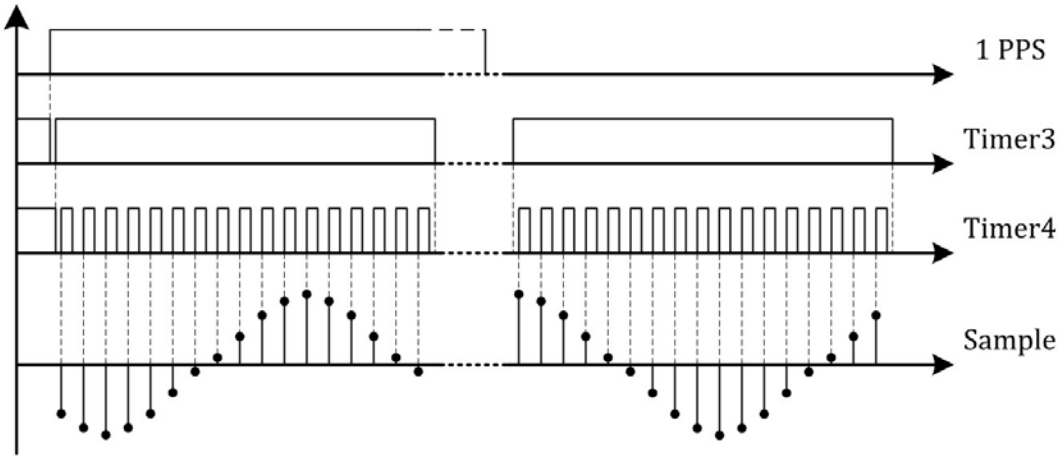

Figure 4-3: Timing Diagram Example.

4.2.1 Timer3

Since GPS time pulse is a 1 pulse per second (1PPS) signal, Timer3 is used as the GPS synchronized time-reference to provide the reference for every phase measuring as the timing diagram in figure 4-3, and to control reporting rate on both 10 and 25 frames per second. Timer3 is synchronized to GPS time pulse by using rising edge of GPS time pulse to reset the counter with a small delay that lower than 100 ns before the counter starts new counting; this makes Timer3 more reliable to be the time reference for phase measuring which synchronizes to all PMUs also. There might be error due to crystal error within a second but for only a second.

4.2.2 Timer4

Timer 4 is used as a DAC trigger, outputs PWM to the DAC chip to start conversion but only when Timer3 gives it permission as the timing diagram in figure 4-3; Timer3 outputs high to enable Timer4 counter and outputs low to disable Timer4 counter. After Timer4 is disabled, its counter is set to steady at maximum value which is left only 1 clock before it is overflow; this gives predictable delay time on next event.

4.3 Interrupt

4.3.1 EXTI Interrupt

External interrupt (EXTI) is assigned to indicate a rising edge of GPS time pulse. The service routine of external interrupt (EXTI-IRQ) resets frame number (Nframe) and enables DMA as shown in figure 4-4.

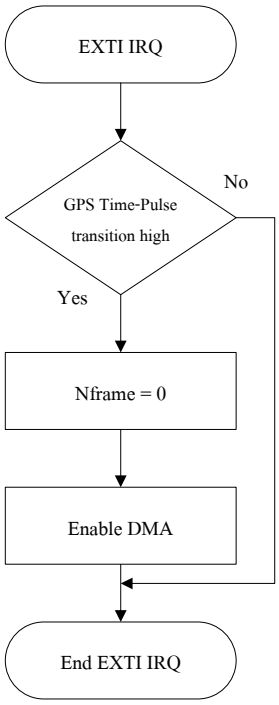

Figure 4-4: EXTI-IRQ Flowchart.

4.3.2 DMA Interrupt

In figure 4-5, Time-Update flag is a software flag; it is created to indicate that a time data from GPS has been received and ready to be converted to UNIX time to stamp on a phasor. This flag is set only by the DMA interrupt service routine (DMA-IRQ) which services an interrupt after last DMA buffer array is written.

DMABuffer is an array that temporarily accumulates data from GPS which is transferred from USART register by DMA.

Alignment and reliability of received data have to be checked by matching '$' and 'A' on DMABuffer[0] and DMABuffer[17] respectively, see RMC package example in chapter 3 for reason and more information.

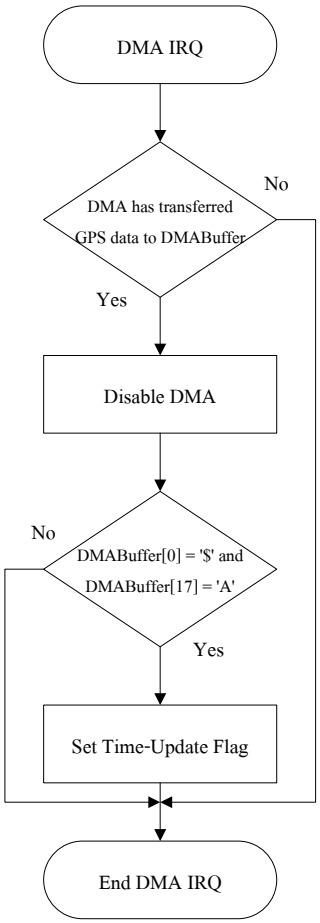

Figure 4-5: DMA-IRQ Flowchart.

4.4 Main Loop

In this section, figure 4-6 shows the main loop flowchart which is a non-stop loop.

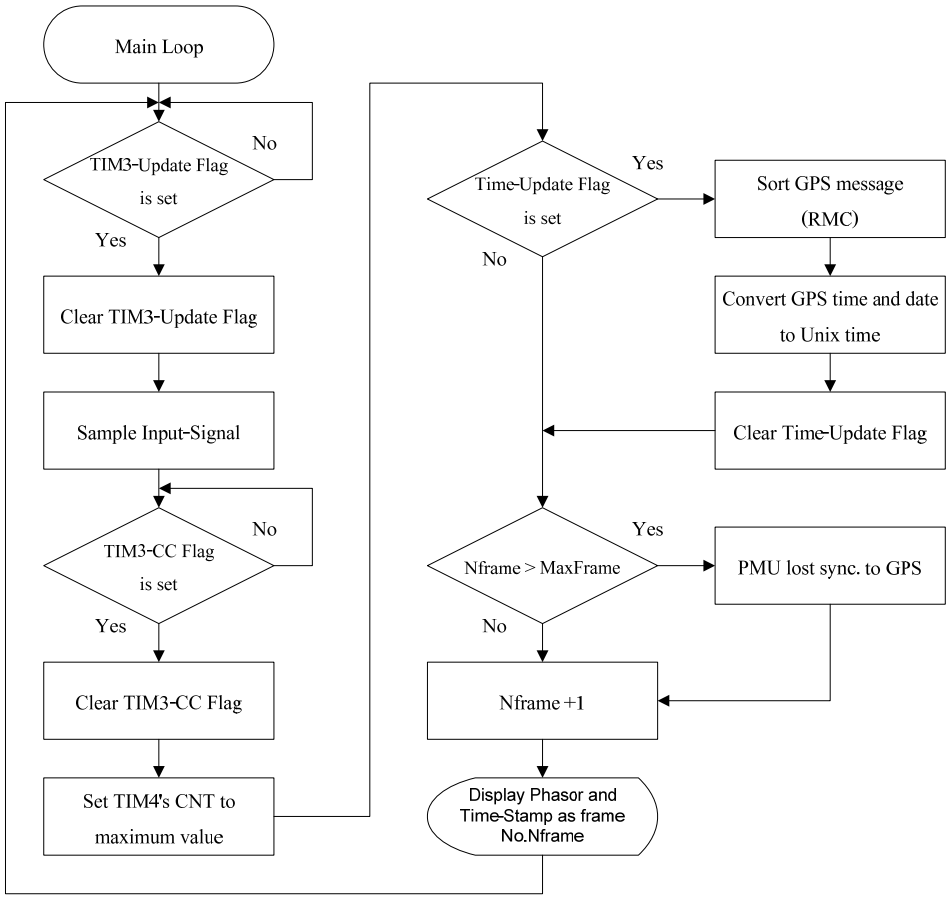

Figure 4-6: Main Loop Flowchart.

From figure 4-6, TIM3-Update flag is a status flag of Timer3; it is automatically set when the counter reaches the overflow or has been reset. TIM3-CC flag also be a status flag but it is set only when the counter matches the compare value, and Timer4 is stopped (no activity on ADC).

The variable “Nframe” is increased by one in every time the main loop is ending a course. If Nframe’s value exceed MaxFrame which indentifies reporting rate (10 or 25 frames per second), lost of synchronization is indicated.

4.4.1 Sample Input-Signal

This minor section is a phasor estimation process that has procedure to sample input signal, identifies the sign of samples to indicate zero-crossing event for phase estimation, accounts samples for RMS magnitude estimation, and then estimates phasor.

Figure 4-7 shows the over-view of both sampling method and is used to describe the procedures. After state of the time reference is changed to logic high at point A, sampling process begins to sample input signal.

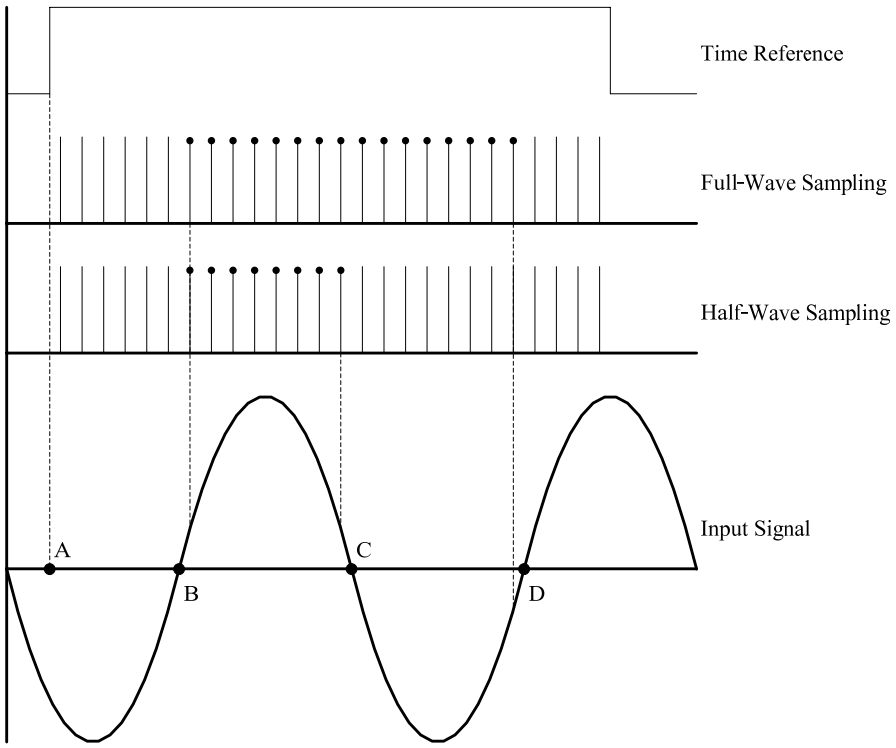

Figure 4-7: Sampling Method Over-View.

For full-wave sampling method, MCU controls ADC to sample input signal without sample accounting until point B is reached or positive zero-crossing is found. After point B, samples are accounted as black-head pike in figure 4-7 until point D or 2nd positive zero-crossing is found; samples after point D are discarded. Magnitude is calculated by using equation (7) but phase angle and frequency are calculated as equation (27) and (28) respectively.

$$Phase = \frac{N_P \cdot R_D}{N} \quad (27)$$

$$Frequency = \frac{f_S}{N} \quad (28)$$

Where N_P is number of sample from point A to point B,

R_D is degree range of signal (360 for full-wave, and 180 for half-wave),

N is number of sample from point B to point D,

f_s is sampling frequency.

Half-wave sampling method is similar to full-wave sampling method but sampling range. For half-wave, after point B is reached, sample accounting is done only from point B to point C or between two nearest zero-crossing (one positive and one negative). Estimation of Magnitude, phase, and frequency use the same equation as full-wave but N is changed to number of sample from point B to point C or between two nearest zero-crossing. Note that for half-wave, magnitude on positive side or negative side are not specified which one is to be used, but positive zero-crossing and half period have to be found.

As experiments, the fastest reporting rate is 25 frames per second which can not be done with full-wave sampling due to limitation of frequency clock, nor with the three-phase signal, not even half-wave sampling. Thus the outputs of the prototype are three-phase half-wave sampling on 10 frames per second of reporting rate for normal operation, and single-phase half-wave sampling on 25 frames per second of reporting rate for rapid requirement of phasor. Figure 4-8 shows a flowchart of half-wave sampling.

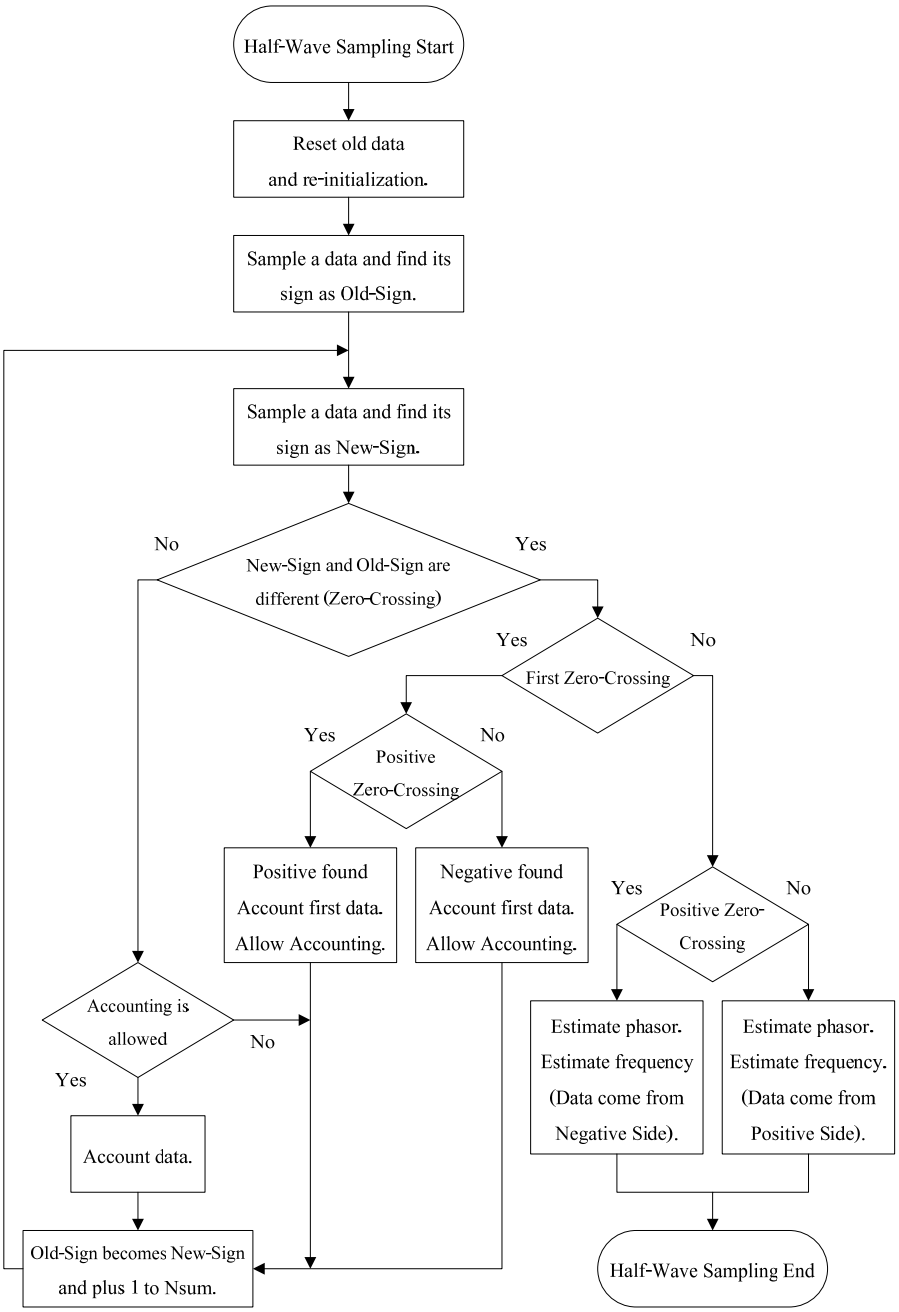

Figure 4-8: Half-Wave Sampling Flowchart.

As flowchart in figure 4-8, zero-crossing is indicated by using sign difference between two samples due to ADC's output which is binary twos complement.

Phase angle and frequency are calculated by using the variable "Nsum".

4.4.2 GPS Message Sorting

This section is a RMC package exacting which is created to convert ASCII data from RMC package to decimal values for unix-time calculation.

4.4.3 Unix-Time Calculation

Unix-Time is a second counting, started from 00.00 a.m. of January 1, 1970. It is widely used as time-stamp for measurement result, and appeared as SOC (Second-of-Century) in communication message of IEEE Standard C37.118. The calculation has 2 branches for year of 365 days and year of 366 days as flowchart in figure 4-9. Note that, a time data from GPS has been checked in DMA-IRQ before running this process, and this process is designed for year 2001 and after.

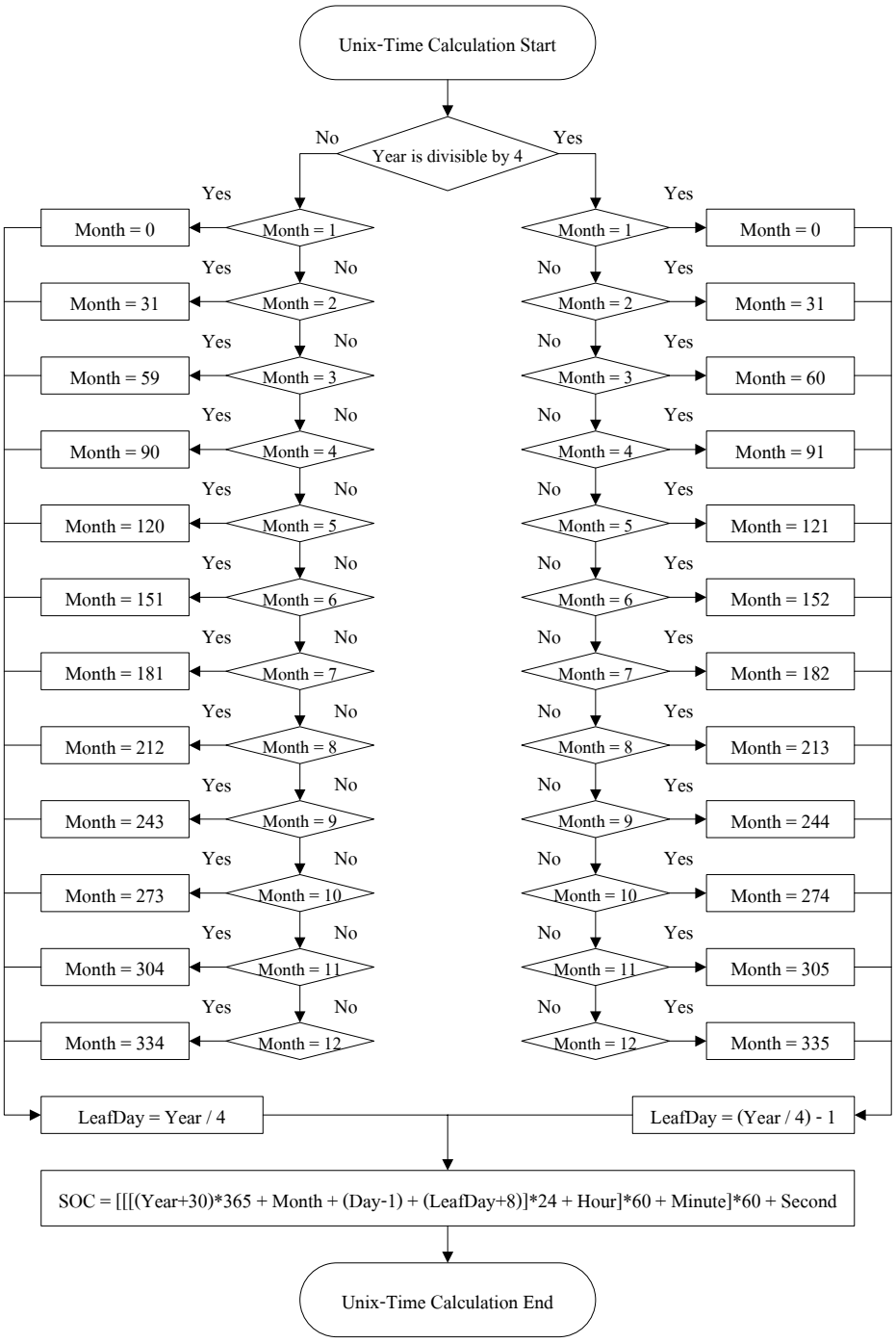

Figure 4-9: Unix-Time Calculation Flowchart.

CHAPTER V

EXPERIMENT

Since this research has no supported commercial or standard PMU device to reference, the experiment is then divided into 2 sections as magnitude experiment and phase experiment with equivalent TVE calculation to equation (8). Note that the prototype outputs both magnitude and phase as phasor as usual but testing devices have their own limitation.

Figure 5-1 shows that vector T (Estimated Phasor) is different from vector R (Theoretical Phasor) by vector Er. Due to no supported commercial or standard PMU device to reference, phase angle error of A degrees is unknown. If magnitude of vector T and vector R is fixed, and different phase angle is also fixed, TVE shall be the same at any phase angle of vector R. Thus phase angle from magnitude experiment can be discarded, and maximum phase angle error of A degrees can be found by phase experiment. Together, vector T can be estimated, and TVE between vector T and vector R shall be found.

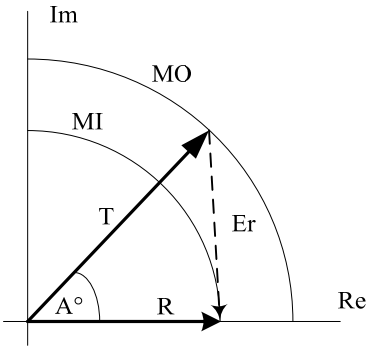

Figure 5-1: TVE Mapping.

5.1 Magnitude Experiment

In magnitude experiment, CALSOURCE200 is used as the AC signal source that output signals to the sensors of the prototype. But it does not support GPS time pulse synchronization, thus the results in this section are just percentage error that came from magnitude comparing between results from the prototype and results from PRS 1.3 which is a 3-phase portable reference standard with class 0.05 % accuracy. Note that percentage errors are calculated from 600 magnitude samples, not just in graph.

The prototype was mainly designed to test with 50 Hz signal of 220 V_{RMS}. But the specification in the research boundary was made before, thus the prototype was then tested with RMS magnitude signal of 10% (22 V), 80% (176 V), 100% (220 V), and 120% (264 V) with frequency of 45 Hz, 50 Hz, and 55 Hz on each voltage signal. Figure 5-2, 5-3, 5-4, and 5-5 show a sample of the first 20 phasors from three-phase magnitude experiment results within 2 seconds on 10 frames per second of reporting rate; graph of magnitude in VRMS versus sample's number is displayed on the left while graph of magnitude's frequency in Hz versus sample's number is displayed on the right.

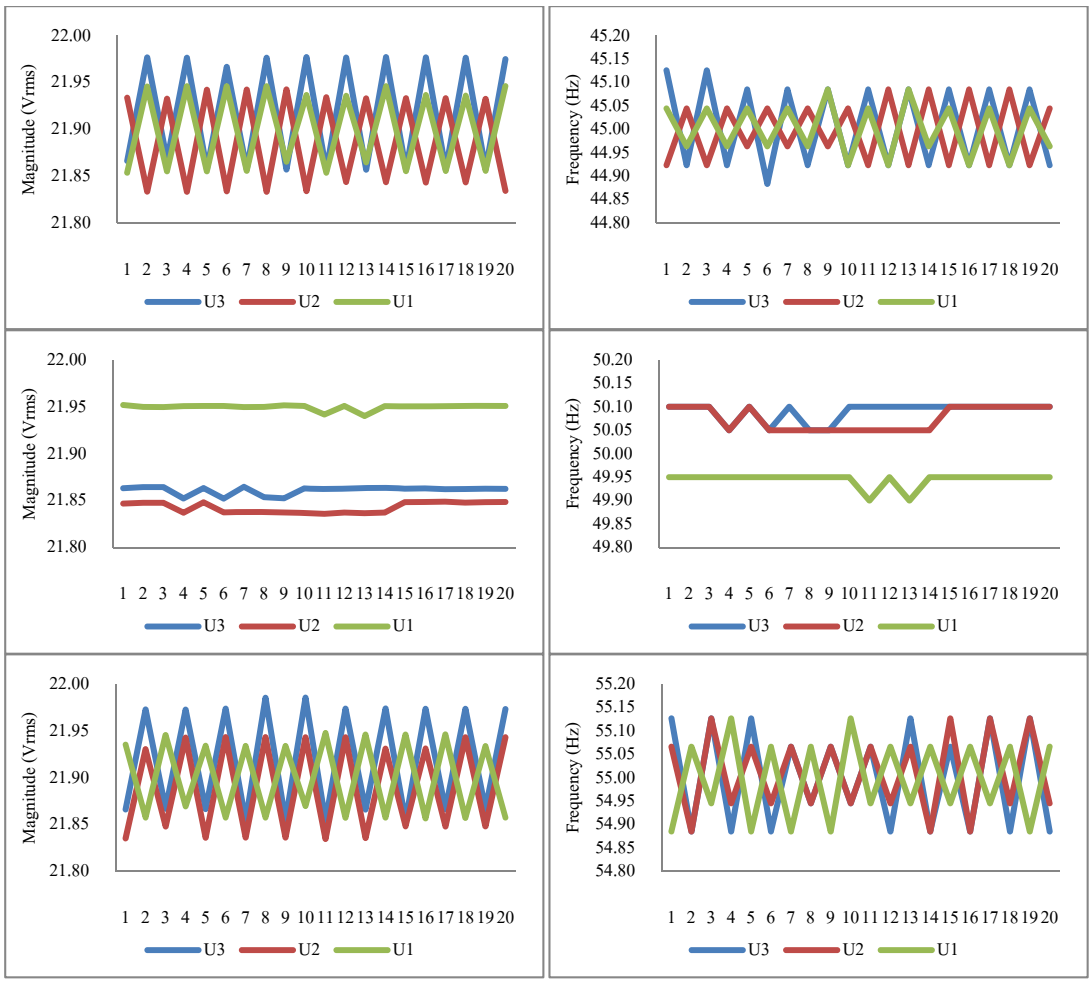

Figure 5-2: Sample of Three-Phase 22 V_{RMS} Experiment Result.

Figure 5-2 shows that the value frequently swings in 45 Hz and 55 Hz results. This could be the effects from low voltage of around 600 mV_{RMS} in front of ADC which can be easily interfered by noise, especially from digital part. And the different of the frequency could cause effect in 45 Hz and 55 Hz results; it is quite stable on 50 Hz.

V_{RMS} results from PRS 1.3 at 45 Hz are 22.024 for U3, 21.992 for U2, and 22.005 for U1. With the same order, at 50 Hz are 22.026, 21.994, and 22.006. And at 55 Hz are 22.026, 21.991, and 22.003. Thus the maximum percentage error of three-phase 22 V_{RMS} experiment is 0.8106 % for 45 Hz, 0.7981 % for 50 Hz, and 0.7881 % for 55 Hz.

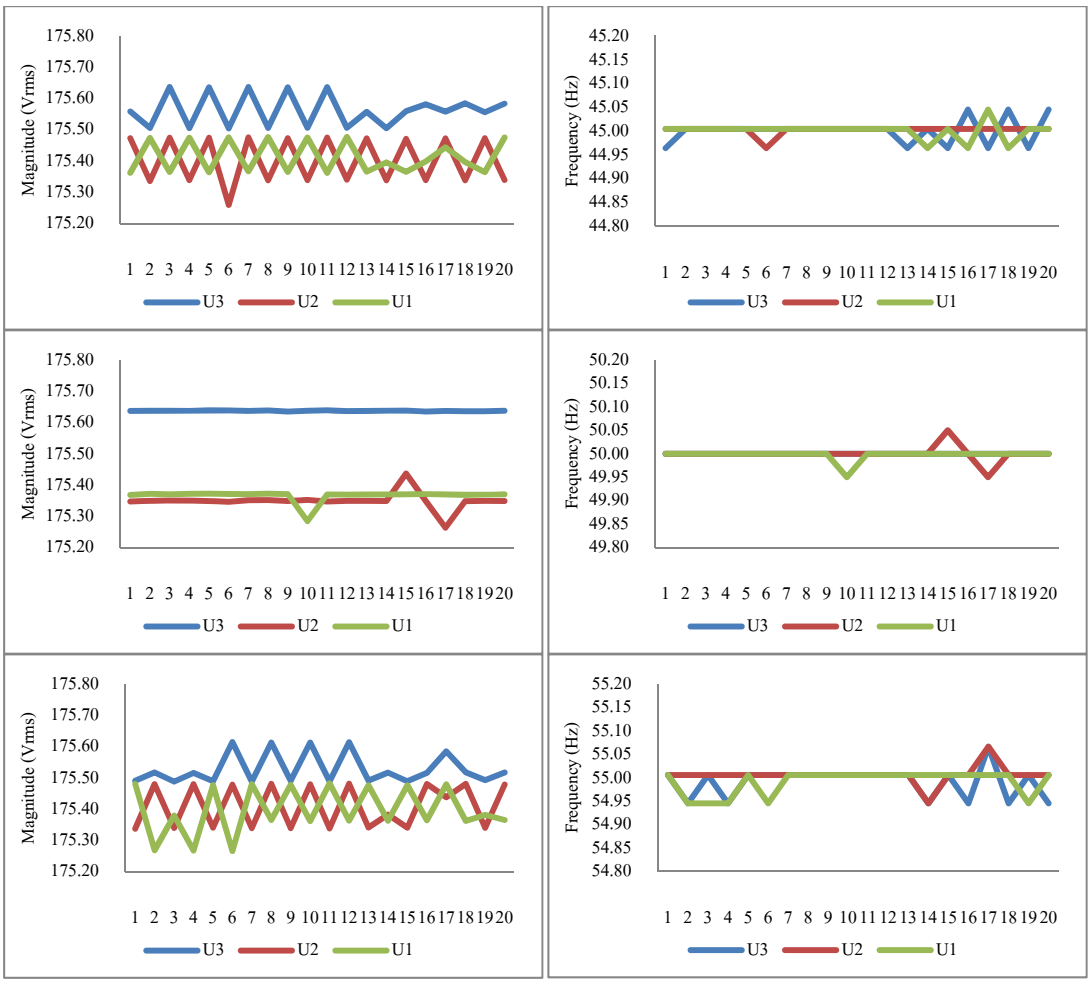

Figure 5-3: Sample of Three-Phase 176 V_{RMS} Experiment Result.

Frequency changing in figure 5-3 is not frequently as figure 5-2; might be the higher voltage that improve zero-crossing finder algorithm, and improve the results.

V_{RMS} results from PRS 1.3 at 45 Hz are 176.16 for U3, 176.00 for U2, and 176.03 for U1. With the same order, at 50 Hz are 176.16, 176.00, and 176.03. And at 55 Hz are 176.16, 175.99, and 176.02. Thus the maximum percentage error of three-phase 176 V_{RMS} experiment is 0.4226 % for 45 Hz, 0.4275 % for 50 Hz, and 0.4461 % for 55 Hz.

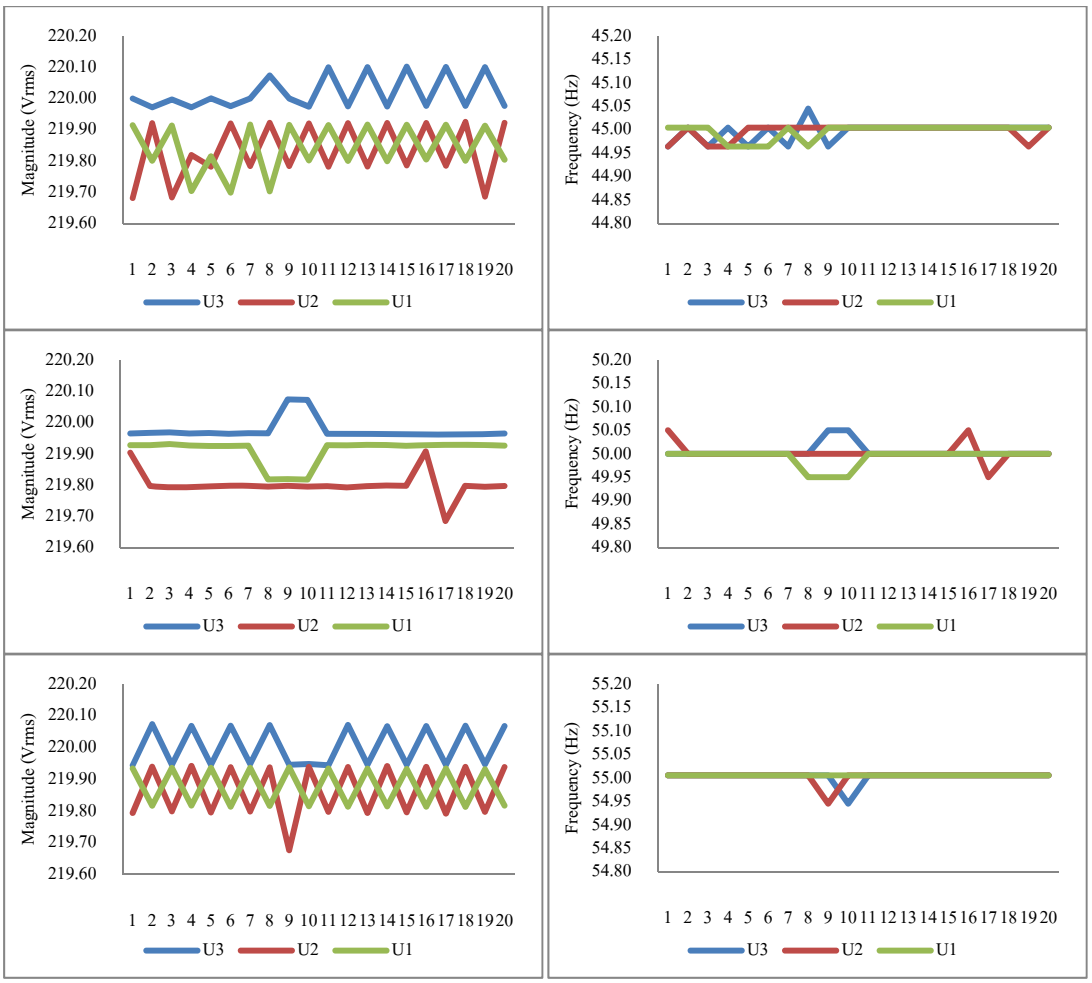

Figure 5-4: Sample of Three-Phase 220 V_{RMS} Experiment Result.

The graphs in figure 5-4 are similar to graphs in figure 5-3 but the constant multiplier is designed for 220 V_{RMS} which is used to multiply estimated magnitude back to undivided magnitude, thus the results in this range are the best of the prototype.

V_{RMS} results from PRS 1.3 at 45 Hz are 220.08 for U3, 219.90 for U2, and 219.94 for U1. With the same order, at 50 Hz are 220.08, 219.91, and 219.93. And at 55 Hz are 220.08, 219.89, and 219.92. Thus the maximum percentage error of three-phase 220 V_{RMS} experiment is 0.1101 % for 45 Hz, 0.1062 % for 50 Hz, and 0.1125 % for 55 Hz.

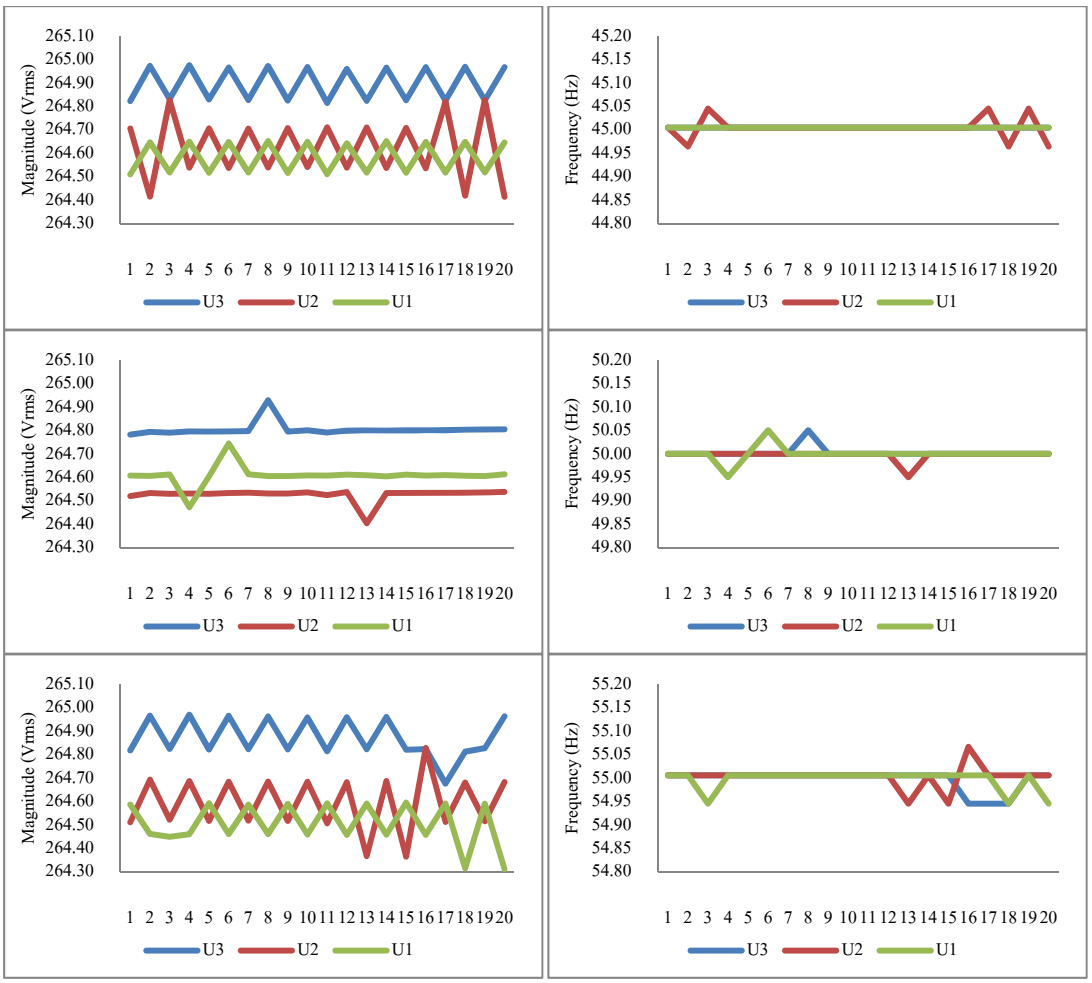

Figure 5-5: Sample of Three-Phase 264 V_{RMS} Experiment Result.

V_{RMS} results from PRS 1.3 at 45 Hz are 264.06 for U3, 263.85 for U2, and 263.91 for U1. With the same order, at 50 Hz are 264.06, 263.86, and 263.89. And at 55 Hz are 264.05, 263.84, and 263.88. Thus the maximum percentage error of three-phase 264 V_{RMS} experiment is 0.3737 % for 45 Hz, 0.3442 % for 50 Hz, and 0.3814 % for 55 Hz.

From now on, figure 5-6, 5-7, 5-8, and 5-9 show a sample of single-phase magnitude experiment results within a second on 25 frames per second of reporting rate.

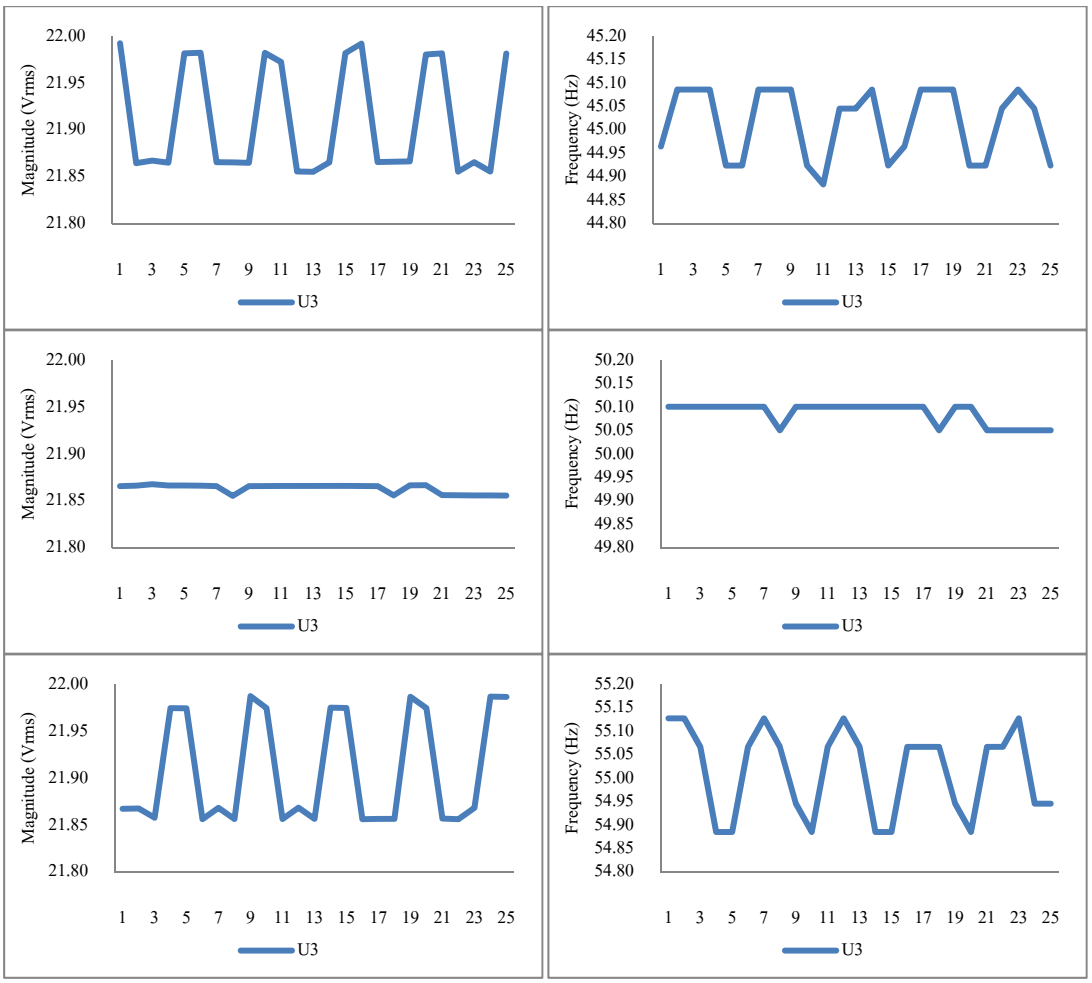

Figure 5-6: Sample of Single-Phase 22 V_{RMS} Experiment Result.

V_{RMS} results from PRS 1.3 are 22.026 for 45 Hz, 22.027 for 50 Hz, and 22.027 for 55 Hz. Thus the maximum percentage error of single-phase 22 V_{RMS} experiment is 0.7794 % for 45 Hz, 0.7866 % for 50 Hz, and 0.8277 % for 55 Hz.

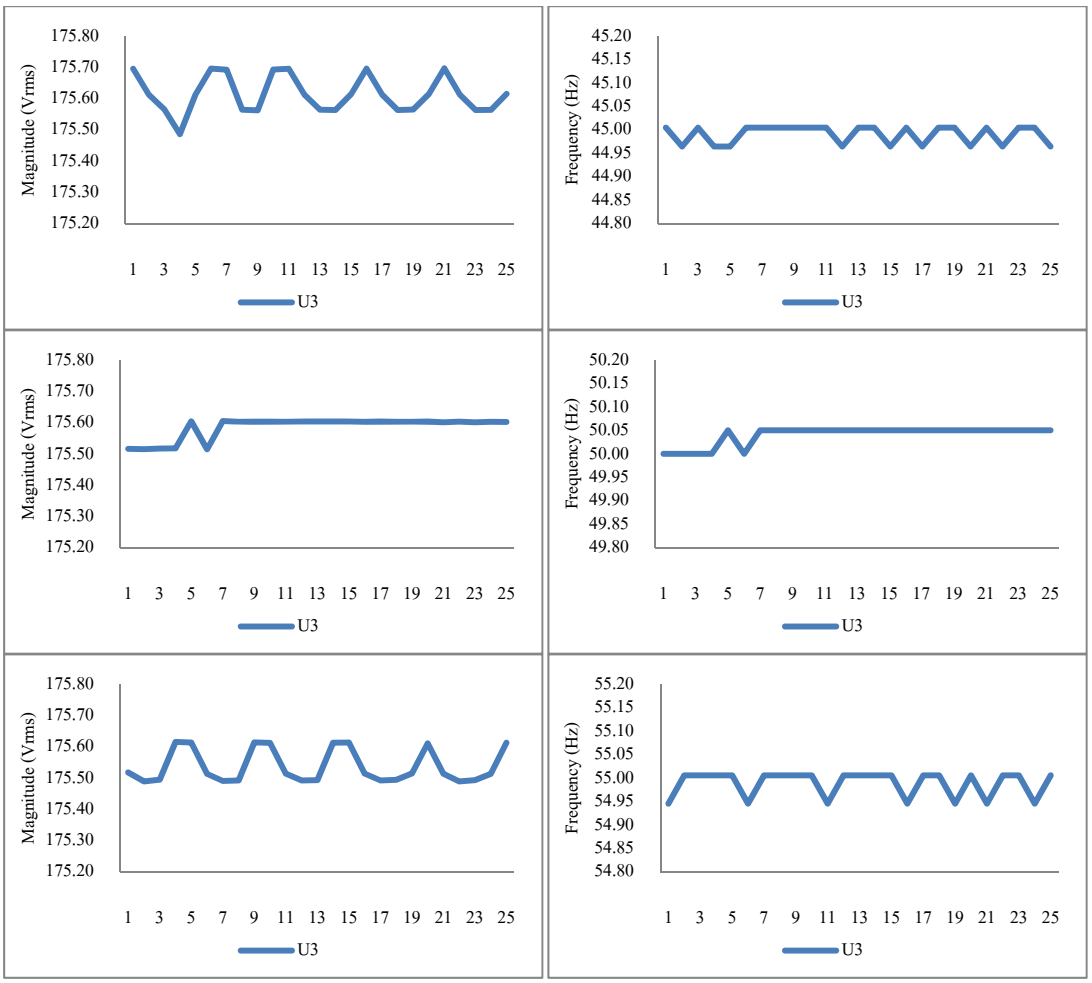

Figure 5-7: Sample of Single-Phase 176 V_{RMS} Experiment Result.

V_{RMS} results from PRS 1.3 are 176.17 for 45 Hz, 176.17 for 50 Hz, and 176.17 for 55 Hz. Thus the maximum percentage error of single-phase 176 V_{RMS} experiment is 0.3896 % for 45 Hz, 0.4209 % for 50 Hz, and 0.4412 % for 55 Hz.

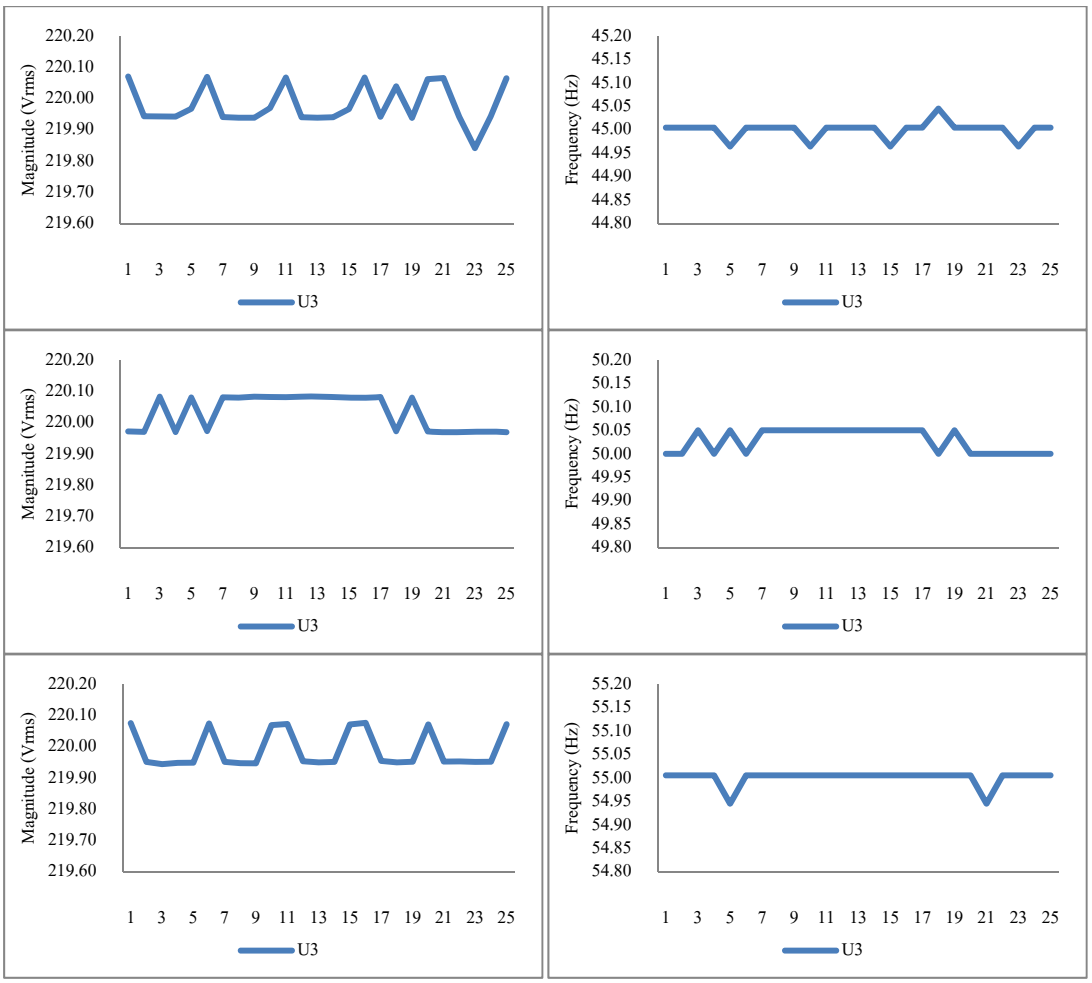

Figure 5-8: Sample of Single-Phase 220 V_{RMS} Experiment Result.

V_{RMS} results from PRS 1.3 are 220.09 for 45 Hz, 220.09 for 50 Hz, and 220.09 for 55 Hz. Thus the maximum percentage error of single-phase 220 V_{RMS} experiment is 0.1157 % for 45 Hz, 0.1040 % for 50 Hz, and 0.1186 % for 55 Hz.

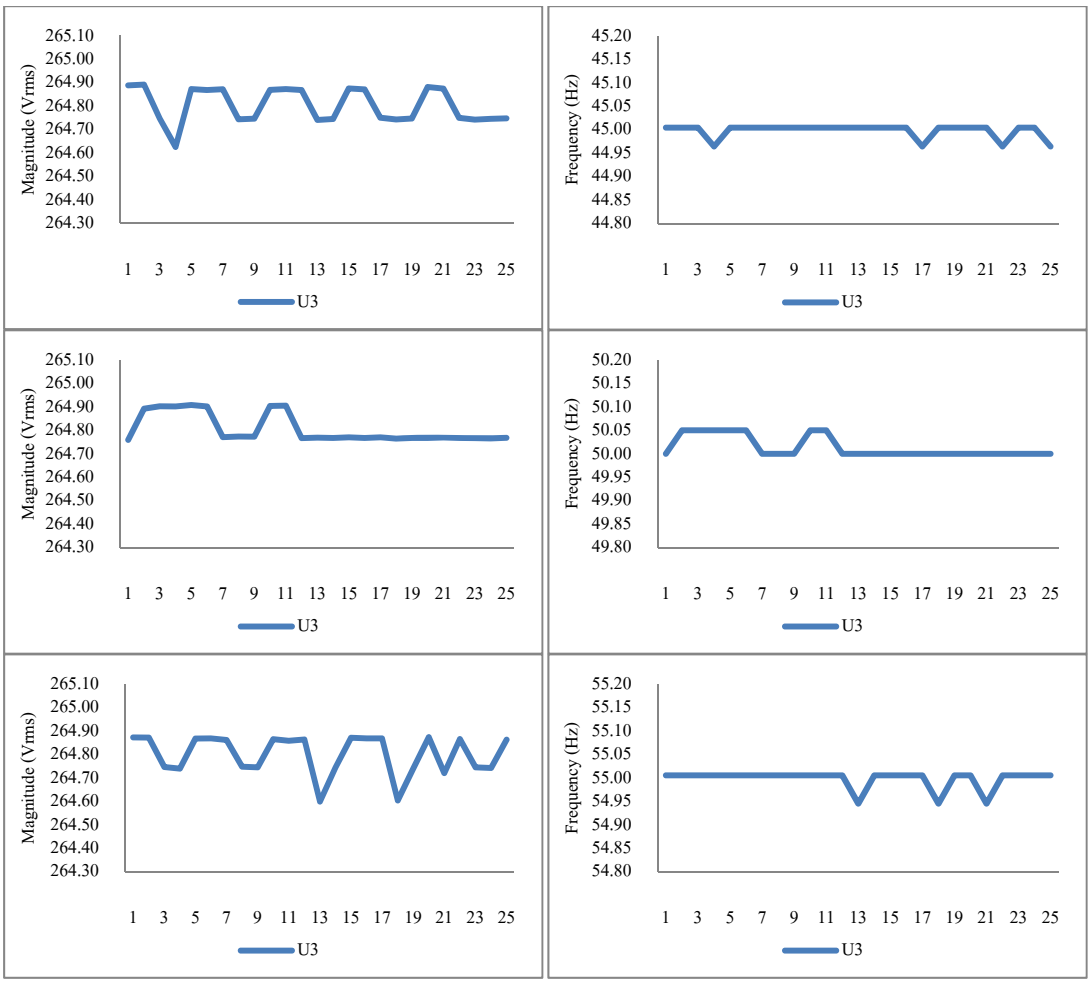

Figure 5-9: Sample of Single-Phase 264 V_{RMS} Experiment Result.

V_{RMS} results from PRS 1.3 are 264.06 for 45 Hz, 264.07 for 50 Hz, and 264.05 for 55 Hz. Thus the maximum percentage error of single-phase 264 V_{RMS} experiment is 0.3603 % for 45 Hz, 0.3294 % for 50 Hz, and 0.3206 % for 55 Hz.

5.2 Phase Experiment

The idea of this experiment is to show that if input signal of PMU is ideal 50 Hz sinusoidal waveform, the prototype should outputs constant phase angle. In real life, ideal 50 Hz source is hardly to craft; only GPS clock is reliable and affordable. Thus a GPS synchronized sinusoidal source is designed in the idea of independent crystal clock and independent GPS receiver for the GPS synchronized sinusoidal source and the prototype. If output phase angles are constant or swing narrowly around a point, the prototype might be considered as acceptable device.

5.2.1 Hardware

The GPS synchronized sinusoidal source requires only one MCU and one GPS receiver. But its output signal stands in the range of positive side, thus a simple passive high-pass filter is required to shift the signal down as a real AC signal before entering the anti-aliasing part of the prototype. Figure 5-10 shows a simple hardware block diagram of the phase experiment.

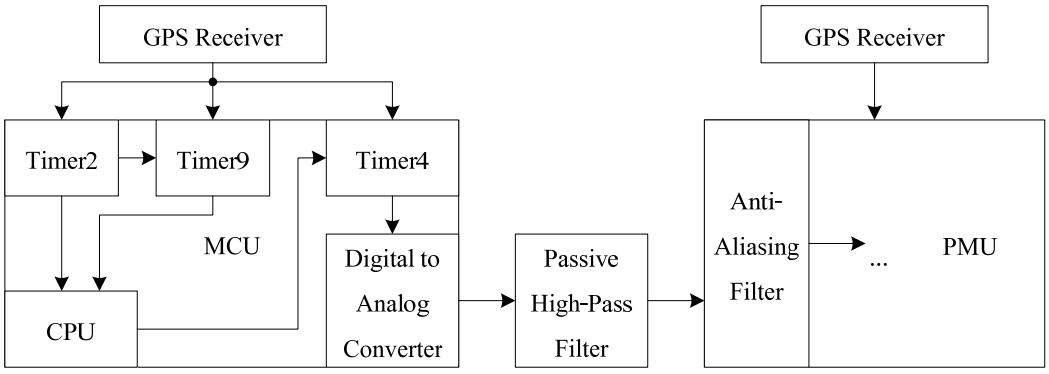

Figure 5-10: Phase Experiment Hardware Block Diagram.

16-bit Timer2 and Timer9 are cascaded as a 32-bit timer to count number of system clock (32 MHz) in every period of 1 second. Timer2 runs as the least significant timer that gives Timer9 the most significant timer 1 counting when it reached overflow.

After rising edge of GPS time pulse occurred, Timer2 and Timer9 are reset, and their counting values are send to compare with the theoretical value in CPU; clock frequency error shall be computed to adjust Timer4 period.

Timer4 is designed to be the DAC trigger, and also be synchronized to GPS time pulse. Its period defines output sample period, and effects output signal frequency.

5.2.2 Software

The DAC's output is driven by 500 samples of sine waveform in a look-up table. And there are 2 interrupt service routines (IRQ) from Timer2 and Timer4 that drive MCU of the GPS synchronized sinusoidal source.

The Timer2-IRQ does clock error calculation by using counter values from Timer2 and Timer4 as is shown in figure 5-11.

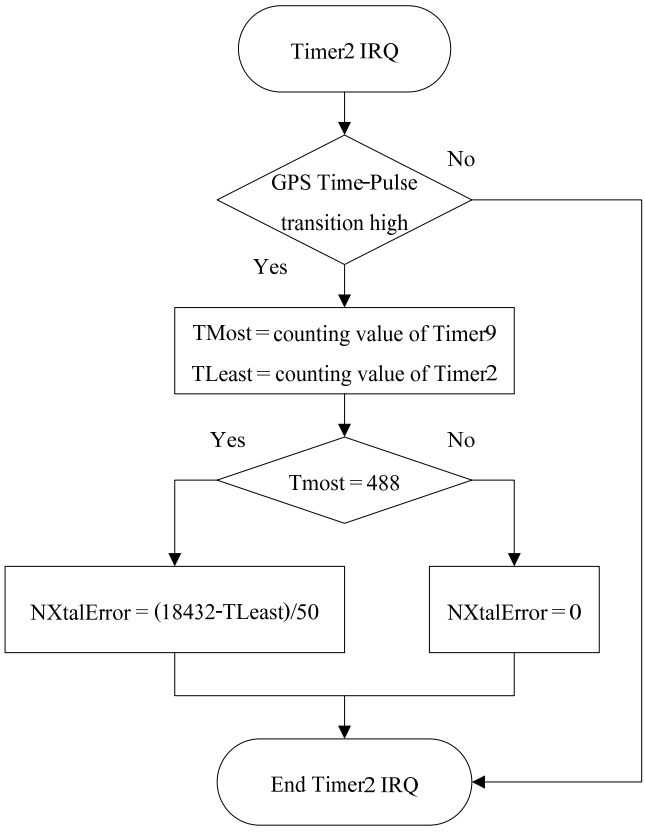

Figure 5-11: Clock Error Computation on Timer2 IRQ Flowchart.

The counter values are compared to theoretical values which are 488 for Timer9 and 18432 for Timer2. If counter value of Timer9 is not 488, GPS receiver must be lost of synchronization; clock error should not be calculated, and Timer4 period shall not be adjusted. If crystal is error, number of different clock shall be divided by 50 before it is

used to adjust output waves (50 waves per second). Thus output signal of GPS synchronized sinusoidal source is equal period or frequency which is close to 50 Hz as it could.

For Timer4-IRQ, there is a process of DAC value setup and DAC output signal adjusting as is shown in figure 5-12.

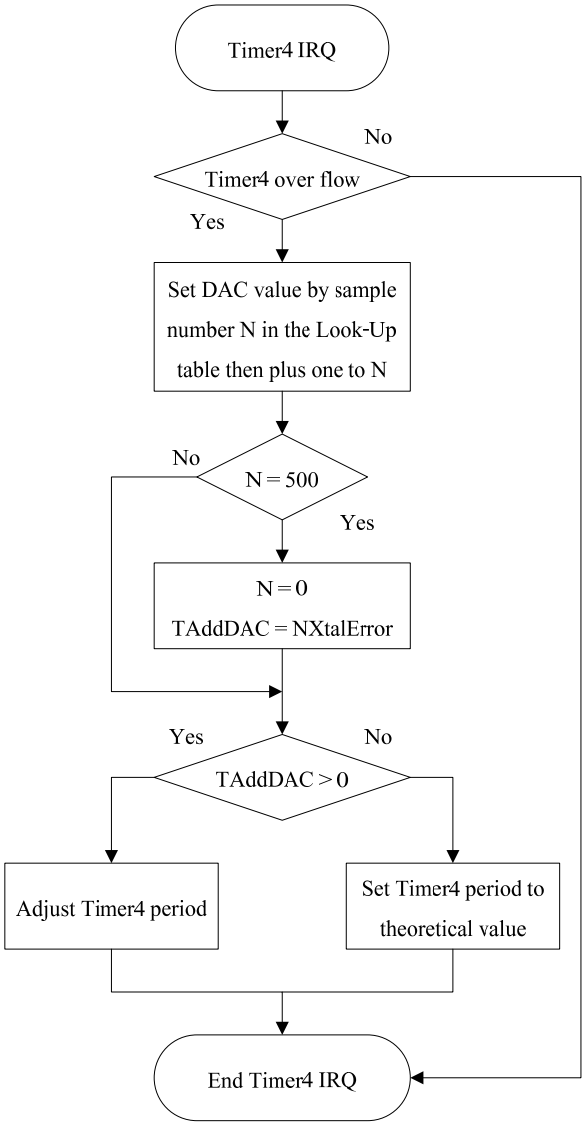

Figure 5-12: Period Adjusting of DAC Trigger on Timer4 Flowchart.

N variable is limited to 500 due to total number of sample in sine wave look-up table. Timer4 period or DAC output signal is adjusted only when previous wave is totally out for wave smoothing and periodic. If no clock error, Timer4 period shall be set to default value.

5.2.3 Result

Phase angle results from 100 kHz of sampling frequency are constant and prove nothing. Thus the sampling frequency is doubled, and the result is given as in figure 5-13 which shows a sample of phase angle variation within 3 seconds on 10 frames per second of reporting rate. Note that reporting rate effect nothing to the phase estimation accuracy.

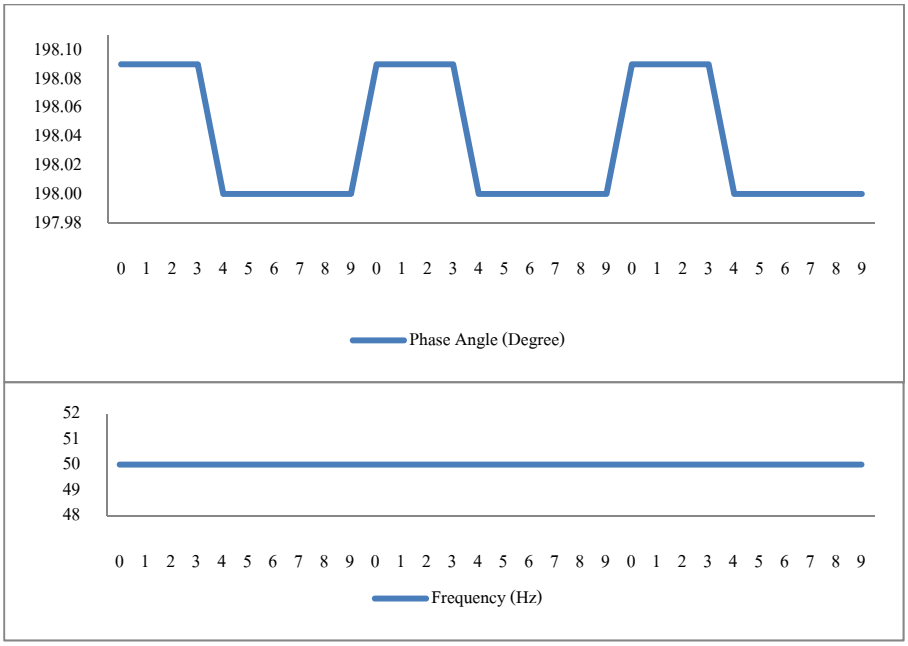

Figure 5-13: Phase Angle Result of 200 kHz Sampling Frequency.

Figure 5-13 shows that phase angle was swung while its frequency was constant. Be reminded that the sampling frequency was changed to 200 kHz or 5 µs/sample for 50 Hz system; delay of 5 µs causes phase angle to shift for 0.09 degrees which is the error of phase estimation.

As result, phase angle swung to 198.09 degrees every 0^{th} frame of a second which was caused by the action of GPS time pulse reset timer of the prototype (sampling clock resetting). And swung back to 198.00 degrees every 4^{th} frame of a second which was caused by crystal clock error of the prototype; clock errors were accumulated for 4 frames or around 0.4 second before phase error reached 5 μs (0.09 degrees) or 1 sample which is only a half of 10 μs, and that is why phase angles were constant on 100 kHz of sampling frequency.

5.3 TVE Analysis and Result

After GPS time pulse rose to high logic, the actual phasor at that rising edge is delayed by anti-aliasing filter while the inside of the prototype has its own delay on Timer3 and Timer4, thus sampling process begins before actual phasor arrival as is shown in Figure 5-14.

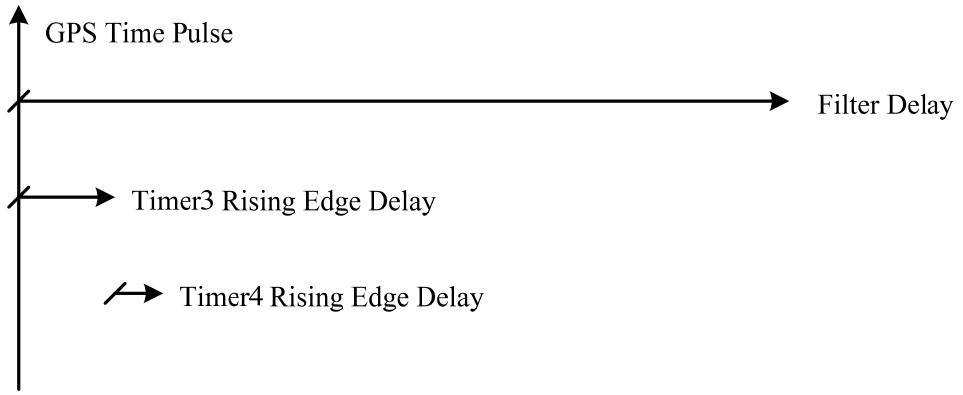

Figure 5-14: Delay Mapping.

Moreover, GPS time pulse has its own delay by its cable; the cable is 5 meter long of RG174 solid polyethylene coaxial cable type. With experiment result in [1], total delay for GPS time pulse was claimed to be 25.26247 ns with possible error of 0.02789 ns.

Stable delay was considered as constant delay and used to adjust phase angle result directly. But unstable delay was considered as error that increased TVE. The delays were summarized as in the table 3.

Delay Caused Part	Constant Delay (ns)	± Maximum Error (ns)
GPS time pulse	25.263	60 + 0.028
Timer3	200	5 + 0.002
Timer4	92	5 + 0.002
Total	317.263	70.032

Table 3: Delay Summary.

Note that 60ns of GPS time pulse delay was archived by the datasheet of the GPS receiver, delay of Timer3 and Timer4 were obtained by using TDS3014B the oscilloscope; 5 ns is a round-up maximum delay from experiment, and 0.002 ns is a delay from the oscilloscope's accuracy in its datasheet which is 0.002 % at 100 ns/div.

As table 3, total constant delay is equivalent to 0.005711 degrees at 50 Hz with maximum error of 0.000571 degrees for ± 5 Hz tolerance when converted to shifted angle. With 0.081108 degrees of the shifted phase at 50 Hz from anti-aliasing filter in figure 5-14, the prototype samples first data before arrival of actual phasor with 0.075397 degrees.

Moreover, the unstable delay of 70.032 ns is equivalent to 0.001261 degrees at 50 Hz or 0.001381 degrees for ± 5 Hz tolerance. With maximum phase estimation error of 0.198 degrees from section 5.2.3, the maximum error of 0.018015 degrees from anti-aliasing filter, and total constant delay conversion error of 0.000571 degrees, the maximum unstable angle becomes 0.217847 degrees.

The unstable angle effects directly to TVE, with result from magnitude experiment; vector T in figure 5-1 was then re-created. Figure 5-15, 5-16, 5-17, and 5-18 show a sample of TVE results on three-phase signal.

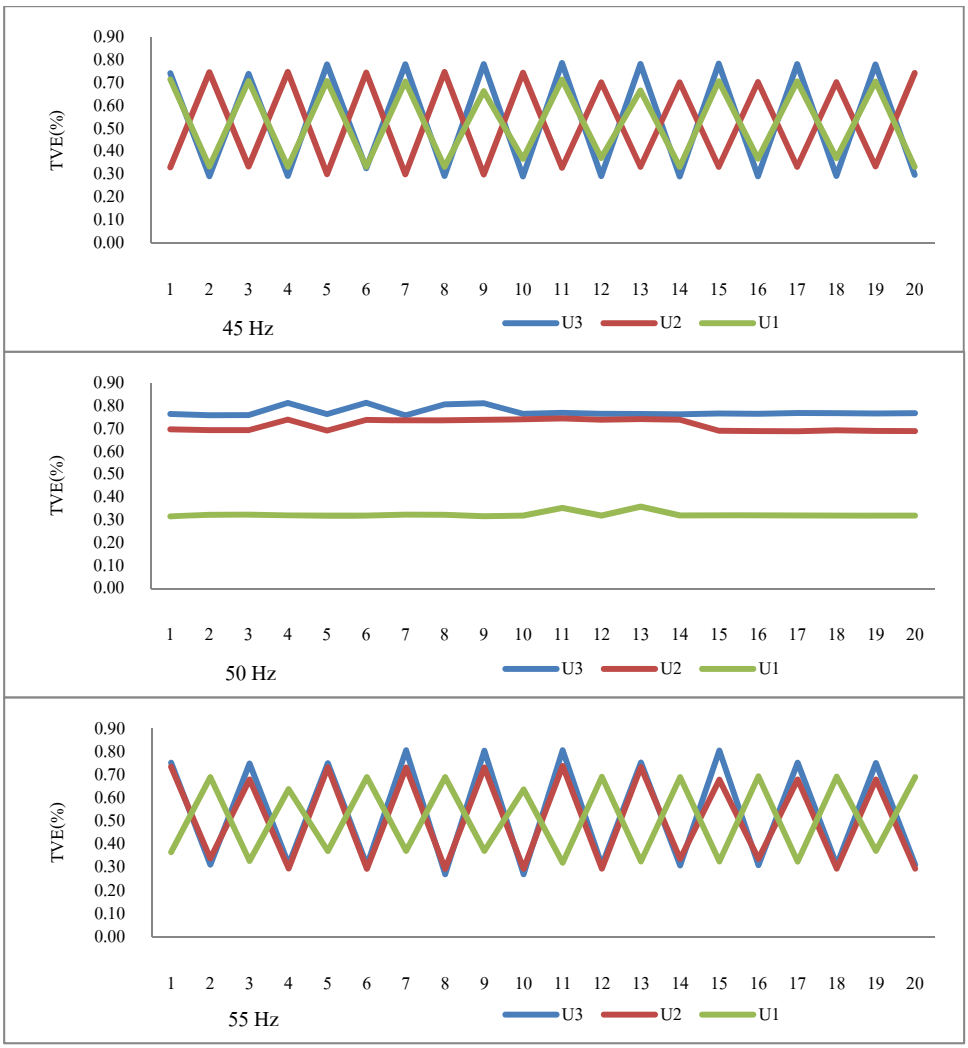

Figure 5-15: Sample of Three-Phase 22 V_{RMS} TVE Result.

Maximum percentage TVEs of three-phase 22 V_{RMS} experiment at 45 Hz are 0.8947 for U3, 0.8554 for U2, and 0.8292 for U1. With the same order, at 50 Hz are 0.8835, 0.8159, and 0.4885. And at 55 Hz are 0.8744, 0.8534, and 0.8167.

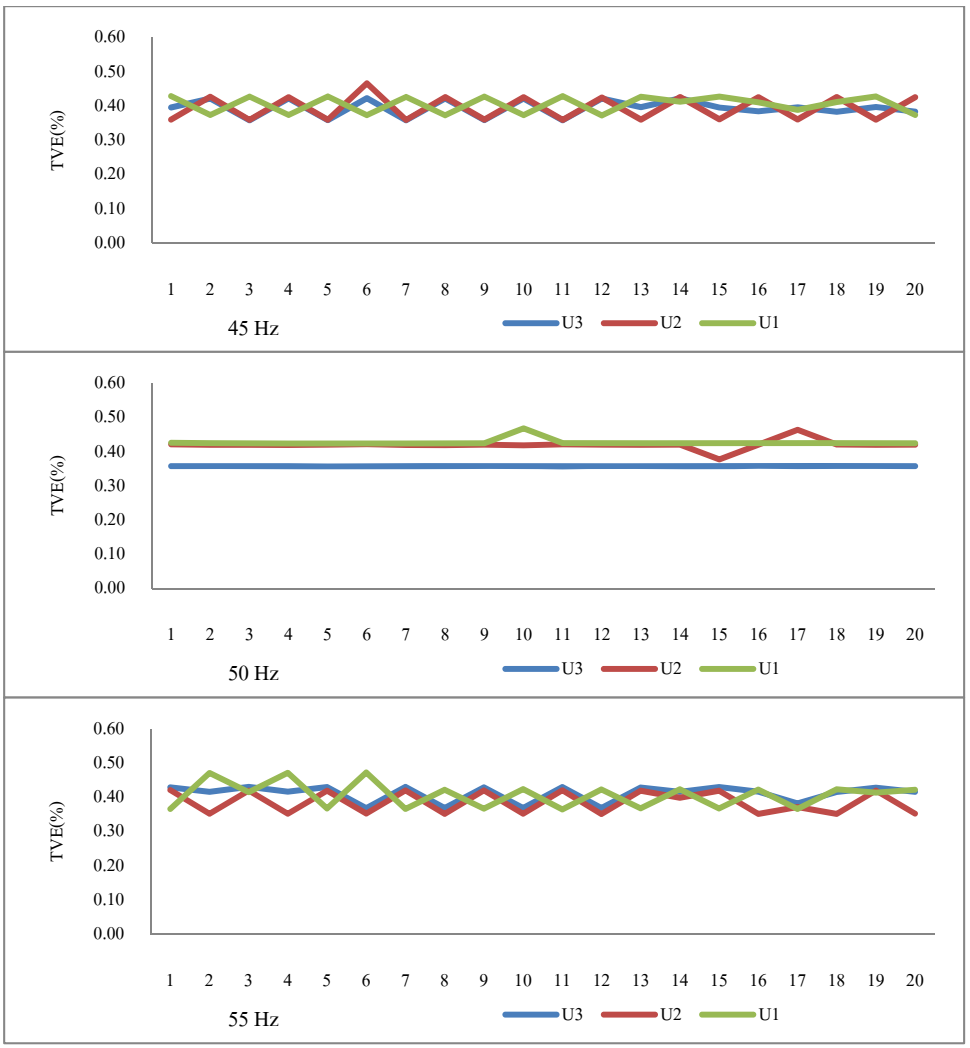

Figure 5-16: Sample of Three-Phase 176 V_{RMS} TVE Result.

Maximum percentage TVEs of three-phase 176 V_{RMS} experiment at 45 Hz are 0.5665 for U3, 0.5680 for U2, and 0.5675 for U1. With the same order, at 50 Hz are 0.5184, 0.5675, and 0.5717. And at 55 Hz are 0.5857, 0.5718, and 0.5725.

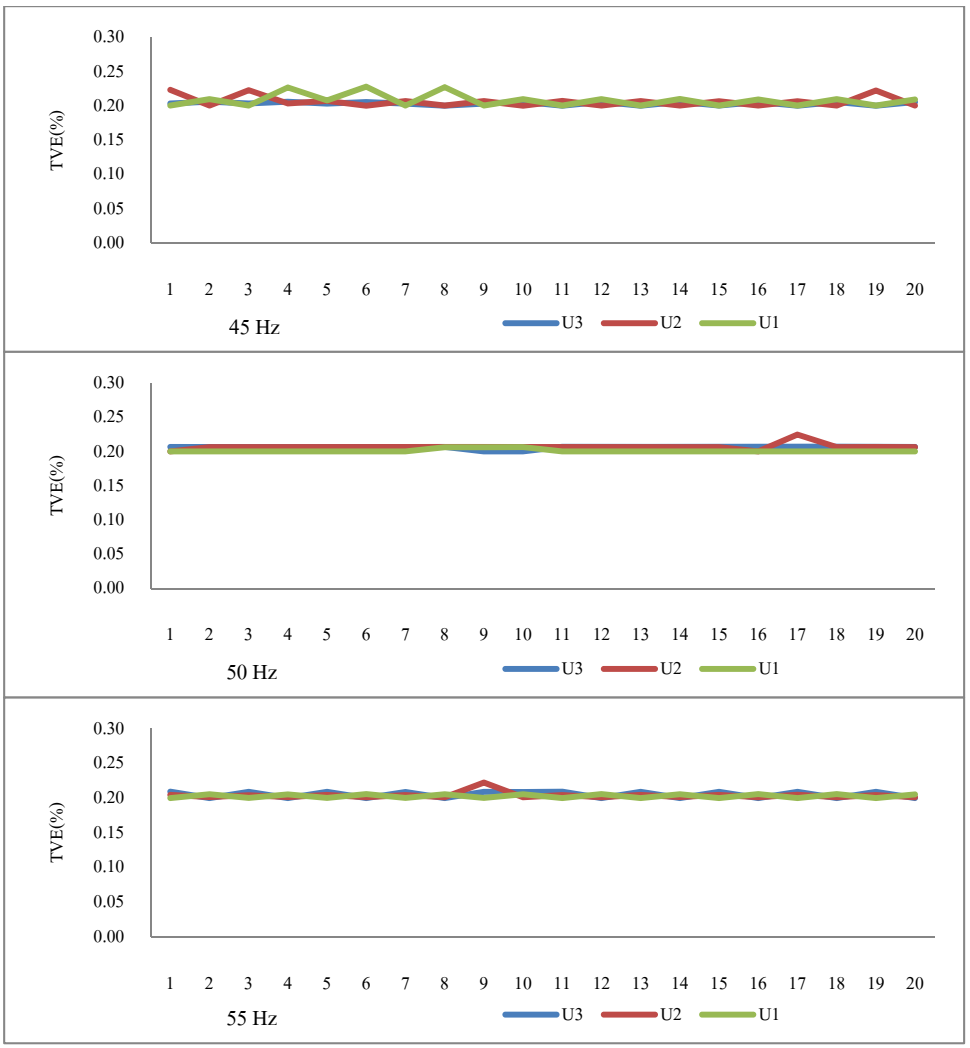

Figure 5-17: Sample of Three-Phase 220 V_{RMS} TVE Result.

Maximum percentage TVEs of three-phase 220 V_{RMS} experiment at 45 Hz are 0.3937 for U3, 0.3939 for U2, and 0.3959 for U1. With the same order, at 50 Hz are 0.3928, 0.3948, and 0.3854. And at 55 Hz are 0.3965, 0.3948, and 0.3962.

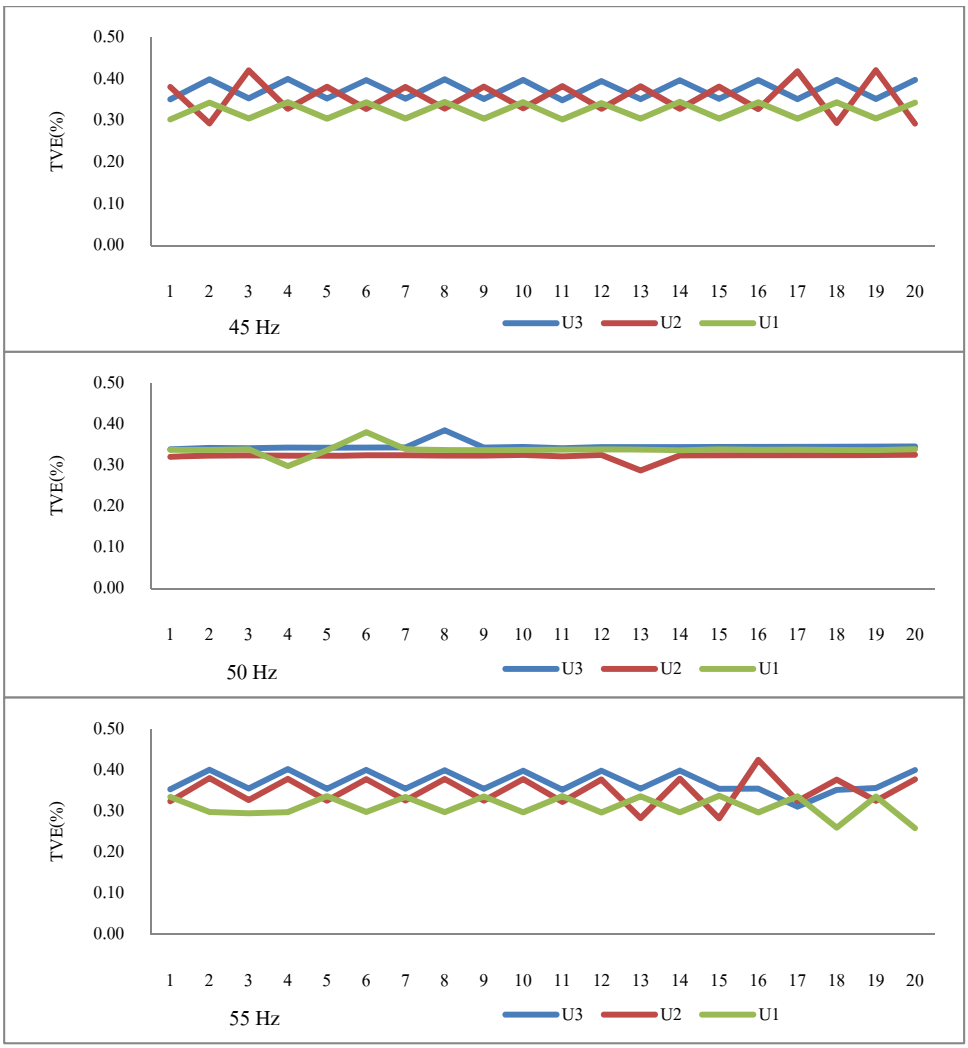

Figure 5-18: Sample of Three-Phase 264 V_{RMS} TVE Result.

Maximum percentage TVEs of three-phase 264 V_{RMS} experiment at 45 Hz are 0.5186 for U3, 0.5338 for U2, and 0.4746 for U1. With the same order, at 50 Hz are 0.5135, 0.4891, and 0.5005. And at 55 Hz are 0.5212, 0.5392, and 0.5031.

Figure 5-19, 5-20, 5-21, and 5-22 show a sample of TVE results on single-phase signal.

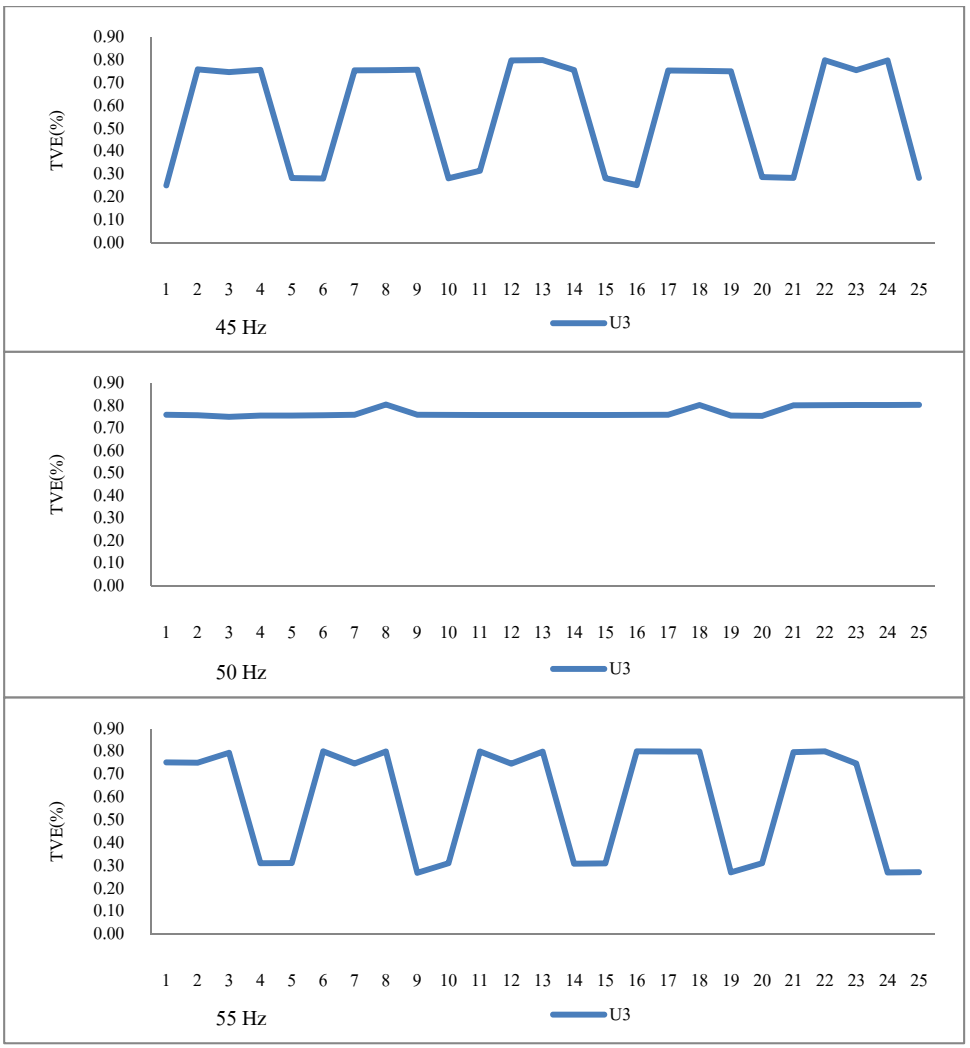

Figure 5-19: Sample of Single-Phase 22 V_{RMS} TVE Result.

Maximum percentage TVEs of single-phase 22 V_{RMS} experiment are 0.8666 for 45 Hz, 0.8732 for 50 Hz, and 0.9103 for 55 Hz.

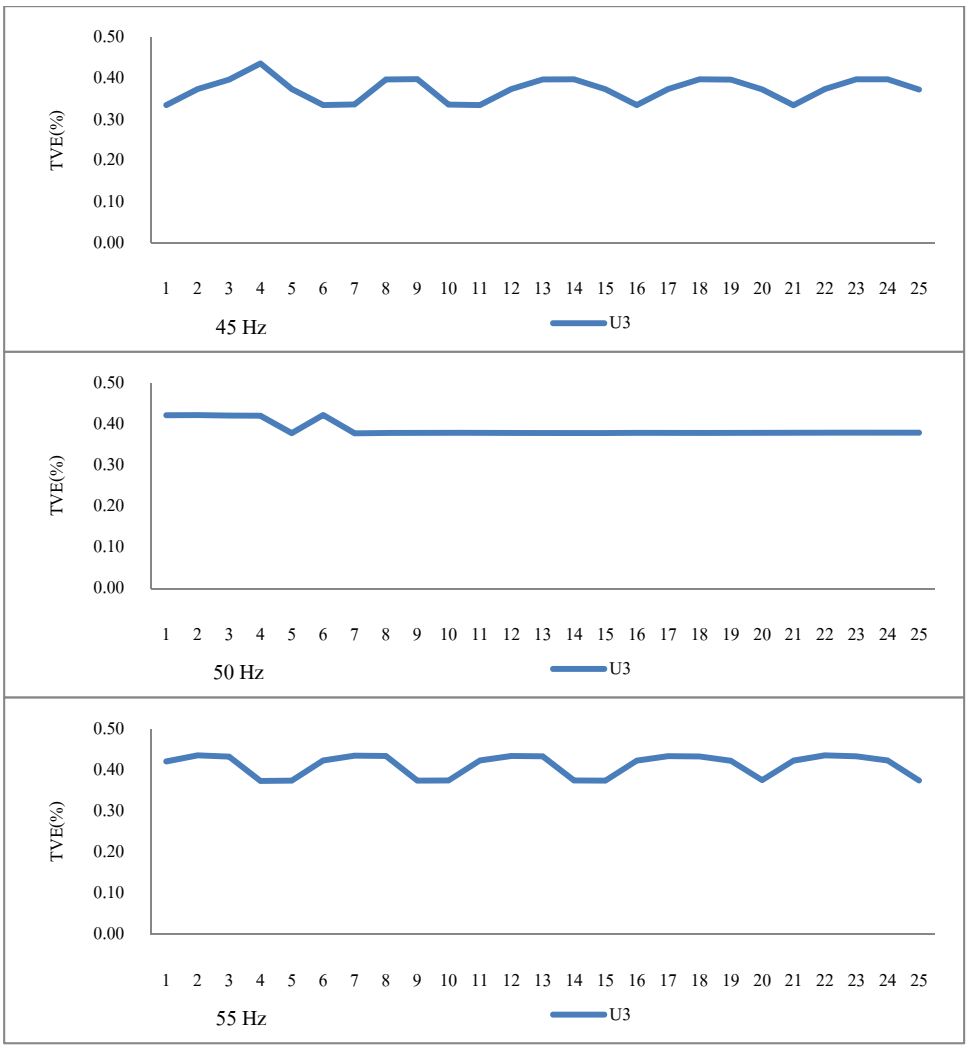

Figure 5-20: Sample of Single-Phase 176 V_{RMS} TVE Result.

Maximum percentage TVEs of single-phase 176 V_{RMS} experiment are 0.5440 for 45 Hz, 0.5669 for 50 Hz, and 0.5820 for 55 Hz.

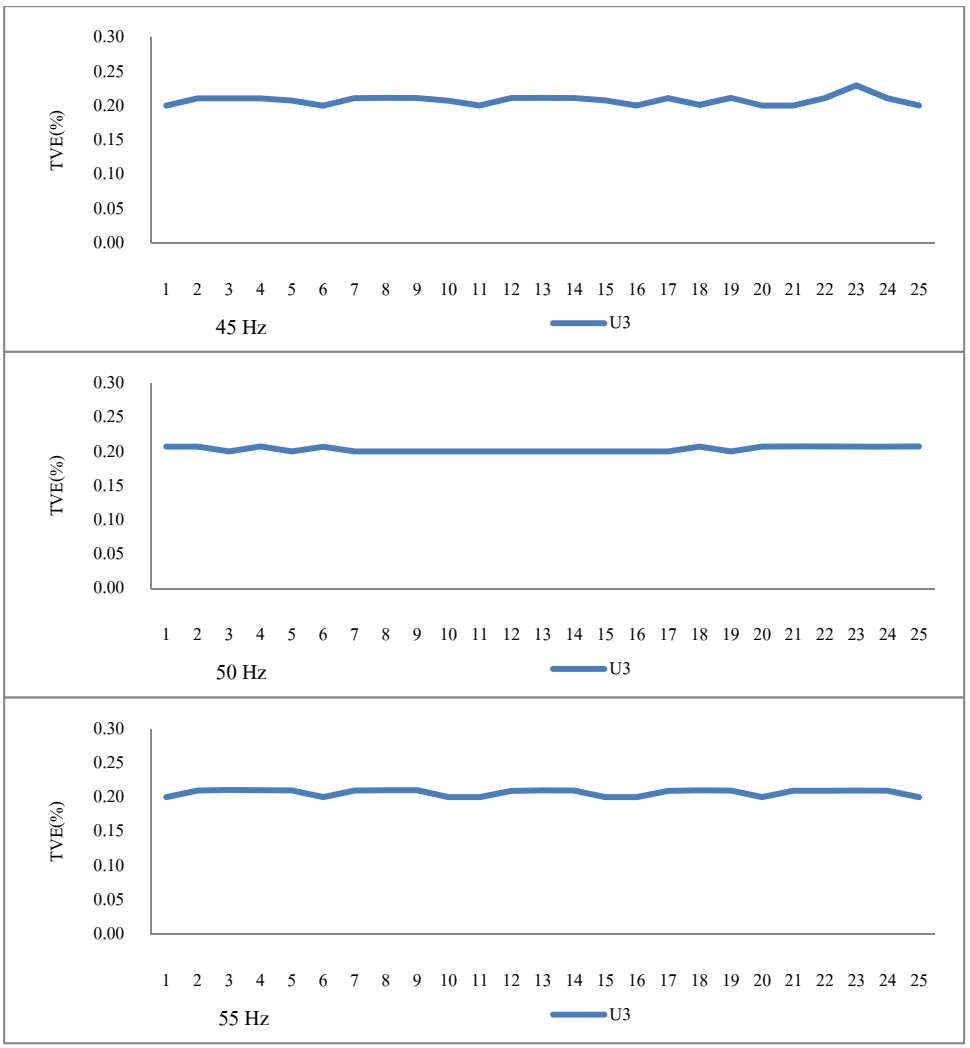

Figure 5-21: Sample of Single-Phase 220 V_{RMS} TVE Result.

Maximum percentage TVEs of single-phase 220 V_{RMS} experiment are 0.3974 for 45 Hz, 0.3942 for 50 Hz, and 0.3983 for 55 Hz.

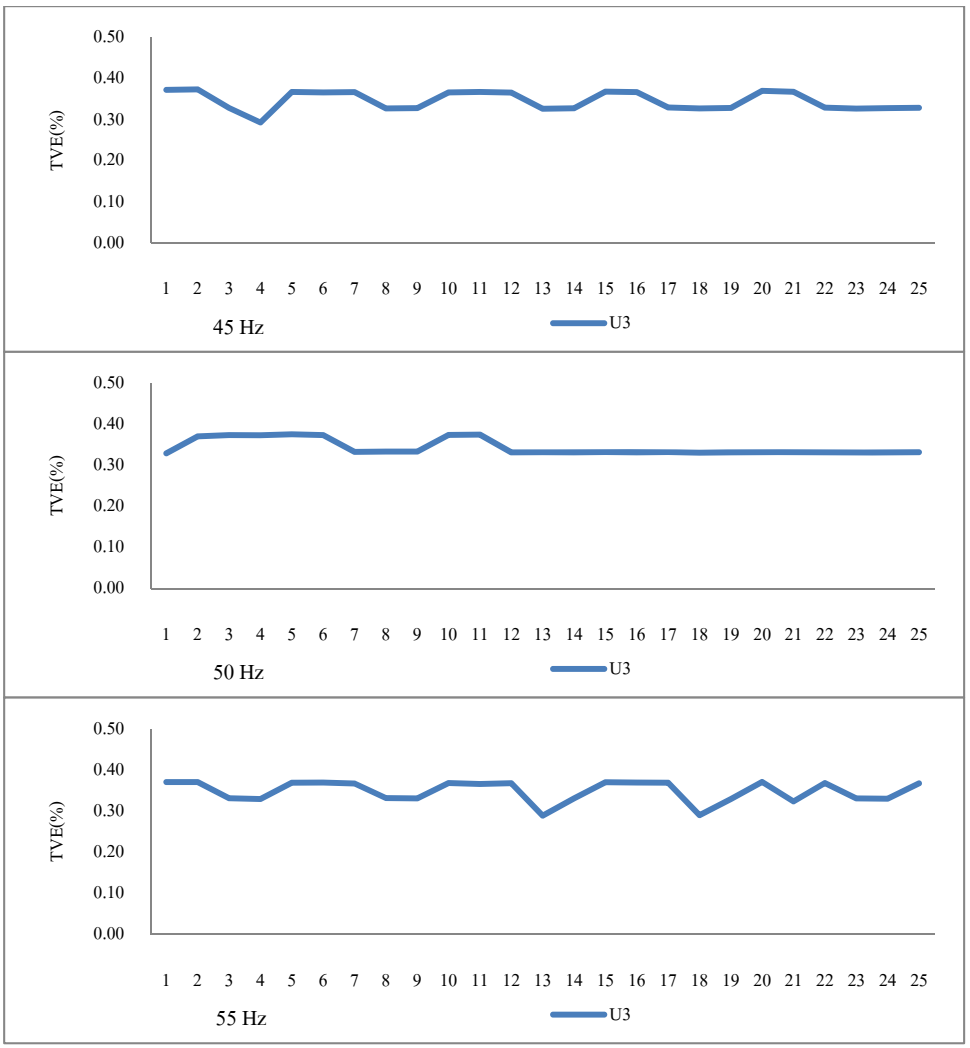

Figure 5-22: Sample of Single-Phase 264 V_{RMS} TVE Result.

Maximum percentage TVEs of single-phase 264 V_{RMS} experiment are 0.5245 for 45 Hz, 0.5037 for 50 Hz, and 0.4980 for 55 Hz.

CHAPTER VI

CONCLUSION AND RECOMMENDATION

The prototype of PMU in this research has ARM Cortex M3 as the MCU with maximum frequency clock of 32 MHz to manipulate the system inside the prototype. It receives sample of input signal from 16-bit ADC and date data from GPS receiver to export time-stamp phasor to computer by USART communication. Sampling process of ADC is controlled by a timer inside MCU which synchronized to GPS time pulse signal for phasor accuracy enhancing and common time reference.

The PRS 1.3 reference standard has no input for GPS time pulse to use the common time reference, thus the experiment is split to magnitude experiment and phase experiment. The phase experiment used another MCU to create a GPS synchronized 50 Hz source to estimate phase angle estimation error of the prototype. Since the TVE of 2 vectors is the same at any angle if the difference of magnitude and the difference of angle are the same, the maximum phase angle estimation error in phase experiment can be combined with magnitude from magnitude experiment to estimate TVE.

The results may show that TVEs are lower than 1 % but the prototype was designed with general commercial components; the accuracy can be improved with higher grade of the components, especially the crystal that oscillates for clock of the system.

The MCU is a STM32L which stands on the range of low power device and runs only 32 MHz of maximum clock frequency. Because of that reasons, sampling algorithm is forced to be half-wave sampling on both reporting rates. Enhances prototype with higher chip's family and clock frequency that can enable full-wave algorithm, and the accuracy shall be improved. Moreover, if more than one PMU are placed in SCADA system, communication needs to be applied.

As the specification of the communication in IEEE C37.118, a lot of communication process needs to be done and STM32L alone can not make it.

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BIOGRAPHY

Mr. Panut Tavilsup was born on September 27, 1988 in Nakhonratchasima province, Thailand. He began his master's degree in electrical engineering and accounted as a member of Embedded System and IC Design (ESID) research laboratory at Chulalongkorn University on 2010. His paper name "Development of Phasor Measurement Unit Conformed to IEEE C37.118 Standard for 50 Hz Power System" was published on December, 2012 in 2012 IEEE International Conference on Electron Devices and Solid State Circuit (EDSSC). His research interests are embedded system design and its application.