Chapter 4

Hardware's Design

To accomplish the objective of this thesis, hardwares and programs will be developed. First, "IBM 3270 Coaxial Type A Interface Board" will be developed to enable the capturing of data trasmitting in the coaxial cable.

Second, "IBM 3270 Coaxial/RS-232C Adapter Board" will be developed to convert data transmitted in coaxial cable to RS-232C, and vice-versa. The details of both hardwares are described in this chapter.

Programs are developed for IBM 3270 Coaxial/RS-232C Adapter Board and personal computer to enable the testing of both hardwares developed. The details of the programs developed are described in chapter 5.

4.1 IBM 3270 Coaxial Type A Interface Board (3270CIB)

The IBM 3270 Coaxial Type A Interface Board is developed to allow capturing of data transmitting in the coaxial cable between the IBM 3274 control unit and IBM 3278. It also allows the personal computer to interface to the coaxial cable for both transmit and receive purposes.

The hardware is developed using the DP8340 Serial Bi-Phase Transmitter/Encoder and DP8341 Serial Bi-Phase Receiver/Decoder for interfacing to the coaxial cable (Appendix K). It is implemented on a 8 bit IBM personal computer bus prototype board. The transmitter and receiver are controlled directly by the personal computer. Figure 4.1 illustrates design's block diagram, and figure 4.2 illustrates photographs of the harware developed.

4.1.1 Hardware's Design

The interface board is developed on the 8 bit IBM personal computer bus prototype board, because of its popularity. Also it is found that there is only a small difference in using the 8 bit and 16 bit bus of the personal computer, ie. after testing with 16 bit bus, it is found that data is still losted when capturing with data bit 10 and data bit 11 during data transfer in multi byte mode.

Personal computer is used because it allows data captured to be saved, printed or displayed.

As illustrates in figure 4.1, three buffers are used to allow the personal computer to access (read/write) the DP8340, and DP8341 for its data and status. Also one decoder is used to decode the personal computer bus read logic, and another decoder is used to decode the bus write logic. The control pins of both

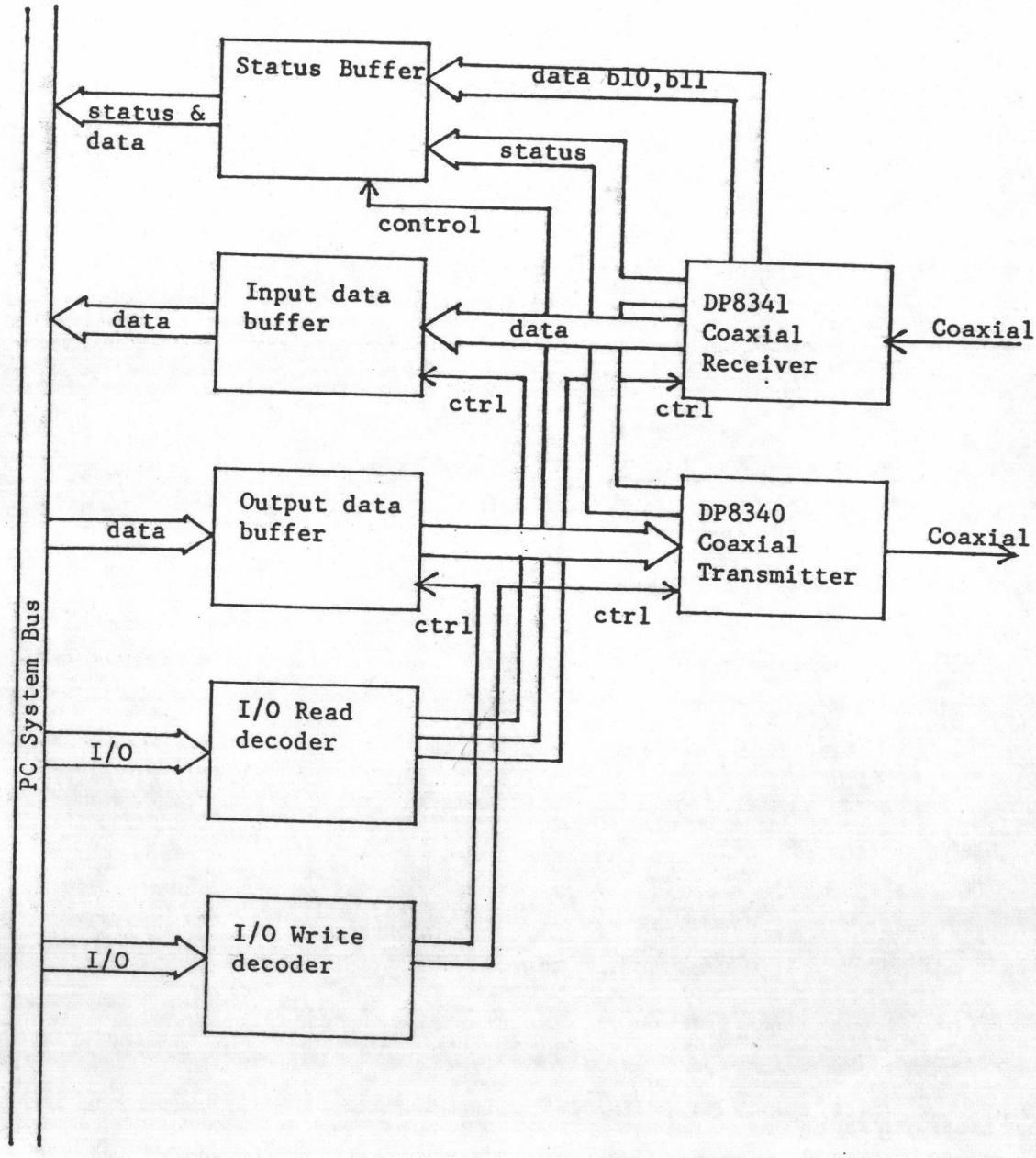


Figure 4.1 IBM 3270 Coaxial Interface Boards's Block Diagram.

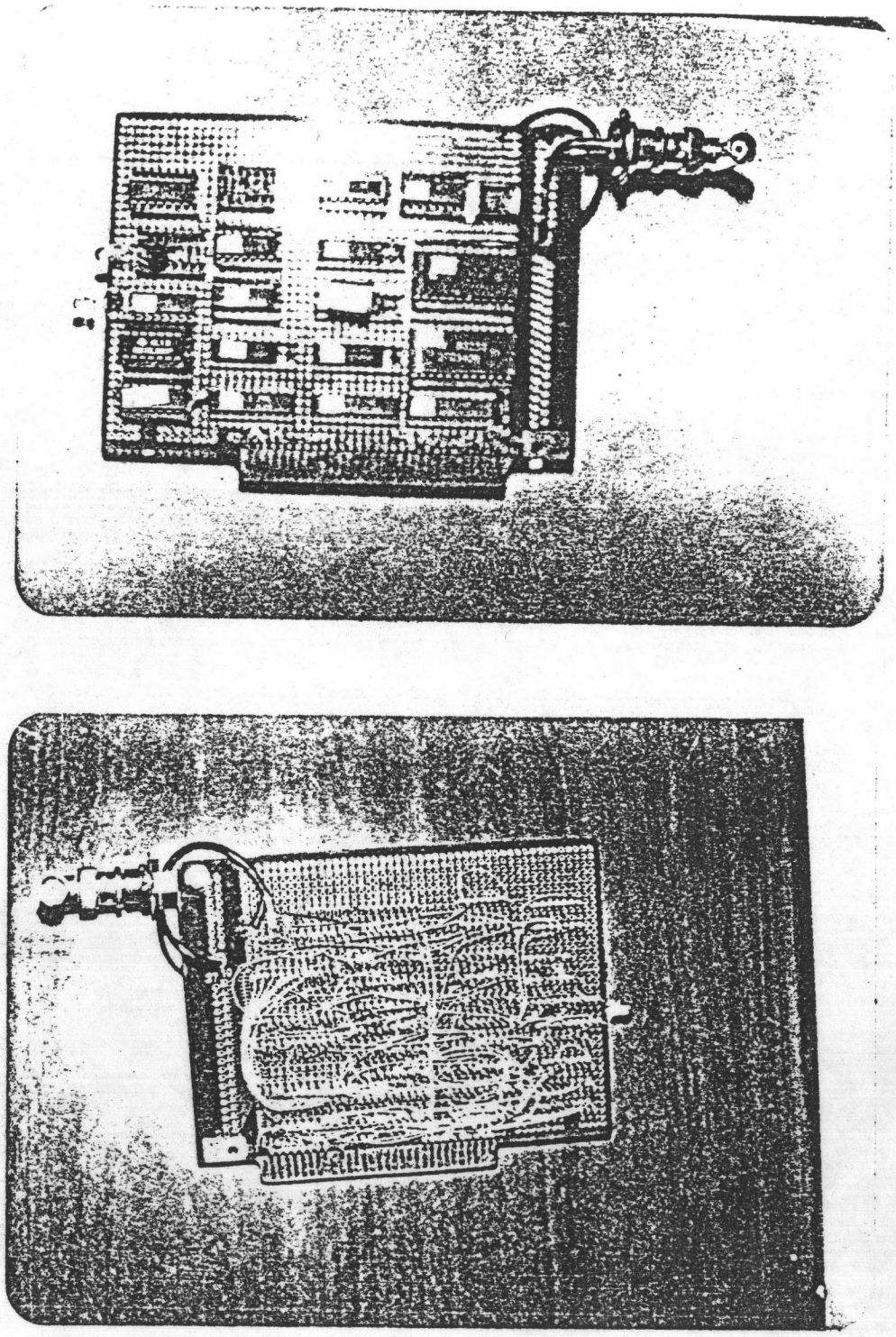


Figure 4.2 Photographs of 3270CIB.

transmitter and receiver are controlled by these two decoders. Appendix L illustrates the complete circuit diagram. Appendix M illustrates the early circuit diagram which is found to have problem in capturing the data bit10 and data bit 11, because it has only one bi-directional buffer for data and status.

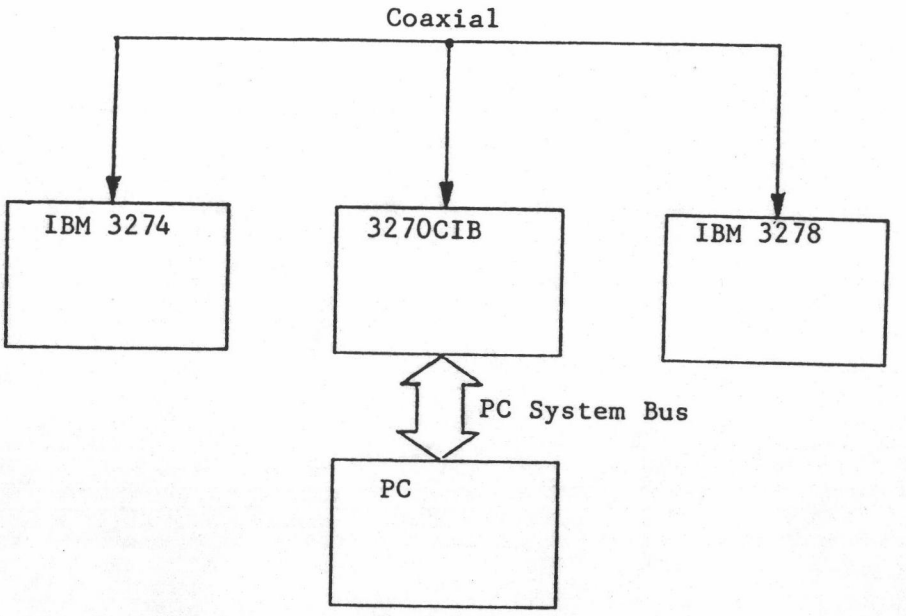
4.1.2 Hardware's Testing

The testing is done in three steps as follows:

1. The 3270CIB is used to capture data transmitted between IBM 3274 and IBM 3278. A sample of data captured is illustrated in Appendix E, and Appendix F. The program used in the testing is shown in Appendix N, and Appendix O. Figure 4.3 illustrates the test configuration and its photograph.

2. The 3270CIB is used to interface to IBM 3278 and emulating itself as IBM 3274. The program used in the testing is illustrated in Appendix P. Figure 4.4 illustrates the test configuration and its photograph.

3. The 3270CIB is used to interface to IBM 3274 and emulating itself as IBM 3278. The program used in the testing is illustrated in Appendix Q. Figure 4.5 illustrates the test configuration and its photograph.



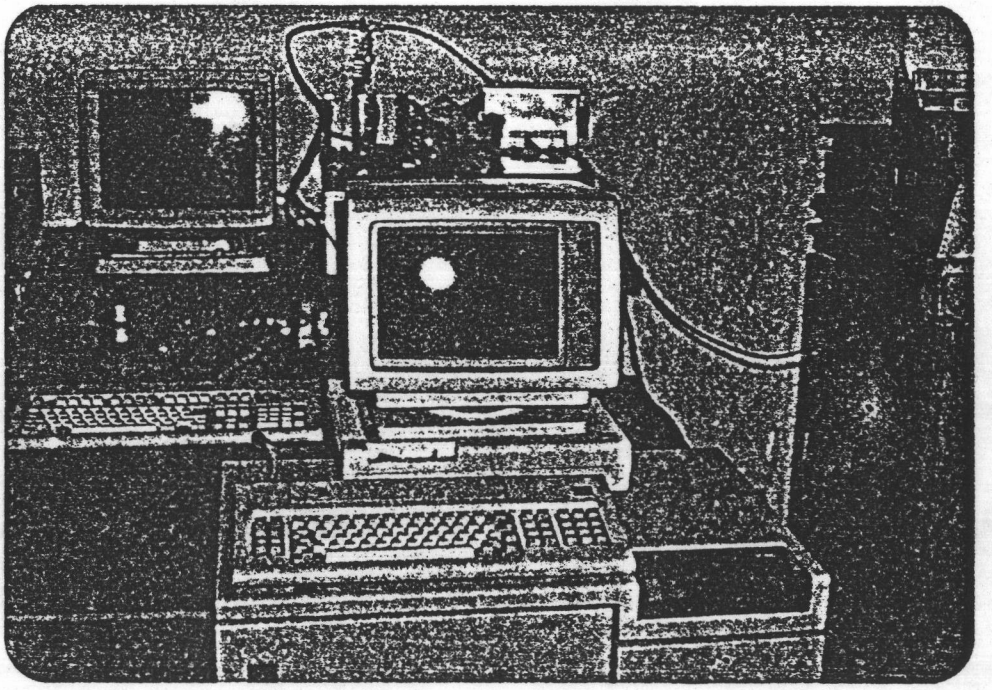
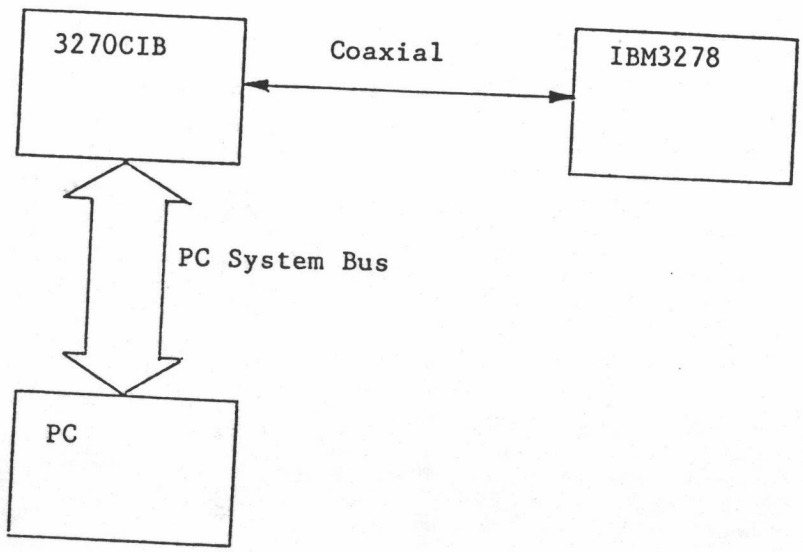


Figure 4.3 Test configuration of 3270CIB for capturing data between IBM 3274 and IBM 3278.



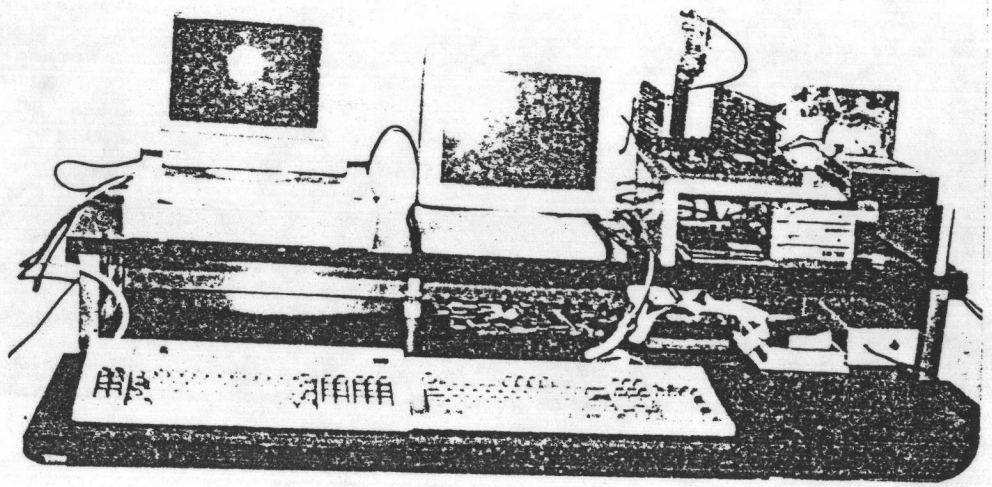
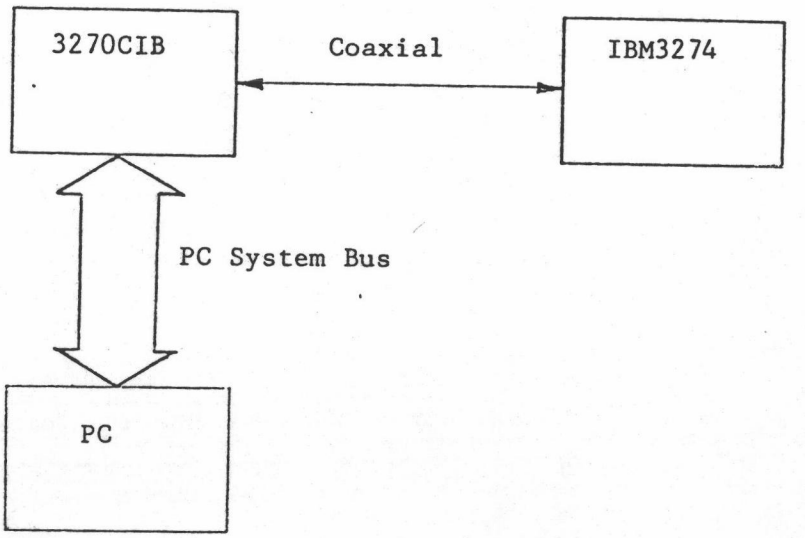


Figure 4.4 Test configuration of 3270CIB for communication between PC and IBM 3278.



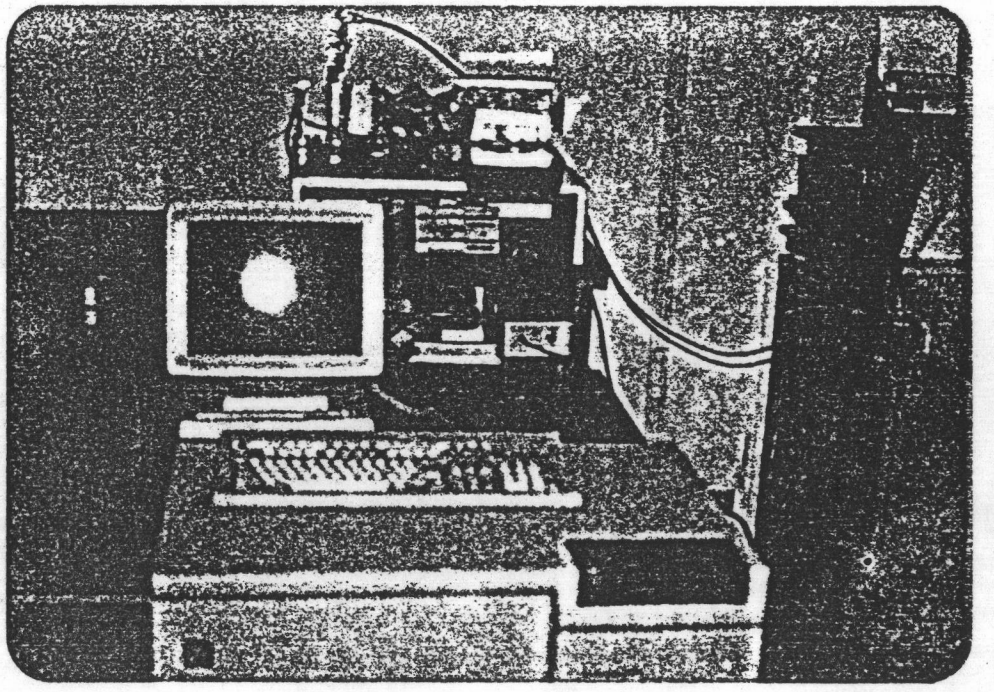


Figure 4.5 Test configuration of 3270CIB for communication between PC and IBM 3274.

After testing in step 1, it is found that the data protocol transmitted in the coaxial cable is conformed to the standard described in chapter 3. Also it is found that the CPU speed of the personal computer(80286 CPU at 10MHz) is not suitable in capturing the data in the coaxial cable, this is due to the high speed transmission during data block transfer in multi byte mode. It is found that the personal computer used can capture data in the coaxial cable, if the data bit 10 and 11 are ignored, and data is losted if data bit 10 and 11 are also captured. Appendix E illustrates data captured without data bit 10 and 11, and Appendix F illustrates data captured with data bit 10 and 11 under the same condition as data illustrated in Appendix E. This problem can be solved if higher speed personal computer with fast I/O is used, but at the time of testing, this personal computer was not readily available.

As the result of testing in step one, the scan code, buffer code (Appendix A), and buffer addressing format (Appendix C) used by the IBM 3274 and IBM 3278 is found. Appendix B illustrates the buffer code used with IBM Thai Language EBCDIC table B.

The testing in step two, helps to verify that the harware developed can be used for data transmission with the coaxial cable, if the multi byte mode is not used. It also helps in verifying the

commands illustrated in Appendix D.

The testing in step three, confirms that interfacing to IBM 3274 required a high speed and specialized CPU, ie. the 8X305 microcontroller or the CHIPSLink 82C570 Single Chip "3270" Protocol Controller(Appendix K). In order to communicate in multi byte mode, the CPU must read data from I/O port at the speed of 196.558 KHz (2.3587 MHz / 12 = 196.557 KHz).

As the results of the above testing, the following conclusion is drawn on the Interfacing concept between IBM 3278 and IBM 3274. IBM 3278 is constantly polled by the IBM 3274, this enable IBM 3274 the ability to determine whether IBM 3278 has been turned off or disconnected (IBM 3278 is disconnected if response to the poll command is not received). Also any key pressed on the IBM 3278 is transmitted to the IBM 3274 as scan code (scan code can only be transmitted in response to the poll command), also the character displayed on the IBM 3278 is transmitted to it by the IBM 3274 as buffer code. The list of commands used by IBM 3274 to communicate with IBM 3278 are illustrated in Appendix D.

4.2 IBM 3270 Coaxial/RS-232 Adapter Board (3270CAB)

The objective of this adapter is to convert signals on IBM 3270 coaxial cable to RS-232C signals and vice-versa.

Since transmission speed on the IBM 3270 coaxial cable is 2.3587 MHz, therefore the timing is critical. Also in some computer applications, such as interactive applications, the response time is important. Therefore, conversion's delay time should be minimized. In order to reduce the delay time, design using 2 microprocessors and 2 memory buffers are proposed for this adapter. Figure 4.6 illustrats the design's block diagram. Figure 4.7 illustrates the photographs of the hardware developed.

4.2.1 Hardware's Design

In the design, Z80A microprocessor is selected, because it is readily available and cheap. It is also a powerful 8 bits microprocessor, compared with other 8 bits microprocessors.

As illustrated in Figure 4.6, CPU A controls the coaxial interface section, and CPU B controls the RS-232C communication section. Two memory buffers is used to reduce receiving and transmitting delay time. Two Kbytes of RAM(Random Access Memory) is the most appropriate size for each memory buffer, because one full page of display screen contains only 1920 positions.

With 2 memory buffers, it is possible for both CPUs to process in parallel, i.e. while one is receiving data, another will be transmitting data. For example, after CPU A fills buffer A with the receiving

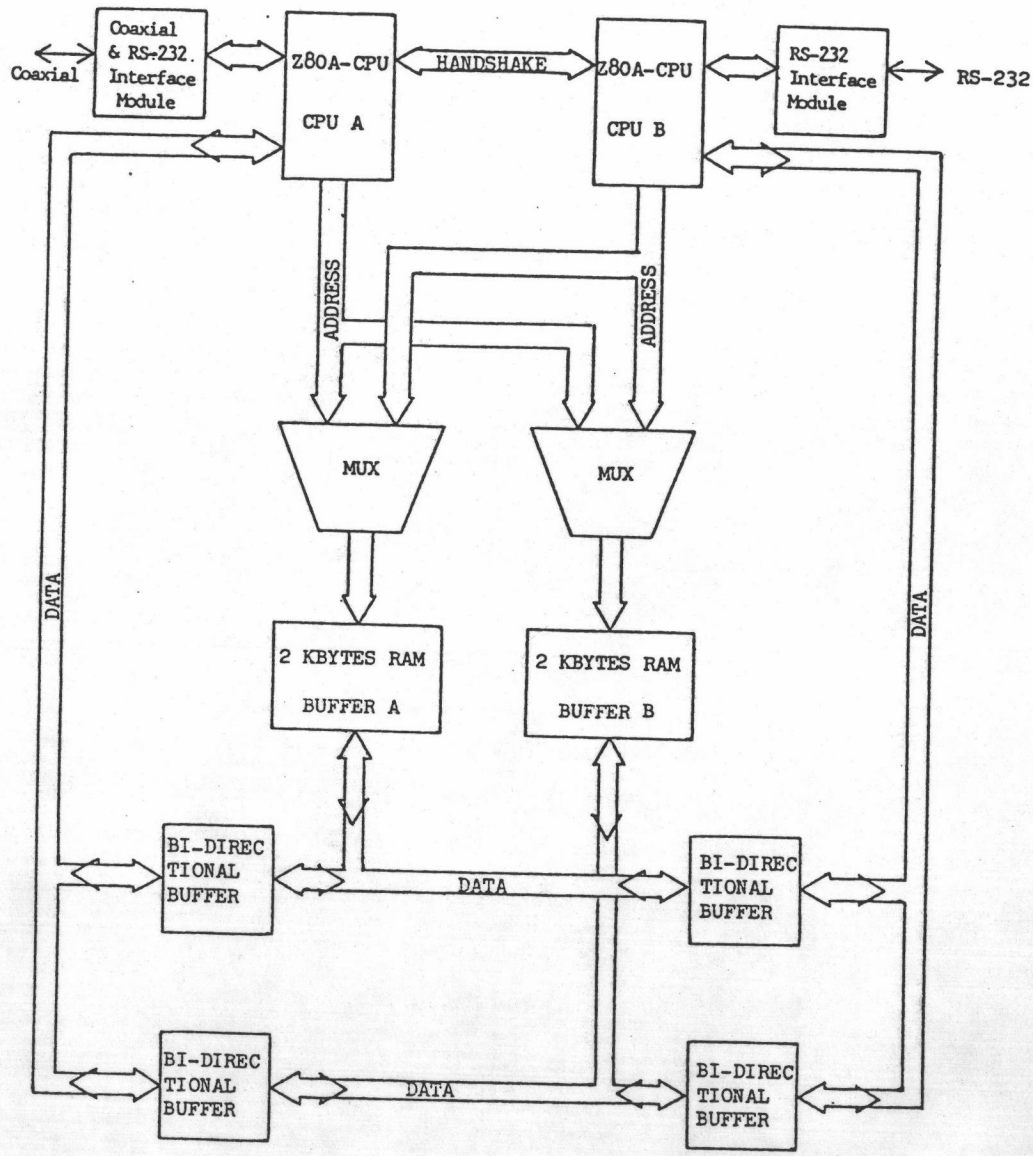


Figure 4.6 IBM 3270 Coaxial/RS-232C Adapter Board's Block Diagram.

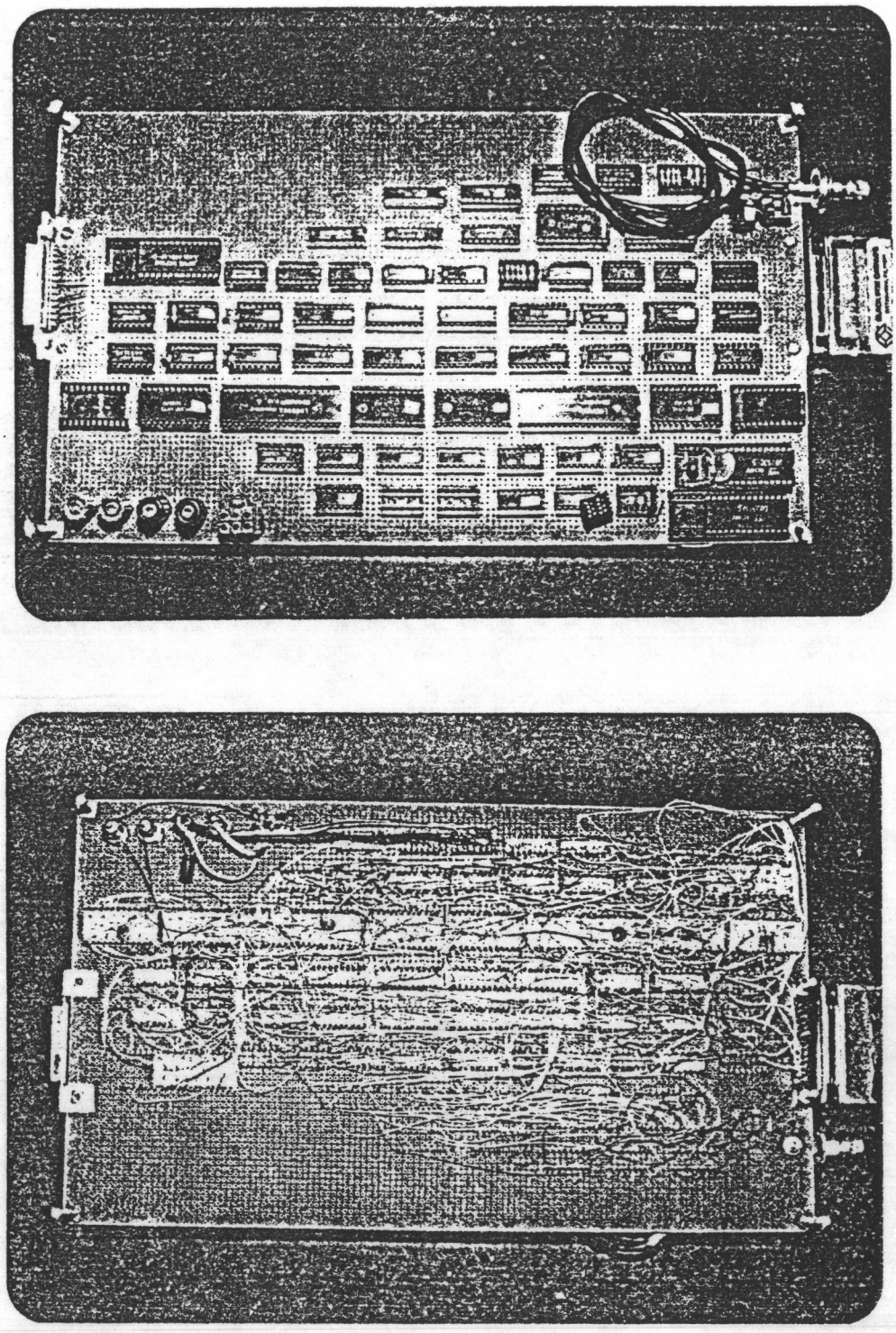


Figure 4.7 Photographs of 3270CAB.

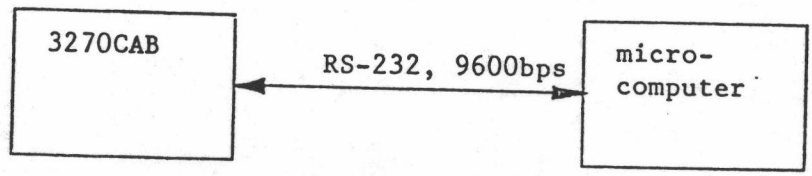
data, it signals CPU B that data is available for transmission. CPU B, then starts transmitting data from buffer A, while CPU A continues, and fills receiving data in buffer B. After buffer B is full, CPU A signals CPU B that data is available for transmission. If CPU B has not completed the transmission of data in buffer A, it signals CPU A to wait, otherwise CPU B will start to transmit data from buffer B, and allows CPU A to fills buffer A with the receiving data, and so on.

4.2.2 Hardware's Testing

The following steps are taken in testing the 3270CAB.

1. CPU B is developed and tested until it can communicate with a microcomputer through RS-232C interface. A program is written for CPU B to receive data and echo it back through RS-232C interface. XTALK program is used on the microcomputer to test this section. The communication speed was 9600 bps. Figure 4.8 illustrates the test configuration and its photograph.

2. CPU A is added a RS-232C interface, similar to CPU B. The RS-232C interface module is added to CPU A for testing the communication between CPU A and CPU B. Two microcomputers are used in this test, the first microcomputer is connected to the RS-232C interface of CPU A, and the second microcomputer is connected to the RS-232C interface of CPU B. Program is



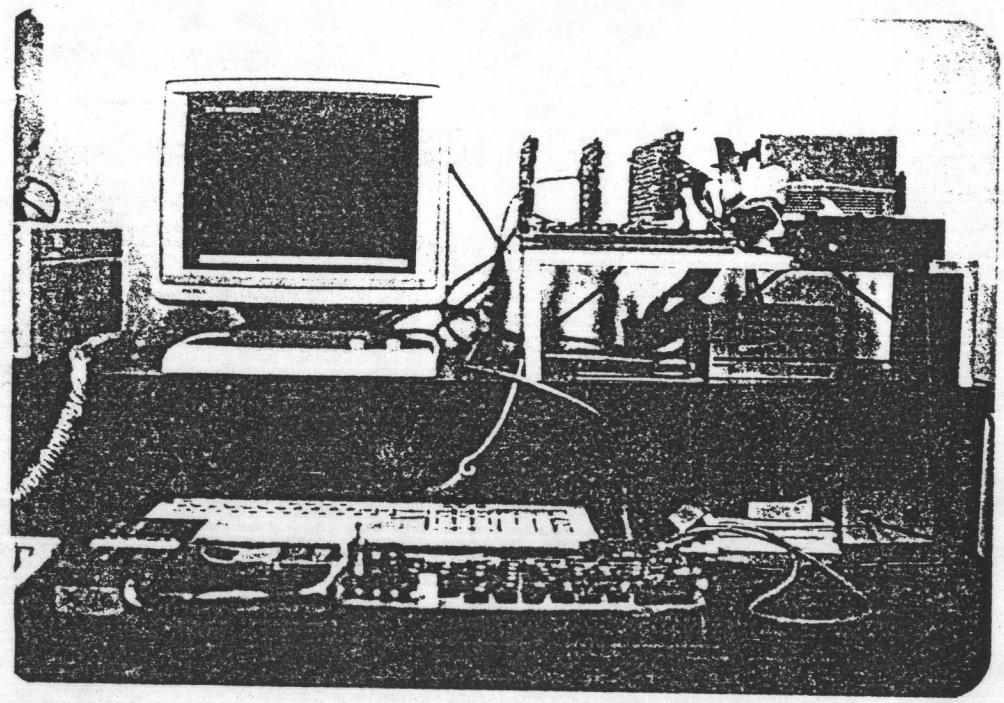
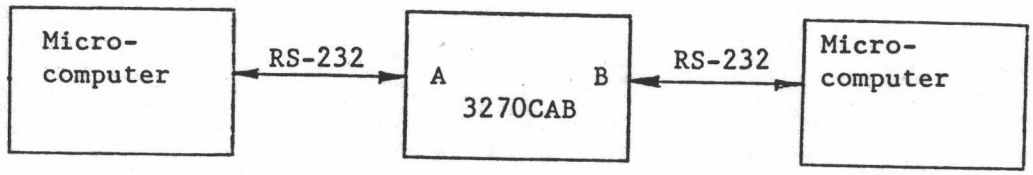


Figure 4.8 Test configuration of 3270CAB communicates with microcomputer.

written for both CPU A and CPU B, CPU A will receive data from RS-232C interface and put it in buffer, upon receiving of return code (0DH), it signals CPU B to send the data received by CPU A, to another microcomputer, and vice-versa. The communication speed was 9600bps. Figure 4.9 illustrates the test configuration and its photograph.

3. CPU A is added a coaxial interface, similar to the 3270CIB. A program is written to allow a microcomputer to communicate with the IBM 3278 using 3270CAB. ASCII character transmitted from the microcomputer is displayed on the IBM 3278, and character of key pressed on the IBM 3278 is displayed on the IBM 3278 and transmitted to microcomputer. Figure 4.10 illustrates the test configuration and its photograph.

As a result of the above testing, the following conclusion is drawn on the 3270CAB. It is possible to use the hardware developed to communicate with IBM 3278, but without the multi byte data transfer mode. Also with reference to the finding in 4.1, the concept of having two CPU and two memory buffers is not practical. Because high speed CPU is required for the data transfer in multi byte mode, but it will have processing time left during the single byte mode, which can be used to process the communication with microcomputer.



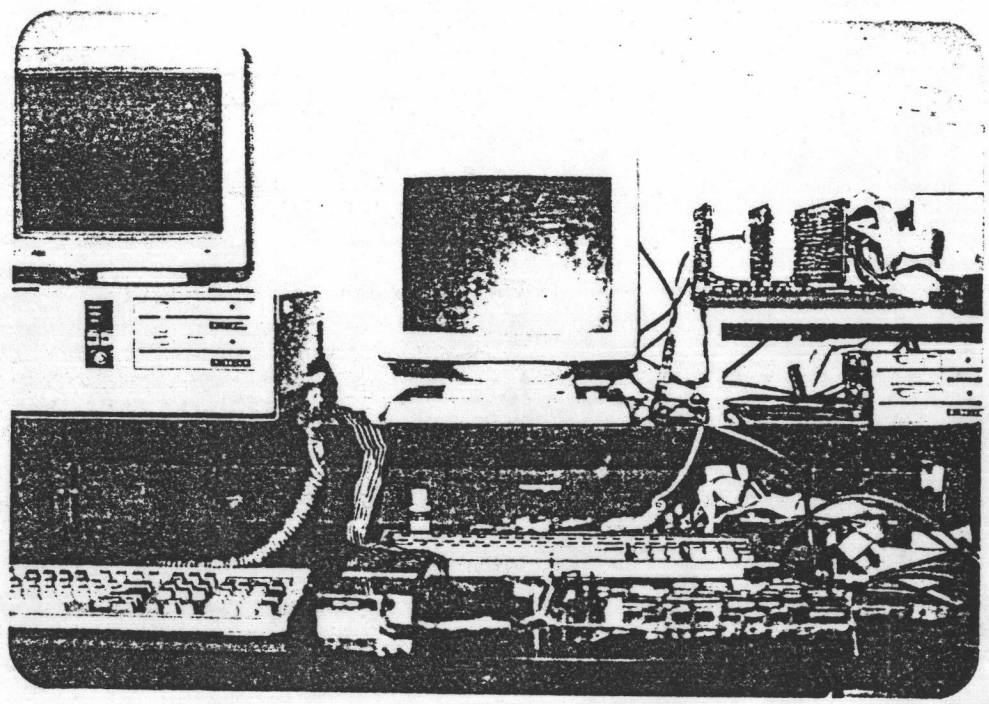
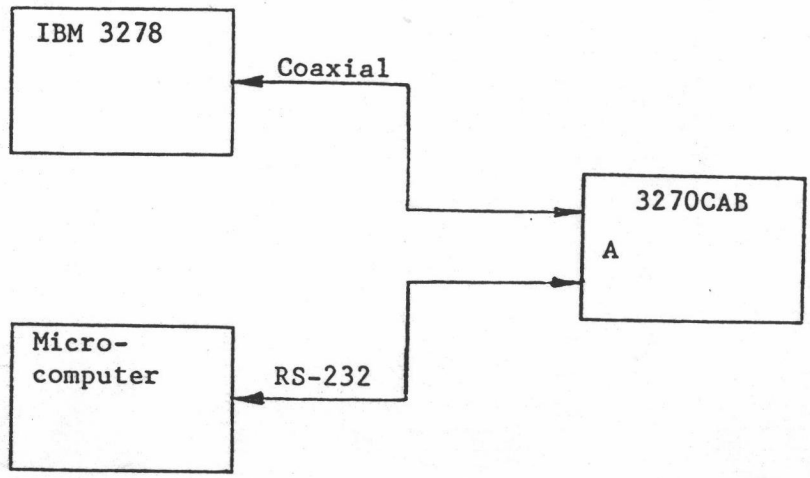


Figure 4.9 Test configuration of 3270CAB for communication between 2 microcomputer.



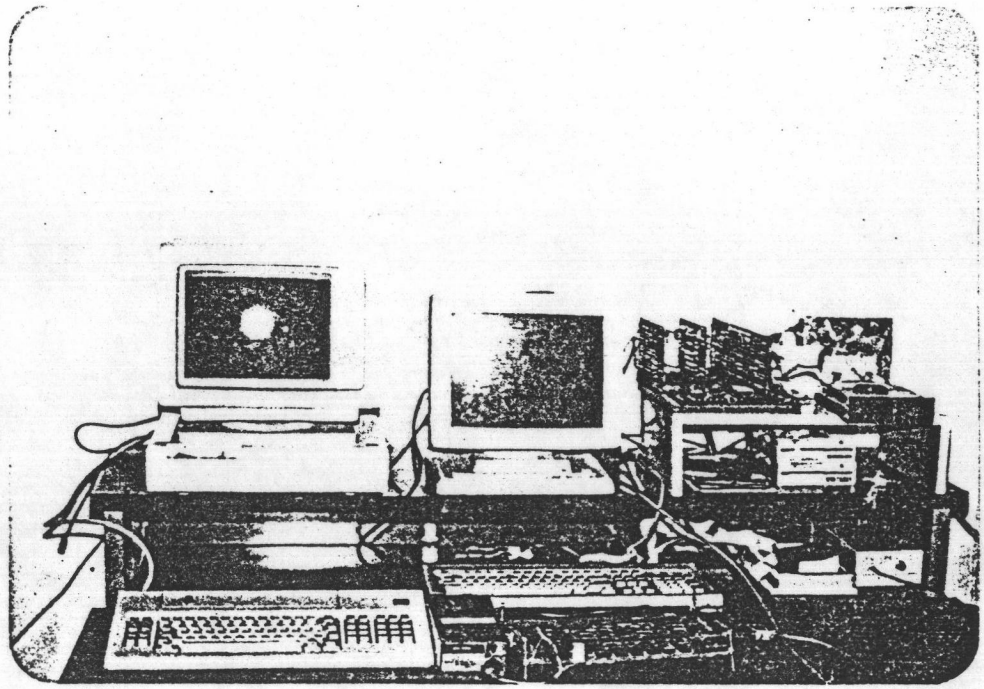


Figure 4.10 Test configuration of 3270CAB for communication between microcomputer and IBM 3278.