CHAPTER 4
Methodology

4.1 Introduction

Improving effectiveness in detecting tester problems provides better control in tester performance. Therefore, the test operation can be done more efficiently. In order to achieve the improved process which provides higher effectiveness other than the current process that known reading HGAs are being used to run across group of testers to monitor tester performance, six sigma breakthrough is used as guidelines in developing this proposed process.

Measurement phase, which is the first phase of six sigma, is useful in identifying the problems and their causes so that the ways to eliminate them could be achieved. In analysis phase, the current system is analysed to bring about the idea that would be benefits in improving the existing process. In improvement phase, the key variables affecting to effectiveness are used to develop the new system used for monitoring tester performance. Finally, control phase concerns about how to maintain the improved system to meet the expected benefits.

4.2 Measurement Phase

Since the quality of HGAs is measured by customer satisfaction, HGAs produced should be operated efficiently. Defect HGAs that are shipped to the customers should be eliminated. Hence, the method in examining the quality of HGAs before shipping the products to the customers has to be effectively worked. It means that testers used to test the ability of the HGAs must be reliable.

To ensure that those testers can work as intended, only calibration by period is not enough. Since variation from calibration could be occurred, testers should be controlled and monitored their performance during their uses. Errors or abnormal conditions from the testing system should be detected and eliminated. The process to control tester

performance that company currently uses is called TSPC. This method has been already elaborately explained in the previous chapter.

From current TSPC method, it is found that TSPC is not effective enough because when SPC out of control is taken place, unnecessary tester downtime has been spent to take the corrective actions that the causes are not from the testing system; factoring part, disc, and tester issues. Most of them are from procedure in performing TSPC. Low effectiveness in the current method is demonstrated. Effectiveness is the percent detection rate when SPC out of control is taken place that the root causes are from tester performance.

When the method used in detecting tester problems is not effective, it results in a lot of bad impacts to the company. The test result might be wrong. Good items might be rejected or reworked while bad items are shipped to the customers. As a result, the company wastes time, effort, and money. It also results in long-term effect from cost of goodwill in case of customer dissatisfaction.

Before the causes of ineffective TSPC will be defined, understanding on process flow of current TSPC is necessary. Figure 4.1 is the process map shown the process steps in performing TSPC. From this process flow, the potential causes have been easily identified, and those causes can be critically analysed.

Since effectiveness can be measured from out of control that the root cause is from testing system, the other root causes resulting in out of control should be identified. By analysing TSPC process flow and brainstorming method, all possible causes are collected and illustrated in cause and effect diagram as shown in Figure 4.2.

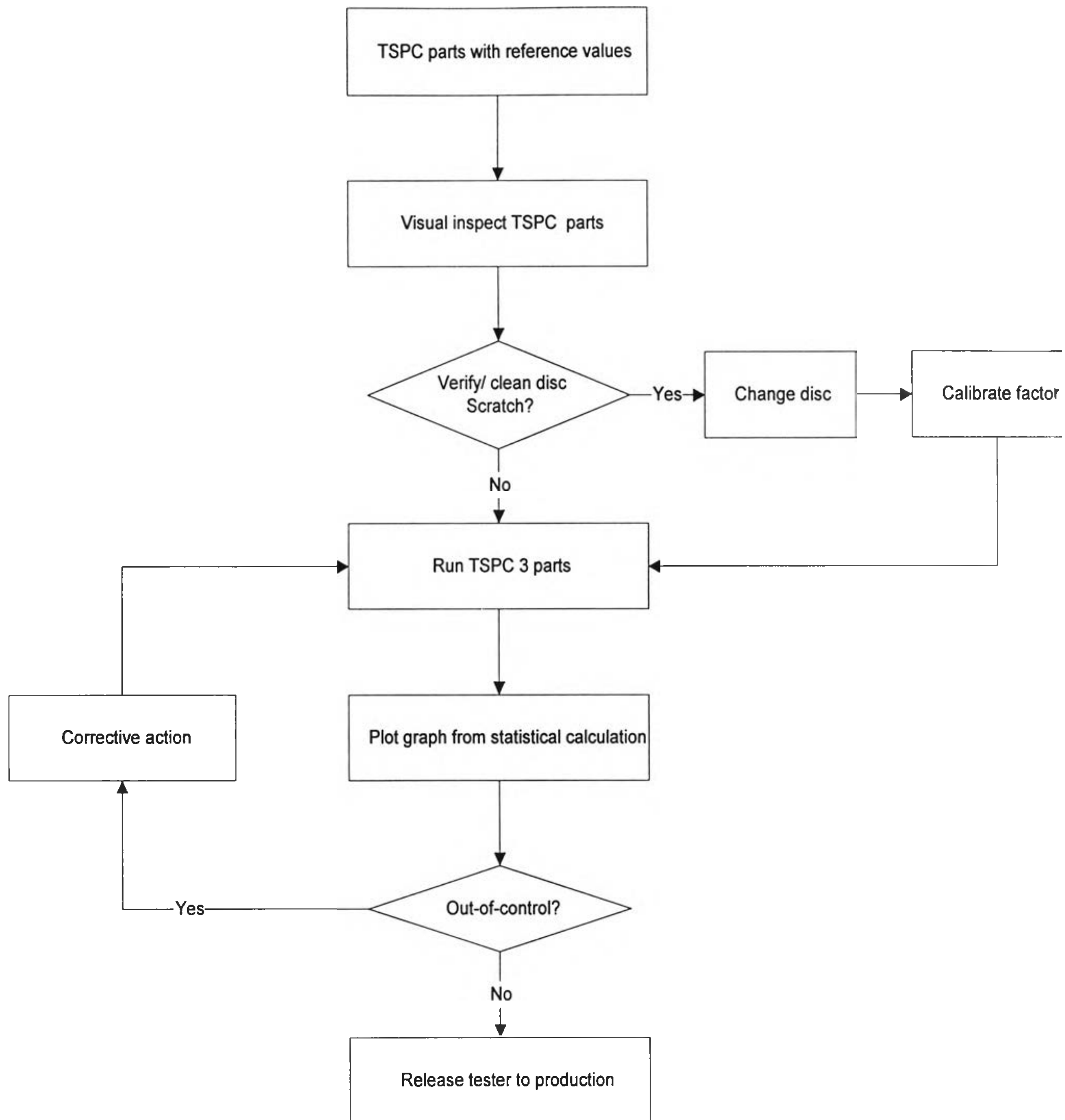


Figure 4.1: Process map of TSPC

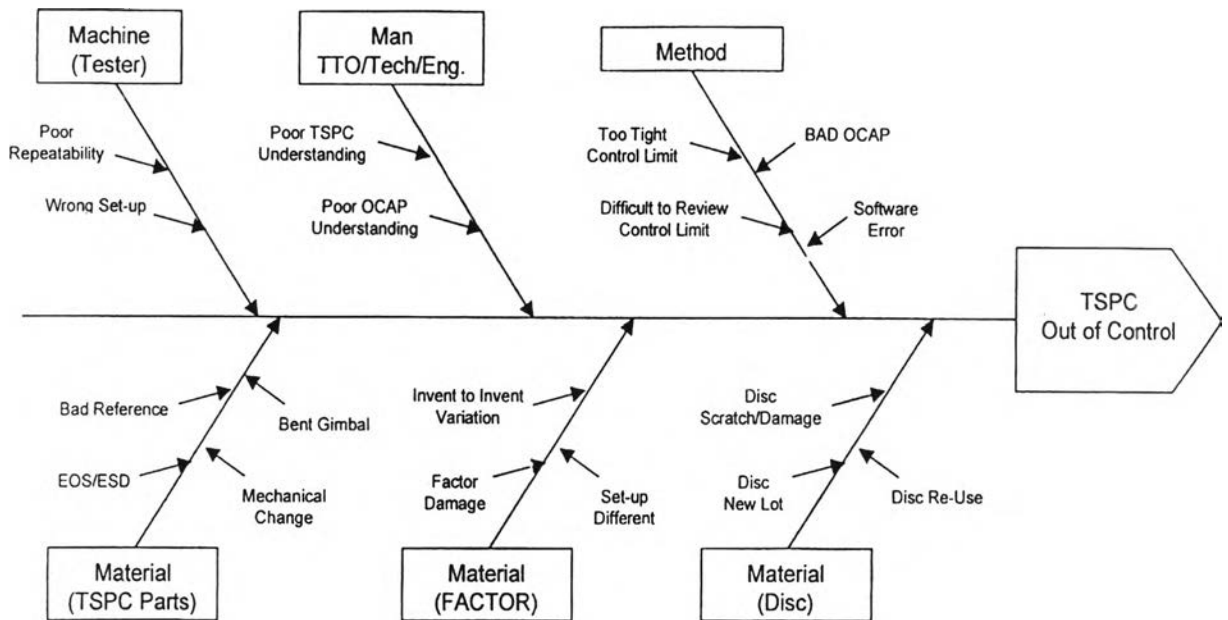


Figure 4.2: Cause and effect diagram of out of control root causes

There are six major causes of TSPC out of control, i.e., tester, operator, method used, TSPC part, factoring part, and disc. Out of control might be occurred from tester itself such as poor testers that have low repeatability or testers that are wrongly setup. It may be from poor understanding in TSPC or out of control corrective action plan implemented by TTO, technician, and engineer. It could be occurred from the method used such as lack of control limit review, too tight control limit, software error, or bad work instruction either in TSPC or out of control corrective action plan. Out of control can also be from TSPC parts. Those parts might have bad reference from secondary standard generation process, or they may be damaged before running on the tester; for example, they may damage from mechanical change when handled, from bent gimbal, or from Electro Static Discharge (ESD). The out of control root causes may also be the damaged factoring parts, variation from different lots of factor, or set-up difference. The other causes of out of control are from disc issues such as disc scratched or damaged, disc new lot, and disc re-used.

TSPC would be effective if causes are from tester, factoring part, and disc. The rest of the causes that are operator, method used, and TSPC part should not be occurred because those causes are come only when performing TSPC. However, those causes are

usually concerned when performing TSPC. Especially, cause from TSPC part is most contributed in TSPC out of control as shown in Table 4.1 and Pareto diagram in Figure 4.3.

Table 4.1: The causes of out of control events

Cause	Frequency	Relative Frequency	Cumulative Relative Frequency
Part	121	0.70	0.70
Factor	34	0.20	0.89
Disc	11	0.06	0.95
Tester	8	0.04	1.00
Total	**174**	**1.00**	

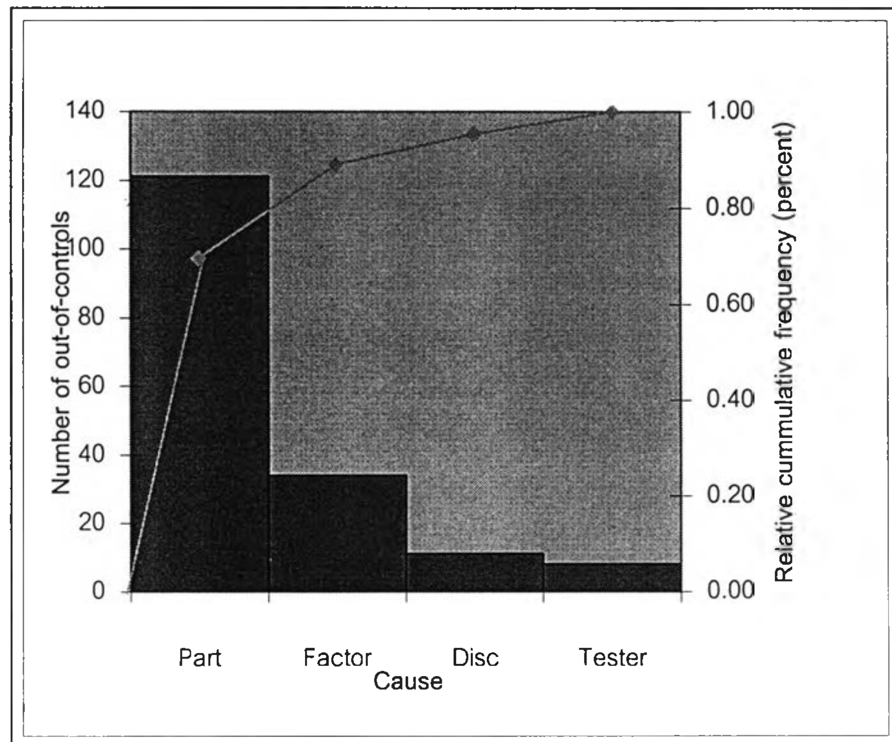


Figure 4.3: Pareto diagram of out of control causes

The causes of out of control were recorded from retest operations when TTO was performing TSPC from September 13, 1999 to September 24, 1999 on Vail. It can be seen

that the major cause of out of control events is from TSPC parts that are used only when running TSPC. It contributed as high as 70% of out of control causes. On the other hand, causes from factoring part, disc, and tester are only 20%, 6%, and 4%, respectively.

From this Pareto diagram, it can be clearly seen that TSPC has only 30% effectiveness, as this percentage is the sum of out of control events that causes are from testing system including factoring parts, disc, and tester. This is because TSPC parts used are poor causing high number of out of control events. The reason for this is that these parts are sensitive so they can be easily damaged such as from handling, holding, falling, and so on, or those parts might have wrong reference. Part sensitive causes changes in reference values of those parts and results in poor repeatability performance over time. Thus, when these parts are run on the tester to determine the difference between reference and reading values, the delta obtained is wrong causing out of control. Additionally, using only 3 TSPC parts per tab is not enough because it is lack of confidence in predicting tester performance. The errors occurred from performing TSPC based on 3 parts are shown below.

Power and Sample Size

1-Sample t Test

Testing mean = null (versus not = null)
Calculating power for mean = null + 3
Alpha = 0.05 Sigma = 1

Sample Size	Power
3	0.7453
2	0.2608

Errors when using three parts is 25.47%. However, when one is desported and removed, only two parts left that causing error high as 73.92%. As a result, the company has to spend time, money, and effort in over taking corrective actions, and it also causes unnecessary tester availability.

To determine the root cause of problem and which causes have most impacted to the company, Failure Modes and Effects Analysis (FMEA) is used to examine potential failures to prevent their occurrences. Thus, the most potential failures can be identified as shown in Table 4.2.

Table 4.2: Failure Modes and Effects Analysis (FMEA)

(Source: "0% HFM and LFM out of control in TSPC", Pornpitakpong, 1997)

Potential Failure Mode	Potential Failure Effects	Severity	Potential Causes	Occurrence	Current Controls	Detection	RPN	Action Recommended
Not enough accuracy of reference	Incorrect reading of TSPC	6	Reference is generated from out of group tester	7	None	8	336	Reference be generated from in-group tester and confirm their reference before be used as TSPC parts
Not clearly understand of TSPC analysis procedure	Incorrect TSPC analysis	6	Improper training	8	None	8	384	Re-train and examination in basis
TSPC parts mechanical change	Incorrect reading of TSPC	6	Poor handling	10	TSPC desport algorithm	7	420	Handling qualification in basis
TSPC parts mechanical change	TSPC out of control	6	Poor head robustness	7	TSPC desport algorithm	7	294	New design of TSPC parts to enhance head robustness
Factor damage	TSPC out of control	8	Not suitable factoring algorithm	6	Factor desport algorithm	8	384	Review the desport algorithm
Factor setup different between factor and production	TSPC out of control	8	Out-of-date setup of factor	5	None	9	360	Coherent setup of factor and production
Factor invent to invent variation	Incorrect reading of TSPC	8	Poor controlling of generating process	5	Impact study	8	320	Strictly control of generating process

It is found that the highest Risk Priority Number (RPN) is from TSPC parts mechanical change. The next highest RPN are from not clearly understanding of TSPC analysis procedure and factoring parts damaged. From this analysis, the problem of TSPC parts damaged is the first priority in taking an action. Then, factoring part problem and lacks of understanding of TSPC can then be focused. The company can eliminate causes of insufficient TSPC understanding by providing training to TTOs, technicians, and engineers. Moreover, causes from factoring parts can be concerned by periodically reviewing the desport algorithm.

In conclusion, drawbacks and limitations of TSPC are summarised. TSPC parts have to be frequently used causing poor repeatability performance. Frequently used increases possibility of parts damage. Additionally, parts are sensitive so they may be damaged from poor handling, or they can be contaminated by cleanroom environment. Sample size that only three parts are used to predict tester performance does not meet statistical requirements. TSPC is too much relying on TTOs that they can make out of control resulting in low effectiveness. TTOs may be lacks of understanding in TSPC analysis, or they usually intend to make SPC pass to reduce workload. Furthermore, the limitations is on TPSC is can be used only on some parameters which follow normal distribution and only product which has satisfied gauge R&R. Results of gauge R&R on each product and parameter are shown in Appendix J. Also, yield which is important to customer's view is not taken into account in decision-making.

From current process of monitoring tester performance, the major cause contribution TSPC less effectiveness is from sensitive TSPC parts damaged from mechanical change. Thus, the improvement should be concerned on finding out a new source of data or the ways to use more reliable parts, and an amount of parts are necessary. Therefore, continuous manufacturing tested data that is the data obtained from testing production parts is considered.

4.3 Analysis Phase

To determine the new methodology of monitoring tester performance and detecting tester problems more effectively, manufacturing tested data that is data from testing all HGAs before shipping to the customers is used instead of performing TSPC. There are the benefits of using this continuous tested data. Firstly, this data is already available. Every HGA has to be tested to confirm that each one can work as intended when it is operating. The manufacturing tested data is kept by the software after those HGAs are tested. Therefore, this data is easy to use. Secondly, manufacturing tested data is free. The company does not need to spend additional cost to indicate the tester performance. For the old method, the company has to pay for performing TSPC. The costs include cost of TSPC parts, cost of generating these TSPC parts by secondary standard generation process, cost of TTOs to perform TSPC, and cost of IAT arms that

used to support TSPC parts. Finally, since manufacturing tested data is from continuous process, it provides a large number of data that would be useful in statistical analysis.

To replace the current method TSPC that control charts are plotted from the difference of readings and references of three parts run on a tester, manufacturing tested data from the test operation of a tester on each day on specified parameter is plotted on the control charts instead. Since LFA and OVW are continuous data and follow normal distribution, X-bar control chart and sigma control chart are used to monitor this manufacturing tested data as shown in Figure 4.4. However, out of control on the control chart cannot indicate tester performance directly because there are other causes resulting in out of control events. They can be mainly from materials (wafer) difference, process change that causes all production parts shift in the same way, or tester performance. For materials, each HGA is composed of the wafer that acts as the slider of HGA that different HGAs might have different wafers, the difference in wafers can cause the shift in mean of tested data. New wafer lot coming is the example of wafer problems. Process change is meant the change on assembly line such as contamination, auto gram load change, etc. This change causes the tested data of the line changed occurs the difference from the other lines. However, HGAs produced from an assembly line will be distributed to certained testers that test that product. For tester issue, tester which has poor performance can result in the shift of test results that cause out of control on control chart. As a result, same wafer quad relation, that is expected to have same performance on same wafer quad, is used to detect the shifts happened so that tester performance can be indicated from this idea.

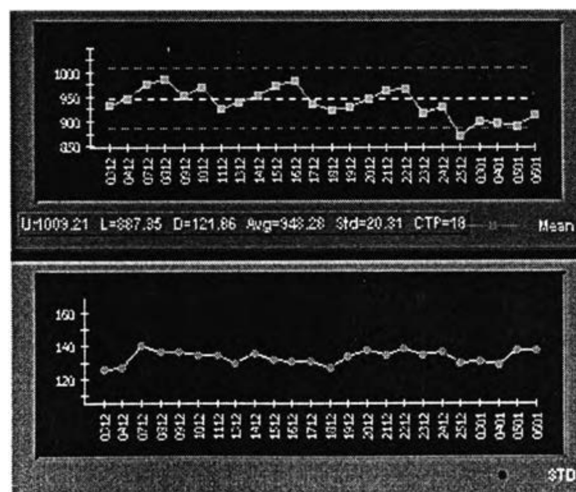


Figure 4.4: X-bar chart shown out of control points of a tester

On wafer analysis, one wafer can be equally divided into four quads, indicating by the first six digits of wafer number. It is recognised that same wafer quad is supposed to have same performance. Hence, detecting the shift on control chart that causes are from tester performance can use this same wafer quad relation. For the process change cause, it can be known from shifting on same wafer quad performance in all testers that load parts from same production line. In the other words, the certain testers that load parts from that production line will shift in the same way.

Only product that has same wafer quad relation can apply this rule. A product has to be tested for same wafer quad relation which is expected to have same performance. In order to prove that same wafer has stable performance on the specified product, same wafers from two different time frames are compared their wafer quad performance on particular parameter.

To compare wafer quad performance on two time frames, sample size of each wafer that is included has to meet statistical requirements from power of test (1-β) at 90% and holding significant level (α) at 5% for LFA and OVW by detect detection difference at 0.85σ of parametric distribution for LFA and 1σ of parametric distribution for OVW. Calculation of sample size could be obtained from Minitab as shown below.

Power and Sample Size of LFA

Testing mean = null (versus not = null)

Calculating power for mean = null + 0.85

Alpha = 0.05, Sigma = 1

Sample Size	Target Power	Actual Power
13	0.8000	0.8031
15	0.8500	0.8642
17	**0.9000**	**0.9079**
21	0.9500	0.9593

Power and Sample Size of OVW

Testing mean = null (versus not = null)

Calculating power for mean = null + 1

Alpha = 0.05, Sigma = 1

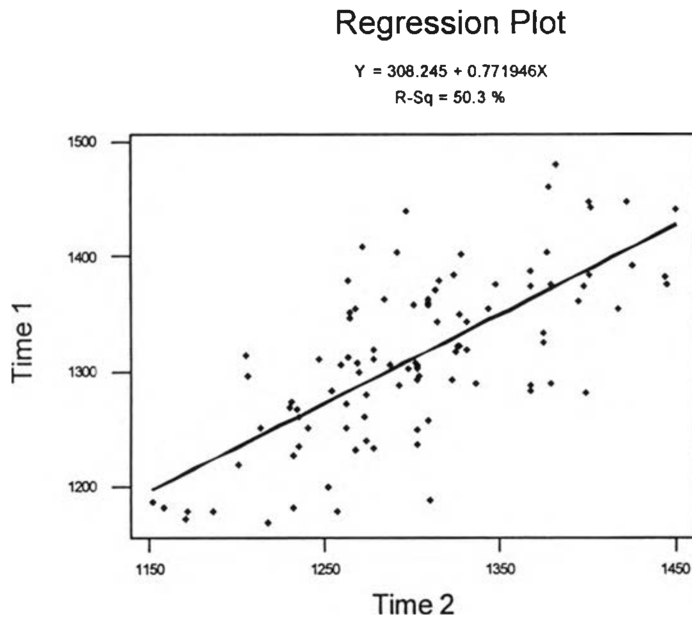
Sample Size	Target Power	Actual Power
10	0.8000	0.8031
12	0.8500	0.8829
13	**0.9000**	**0.9107**
16	0.9500	0.9619

The sample sizes required for each wafer quad are 17 for LFA and 13 for OVW. Wafer quads that have sample sizes meet statistical requirement is called *qualified wafer quads*.

On same wafer quad analysis, five testers are randomly selected, that are ECT391Z, ECT528Z, ECT730Z, ECT736Z, and ECT463Z, for the correlation procedure in wafer quad performance between two time frames. The tested data of those testers on March 1st, 2000 is compared the to the same set of testers on March 8th, 2000 for LFA and OVW parameter.

The strength of relationship between same wafer quads at two different time frames can be determined by correlation coefficient from correlation analysis. P-value tells about the strength of the relationship explained as linear relationship. Referring to Chapter 2 on regression and correlation analysis, if P-value is less than 0.05 (at 5% significant level), same wafer quads at these two time frames have a significant linear relationship. By using Minitab, the results of correlation analysis to compare same wafer quad performance at different time frames for LFA and OVW of Vail are shown below while the raw data are shown in Appendix K and Appendix L for LFA and OVW, respectively.

Vail on LFA: Comparing between different time frames for same wafer quad analysis



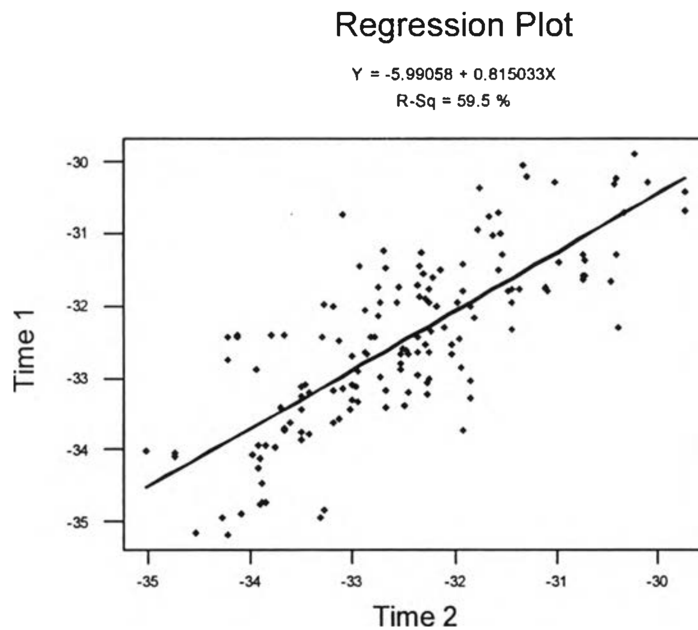
Regression

```
The regression equation is
y = 446 + 0.651 x

Predictor        Coef       StDev          T        P
Constant       446.34       86.01       5.19    0.000
x             0.65120     0.06543       9.95    0.000

S = 47.21       R-Sq = 50.3%     R-Sq(adj) = 49.8%
```

Analysis of Variance

```
Source            DF         SS          MS          F         P
Regression         1     220782      220782      99.06     0.000
Residual Error    98     218415        2229
Total             99     439197
```

Vail on OVW: Comparing between different time frames for same wafer quad analysis



Regression

The regression equation is
y = - 8.81 + 0.730 x

Predictor	Coef	StDev	T	P
Constant	-8.810	1.632	-5.40	0.000
x	0.72952	0.05020	14.53	0.000

S = 0.7210 R-Sq = 59.5% R-Sq(adj) = 59.2%

Analysis of Variance

Source	DF	SS	MS	F	P
Regression	1	109.79	109.79	211.19	0.000
Residual Error	144	74.86	0.52		
Total	145	184.65			

Since P-value on both parameters, LFA and OVW, is less than 0.05, it can be concluded that there is the significant relationship of same wafer quads at different time frames for Vail on both LFA and OVW. For LFA, R-square 50.3% indicates that 50% of variability is explained through linear relationship as OVW has 60% of variability explained through linear relationship.

After the relationship is proved that there is a strong relationship between same wafer quads at two time frames, the samples of five testers at two time frames are tested whether two samples have mean significant differences which indicate they are from

different distributions. This can be done by using single factor ANOVA in which time is a factor. In testing ANOVA, there is the hypothesis testing roadmap shown in Figure 4.5 that must be followed when doing the tests.

Because ANOVA is supported to the samples that are independent and normally distributed with equal variances, the normality test and homogeneity of variance are used to verify the assumptions. Referring to Chapter 2 on ANOVA, P-value is used to indicate the normality and equality of variances. In case of test for normality, P-value that is greater than 0.05 indicates the normal distribution. For test of variance, if P-value is less than 0.05, the two variances are not equal. Otherwise, variances are supposed to be equal from a given evidence so that ANOVA can be used. For ANOVA, if P-value of t-test is less than 0.05, it shows that there is the significant difference in means from two time frames populations. It indicates that wafer of that product does not stable over time. On the other hand, if P-value is more than 0.05, there are no evidence to reject the null hypothesis that is mentioned that $\mu_1 = \mu_2$. As a result, there is no shift happened between two time frames that indicate the wafer performance stability within same wafer quad. By using Minitab, the results of comparison the manufacturing tested data between different time frames on same wafer quads for LFA and OVW of Vail are shown below.

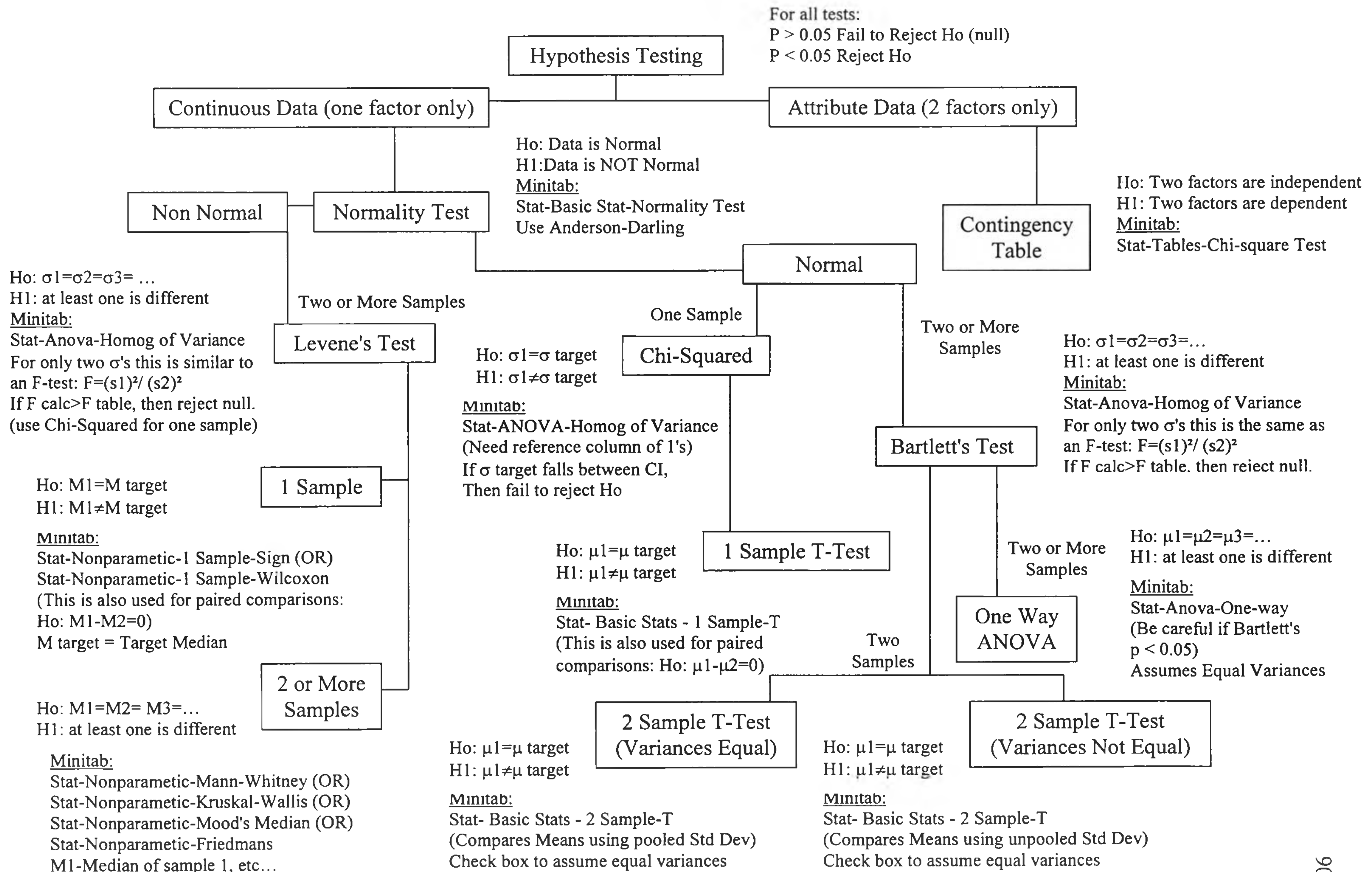
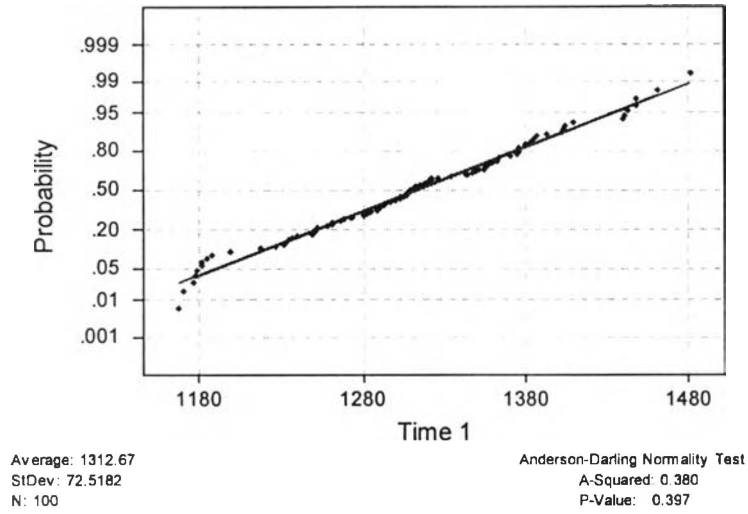


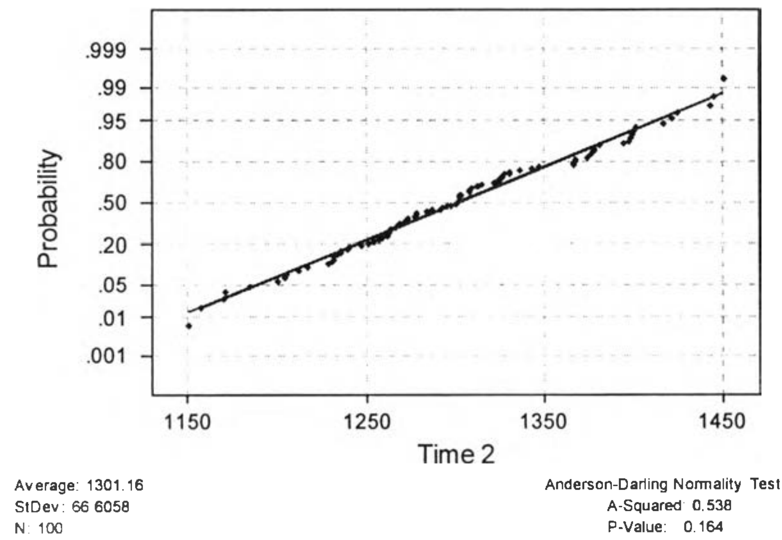
Figure 4.5: Hypothesis testing roadmap (Source: Six Sigma manual)

Vail on LFA: Comparing between different time frames for same wafer quad analysis

Normal Probability Plot



Normal Probability Plot



Homogeneity of Variance Test for Mean

95% Confidence Intervals for Sigmas | Factor Levels

F-Test

Test Statistic: 1.185

P-Value : 0.399

Levene's Test

Test Statistic: 0.791

P-Value : 0.375

Mean

One-way Analysis of Variance

```
Analysis of Variance for Mean
Source       DF          SS          MS          F         P
Factor        1        6626        6626       1.37     0.244
Error       198      959827        4848
Total       199      966452
                                         Individual 95% CIs For Mean
                                         Based on Pooled StDev
Level         N        Mean       StDev  --------+---------+---------+--------
1           100      1312.7        72.5            (-----------*----------)
2           100      1301.2        66.6   (----------*-----------)
                                         --------+---------+---------+--------
Pooled StDev =         69.6                     1296      1308      1320
```

Vail on OVW: Comparing between different time frames for same wafer quad analysis

Normal Probability Plot

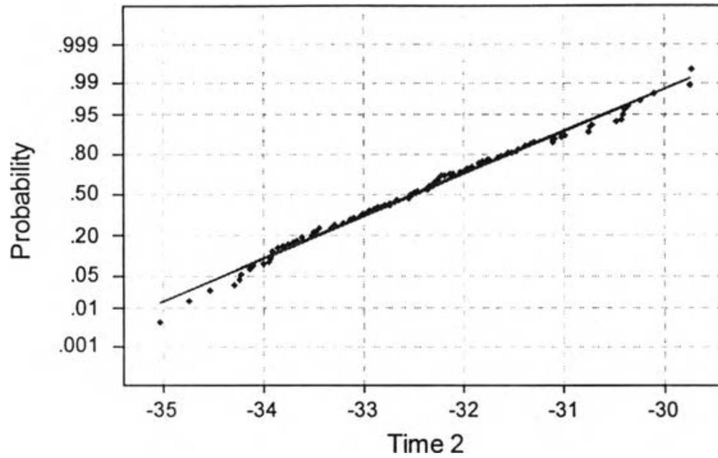
Probability

Time 1

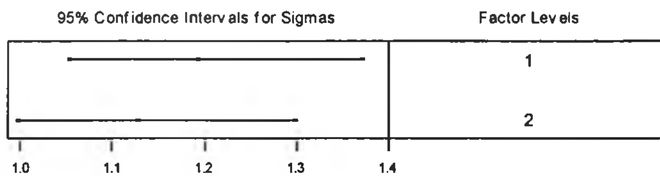
Average: -32.4882
StDev: 1.19279
N: 146

Anderson-Darling Normality Test
A-Squared: 0.296
P-Value: 0.590

Normal Probability Plot



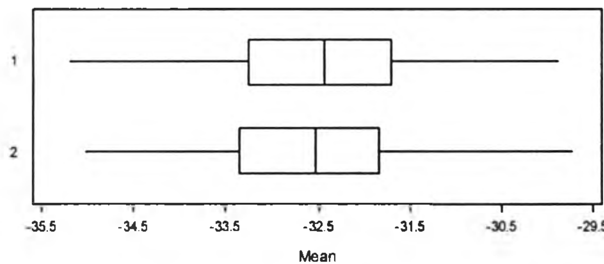
Homogeneity of Variance Test for Mean



F-Test

Test Statistic: 1.117

P-Value : 0.505



Levene's Test

Test Statistic: 0.466

P-Value : 0.495

One-way Analysis of Variance

```
Analysis of Variance for Mean
Source     DF        SS        MS        F        P
Factor      1      0.04      0.04     0.03    0.866
Error     290    390.95      1.35
Total     291    390.99
                                   Individual 95% CIs For Mean
                                   Based on Pooled StDev
Level       N      Mean     StDev  ------+---------+---------+---------+
1         146   -32.488     1.193    (---------------*--------------)
2         146   -32.511     1.128   (---------------*---------------)
                                   ------+---------+---------+---------+
Pooled StDev =     1.161              -32.64    -32.52    -32.40    -32.28
```

From the calculation of Minitab on both LFA and OVW, the sample tested data of two time frames conform normal distribution with equal variances as indicated by P-values that are greater than 0.05 on normality test and more than 0.05 on F-test. Then, ANOVA can be determined. Since P-value of ANOVA is greater than 0.05, they can be concluded that there are no significant differences between same wafer quad performance on two different time frames. It indicates that wafer quads at different time frames which are from the same population does not provide the significant difference within same wafer quads. It can be concluded that Vail is the product the same wafer quad has stable performance.

Hence, same wafer quad relation on Vail is qualified to be used for this analysis because it is stable. However, this test should be done periodically to ensure that this product is still in stable condition. Also, this method would be applied to any products that would use the proposed process to monitor tester performance.

When good correlation of same wafer quad exists among different time frames and no significant difference in means of two time frames, it means there is wafer quad stability. Since there is wafer quad relation on Vail both at LFA and OVW, manufacturing tested data on same wafer quad can be used to monitor tester performance. This analysis is used to detect tester problems resulting in the shift of wafer quad performance.

4.4 Improvement Phase

As current TSPC has low effectiveness in detecting tester problems as specified in measurement phase, the new methodology is created by using continuous manufacturing tested data from the production. In order to use manufacturing tested data to identify the tester performance instead of using three parts known readings running across testers, same wafer quad relation is studied as mentioned in analysis phase.

From knowledge of same wafer quad relation, it is recognised that there is no significant difference in means within same wafer quad that provides stable performance.

This rule can be used to detect tester performance when there is a shift in same wafer quad performance.

To detect out of control on control chart whether that shift is from tester performance, same wafer quad relation is used. On SPC, manufacturing tested data each day of a tester will be tested hypothesis testing on same wafer quad basis comparing to the tested data of the past on that tester to detect the shift happened at same wafer quad. Tested data of the past is the average of tested data on the past days as many as data is available, usually 24 days. If the significant difference in means of those two sets of data exists, it means that there is a cause of the shift of manufacturing tested data on same wafer quad. That cause is supposed to be mainly from tester performance or process change.

However, comparing the hypothesis testing of that tester on a day to different time, historical data on the past day, is difficult to predict tester performance because sample size of qualified wafer quads is very small or even zero that means no same wafer quad matching. Thus, it lacks of confidence in predicting tester performance. To solve this problem, tested data each day of interested tester is compared to average data of other testers that test same product. Hence, the interested tester is also compared to the rest of testers at same time and the rest of testers at different time. In conclusion, the interested tester that is denoted as "*own tester*" will be compared to the "*same tester at different time frame*" that denoted as "*SD*", "*different testers at same time frame*" that denoted as "*DS*", and "*different testers at different time frame*" that denoted as "*DD*". Different testers are meant all the rest of the tester, giving in control, testing same product that the average of them is used. Different time means averaged out tested data at in control on the past days as long as data available, usually 24 days.

To detect the shift in same wafer quad performance, inferential statistical analysis or hypothesis testing is useful as a tool to be used in comparing own tester to SD, DS, and DD. To perform this hypothesis testing, hypothesis roadmap in Figure 4.5 should be followed.

Not only out of control points on control chart, but in control points should also be investigated. From SPC viewpoint, the actions are not necessary to be done if the process

is in statistical control. However, there are many factors, other than tester performance, affecting to SPC to be in control such as wafer performance. Thus, tester problems might be taken place even though SPC is in control. Hence, in control is investigated if it responses to tester performance.

After the tester is compared to SD, DS, and DD on same wafer quads, the significant differences between the means of any two sets of comparison are mainly caused from process change or tester problem. Therefore, when significant difference is indicated, the investigation is required to find out the causes of this shift in means whether it is from process changes or tester problems that tester problems will be focused first because of low possibility of process change. In addition, process change can be noticed from shifts of other testers.

The hypothesis testing procedure shown in Figure 4.5 is followed for each pair of comparison that are own tester versus SD, own tester versus DS, and own tester versus DD when SPC is out of control and in control. In addition to testing three pairs of those, the comparison between DS and DD is also concerned. Testing DS against DD can be used as the reference to identify the process condition. The results of this test indicate the stability of the process. If there is the significant difference between these references, the company has to investigate this before doing the further testing. If the process is normally operated that no change occurs, the result of this testing is likely to show no significant difference between these two means.

On hypothesis testing to detect the shift happened on same wafer quad, the samples are firstly checked for normality to appropriately select the method use for hypothesis testing. From the graph of normality, P-value is identified. It can be concluded that the sample follows normal distribution when P-value is greater than 0.05 (5% significant level of Type I error). When the normality is verified for two samples, homogeneity of variance is tested by Bartlett's Test for the equality of their variances. For normal distribution, F-test is used to indicate the significant difference of variances that P-value should be greater than 0.05. Otherwise, cause of failing F-test should be investigated. After that, the appropriate T-test can then be selected to compare the significant difference between two means of the samples. For T-tests, these two samples have no significant difference in mean if P-value is greater than 0.05 because no evidence

indicates for the significant difference. When two samples have the same mean, the cause of out of control is unlikely to be from tester problems or process changes. On the other hand, if P-value is less than 0.05, there is the significant difference between in means of two. It could be supposed that there is a shift in same wafer quad performance that tester issue will be focused first.

To test the hypothesis testing of two samples to compare their variances and means, normality of those samples is important; especially, F-test is more sensitive to normality. Here, data is assumed to follow normal distribution, especially when sample size is more than 30 from Central limit Theorem, as shown in Figure 4.6 for LFA and Figure 4.7 for OVW. Raw data of LFA tested on ECT 419Z on March 1st, 2000 is shown in Appendix M, and raw data of OVW tested on ECT738Z on March 1st, 2000 is shown in Appendix N.

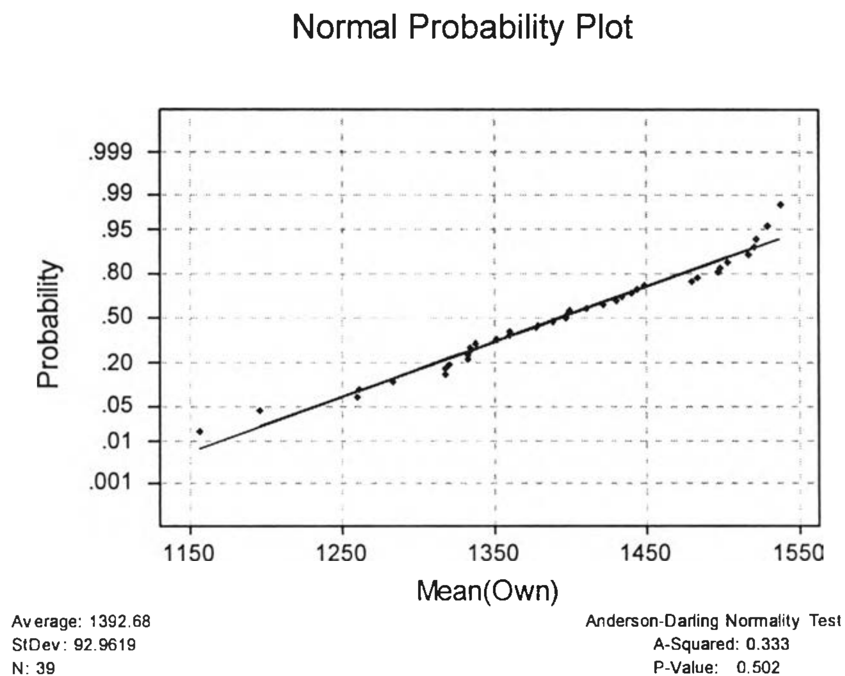


Figure 4.6: Normality test for LFA

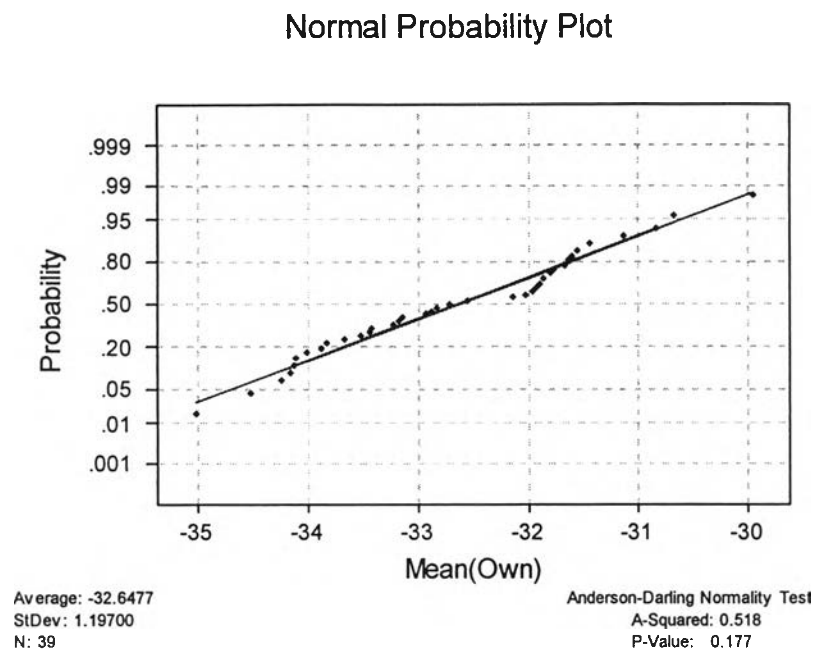
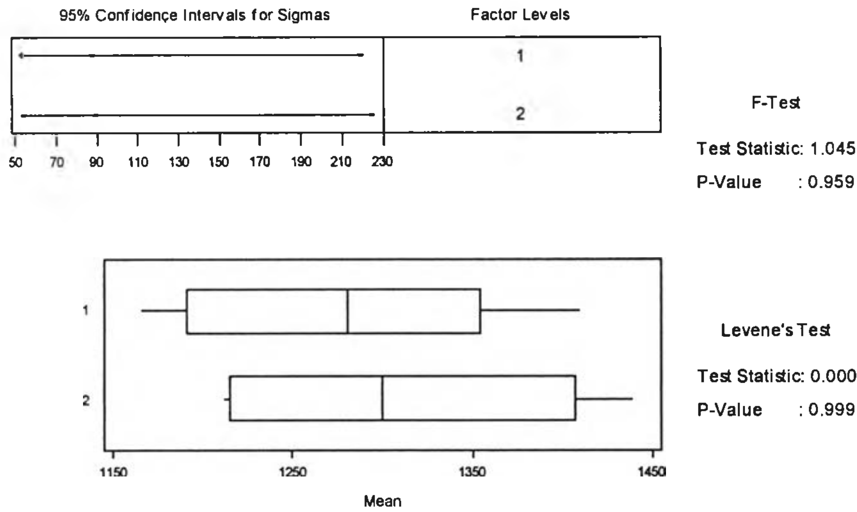


Figure 4.7: Normality test for OVW

Examples of hypothesis testing on LFA to detect the shift from same wafer performance indicating tester problems are given below that calculation is based on Minitab. Own tester is compared to SD, DS, and DD both at in control of SPC and out of control of SPC. Moreover, comparing between DS and DD is also provided. Raw data of hypothesis testing at in control is in Appendix O, and raw data of hypothesis test at out of control is in Appendix P.

Vail on LFA: In control, no significant difference on any pairs of comparison (ECT624Z on 1/3/2000)

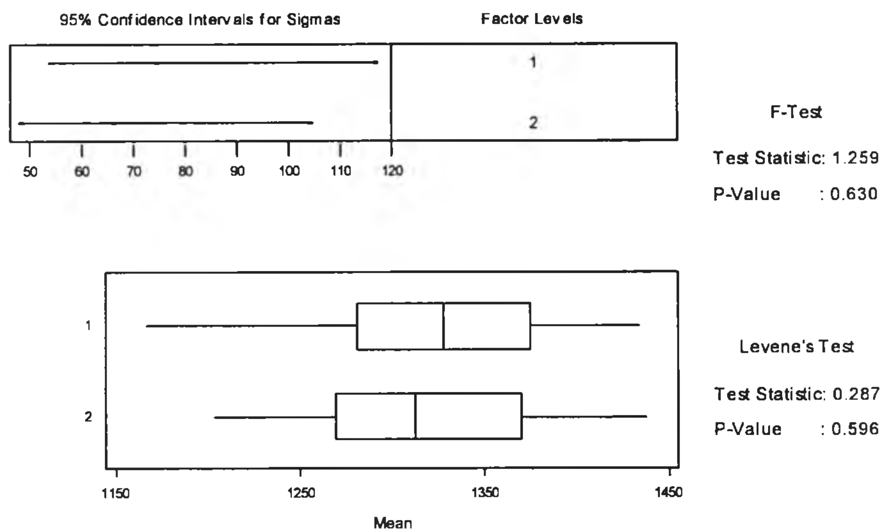
→ ***Own tester & SD***



Two Sample T-Test and Confidence Interval

```
Two sample T for Mean

Factor       N      Mean     StDev   SE Mean
1            7    1283.3      87.4        33
2            7    1305.0      89.3        34

95% CI for mu (1) - mu (2): ( -126,  82)
T-Test mu (1) = mu (2) (vs not =): T = -0.46  P = 0.65  DF = 11
```

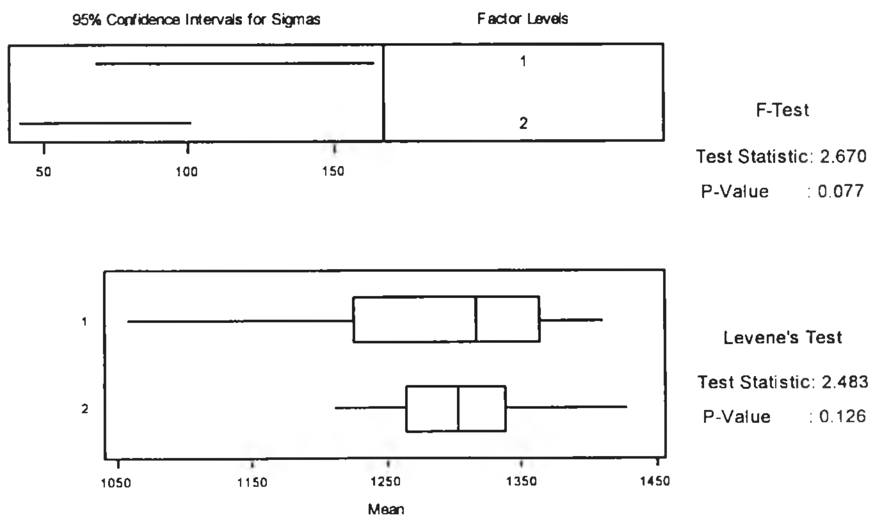
➔ ***Own tester & DS***



Two Sample T-Test and Confidence Interval

```
Two sample T for Mean

Factor         N       Mean      StDev    SE Mean
1             19     1319.1       74.3         17
2             19     1322.0       66.2         15

95% CI for mu (1) - mu (2): ( -49,  43)
T-Test mu (1) = mu (2) (vs not =): T = -0.13  P = 0.90  DF = 36
Both use Pooled StDev = 70.4
```

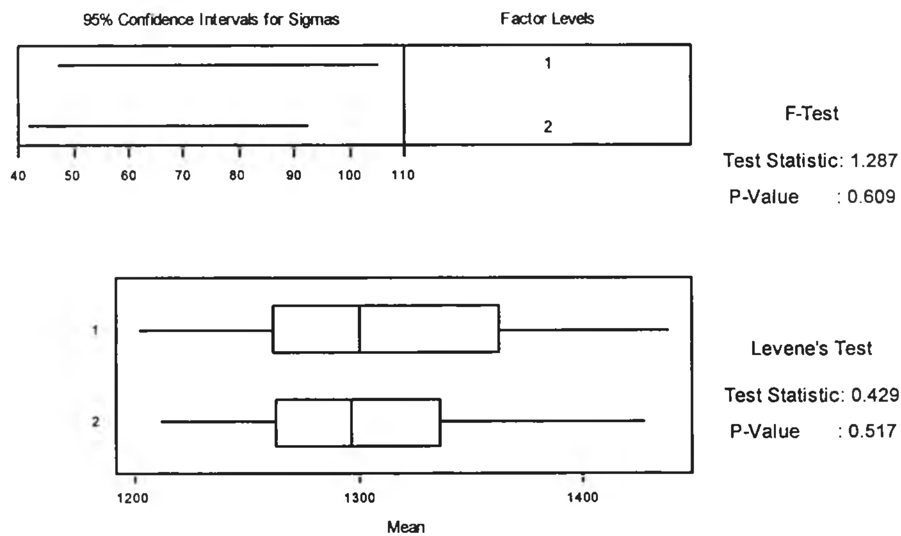
➔ ***Own tester & DD***



Two Sample T-Test and Confidence Interval

```
Two sample T for Mean

Factor        N       Mean      StDev   SE Mean
1            15     1289.9       96.8        25
2            15     1306.2       59.2        15

95% CI for mu (1) - mu (2): ( -77,  44)
T-Test mu (1) = mu (2) (vs not =): T = -0.56  P = 0.58  DF = 23
```

→ ***DS & DD***

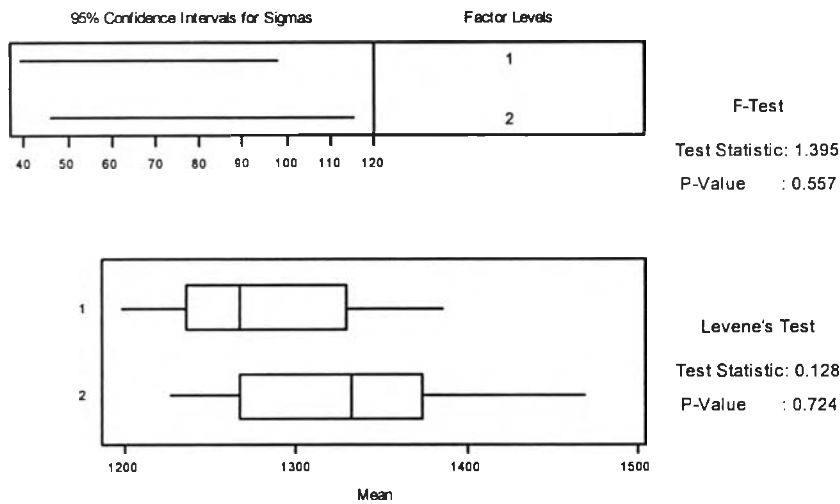


Two Sample T-Test and Confidence Interval

```
Two sample T for Mean

Factor        N       Mean      StDev   SE Mean
1            18     1307.8       65.7        15
2            18     1298.8       57.9        14

95% CI for mu (1) - mu (2): ( -33,  51)
T-Test mu (1) = mu (2) (vs not =): T = 0.43  P = 0.67  DF = 33
```

Vail on LFA: In control, significant difference at least one pair of comparison (ECT436Z on 1/3/2000)

➔ ***Own tester & DS***

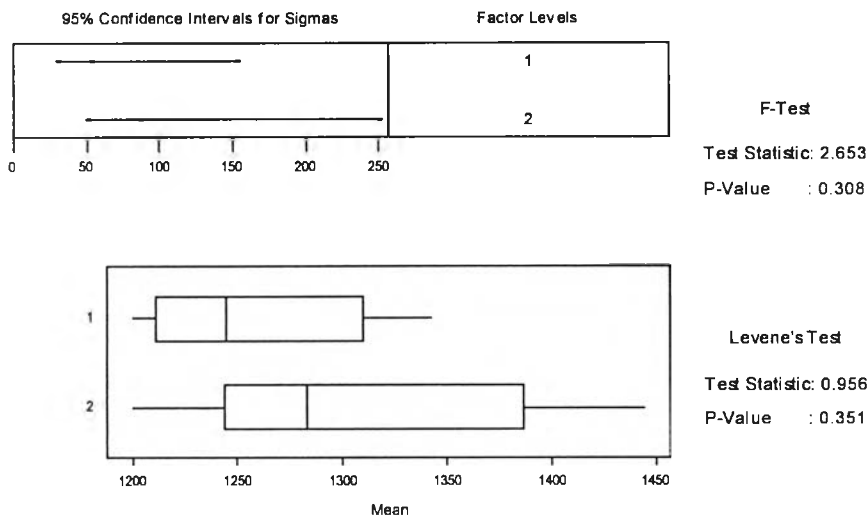


Two Sample T-Test and Confidence Interval

```
Two sample T for Mean

Factor        N      Mean      StDev   SE Mean
1            14    1279.4       56.3        15
2            14    1327.7       66.4        18

95% CI for mu (1) - mu (2): ( -96,  -0)
T-Test mu (1) = mu (2) (vs not =): T = -2.07  P = 0.048  DF = 26
Both use Pooled StDev = 61.6
```

➔ *Own tester & DD*

Homogeneity of Variance Test for Mean

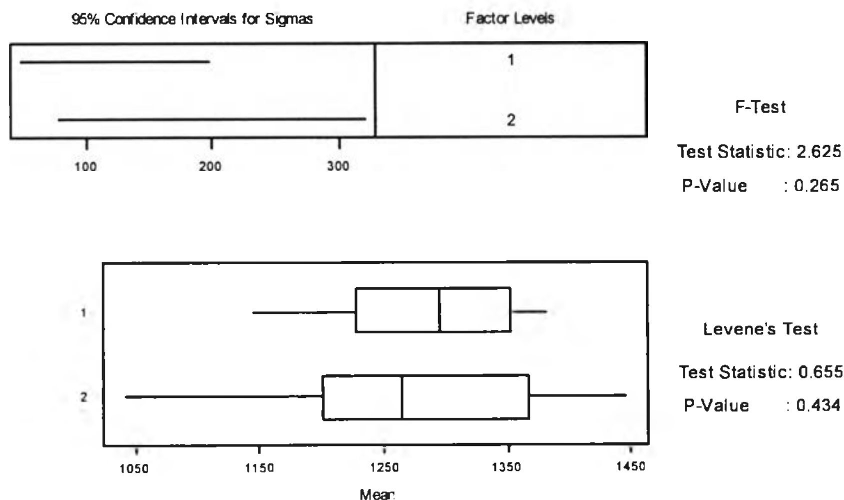


Two Sample T-Test and Confidence Interval

```
Two sample T for Mean

Factor        N      Mean     StDev   SE Mean
1             6    1257.4      53.8        22
2             6    1306.0      87.6        36

95% CI for mu (1) - mu (2): ( -145,  48)
T-Test mu (1) = mu (2) (vs not =): T = -1.16  P = 0.28  DF = 8
```

➔ *DS & DD*

Homogeneity of Variance Test for Mean

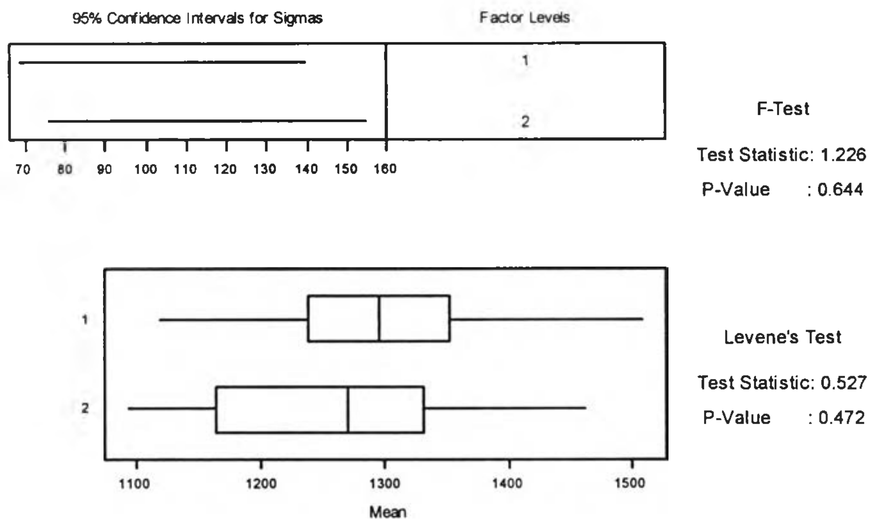


Two Sample T-Test and Confidence Interval

```
Two sample T for Mean

Factor        N       Mean      StDev   SE Mean
1             7     1282.9       78.8        30
2             7       1268        128        48

95% CI for mu (1) - mu (2): ( -114,  143)
T-Test mu (1) = mu (2) (vs not =): T = 0.26  P = 0.80  DF = 9
```

Vail on LFA: Out of control, significant difference at least one pair of comparison (ECT435Z on 28/1/2000)

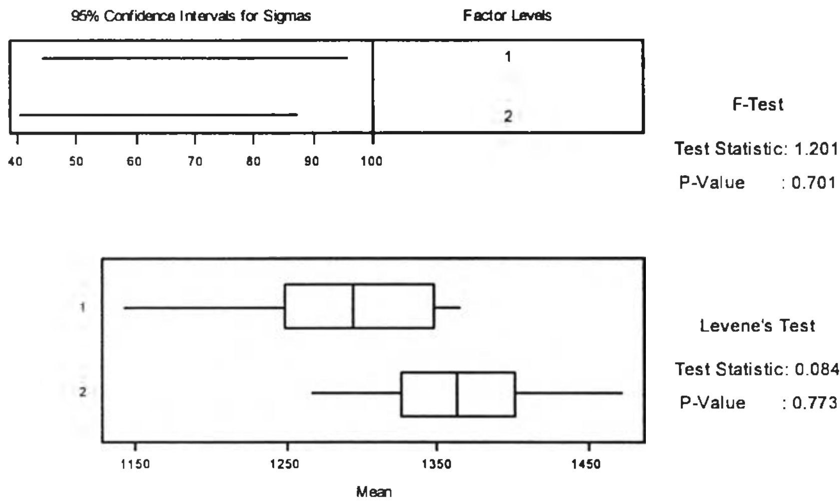
➔ ***Own tester & SD***



Two Sample T-Test and Confidence Interval

```
Two sample T for Mean

Factor        N       Mean      StDev   SE Mean
1            22     1289.9       92.4        20
2            22       1256        102        22

95% CI for mu (1) - mu (2): ( -26,  93)
T-Test mu (1) = mu (2) (vs not =): T = 1.14  P = 0.26  DF = 41
```

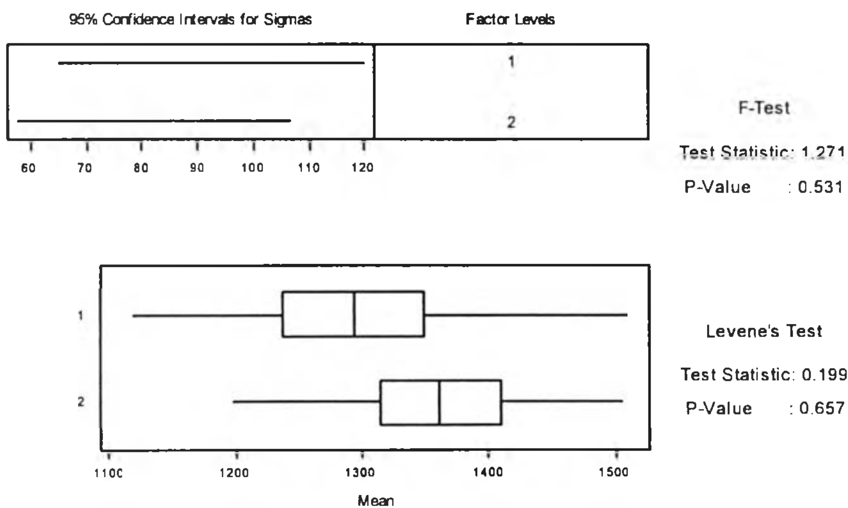
→ ***Own tester & DS***



Two Sample T-Test and Confidence Interval

```
Two sample T for Mean

Factor        N      Mean     StDev   SE Mean
1            19    1288.8      60.8        14
2            19    1363.9      55.5        13

95% CI for mu (1) - mu (2): ( -113,  -37)
T-Test mu (1) = mu (2) (vs not =): T = -3.98  P = 0.0003  DF = 35
```

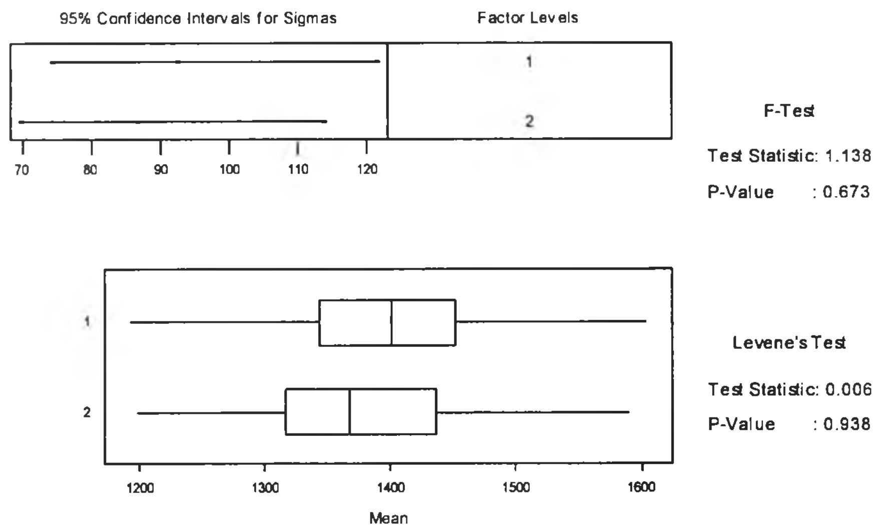
→ ***Own tester & DD***



Two Sample T-Test and Confidence Interval

```
Two sample T for Mean

Factor        N      Mean     StDev   SE Mean
1            29    1284.4      84.6        16
2            29    1358.5      75.1        14

95% CI for mu (1) - mu (2): ( -116,  -32)
T-Test mu (1) = mu (2) (vs not =): T = -3.53  P = 0.0009  DF = 55
```

→ ***DS & DD***

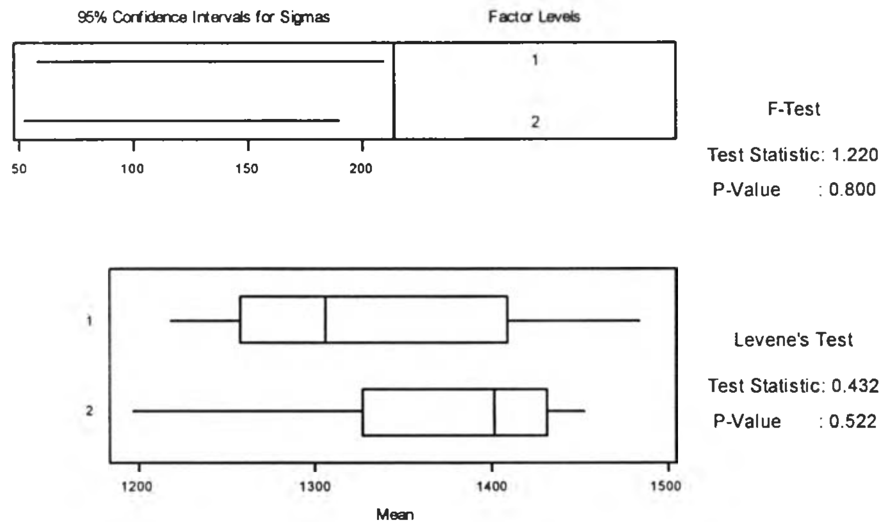


Two Sample T-Test and Confidence Interval

```
Two sample T for Mean

Factor        N      Mean     StDev   SE Mean
1            44    1399.5      92.5        14
2            44    1375.7      86.7        13

95% CI for mu (1) - mu (2): ( -14,  62)
T-Test mu (1) = mu (2) (vs not =): T = 1.25  P = 0.22  DF = 85
```

Vail on LFA: Out of control, no significant difference on any pairs of comparison (ECT602Z on 17/2/2000)

➔ ***Own tester & SD***

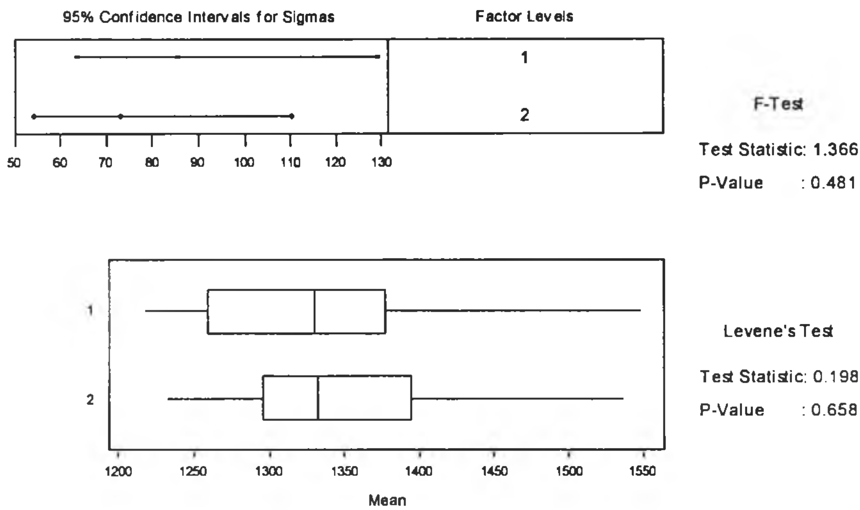


Two Sample T-Test and Confidence Interval

```
Two sample T for Mean

Factor        N      Mean      StDev    SE Mean
1             8    1327.4       91.5         32
2             8    1372.1       82.9         29

95% CI for mu (1) - mu (2): ( -139,  50)
T-Test mu (1) = mu (2) (vs not =): T = -1.02  P = 0.32  DF = 13
```

→ *Own tester & DS*

Homogeneity of Variance Test for Mean

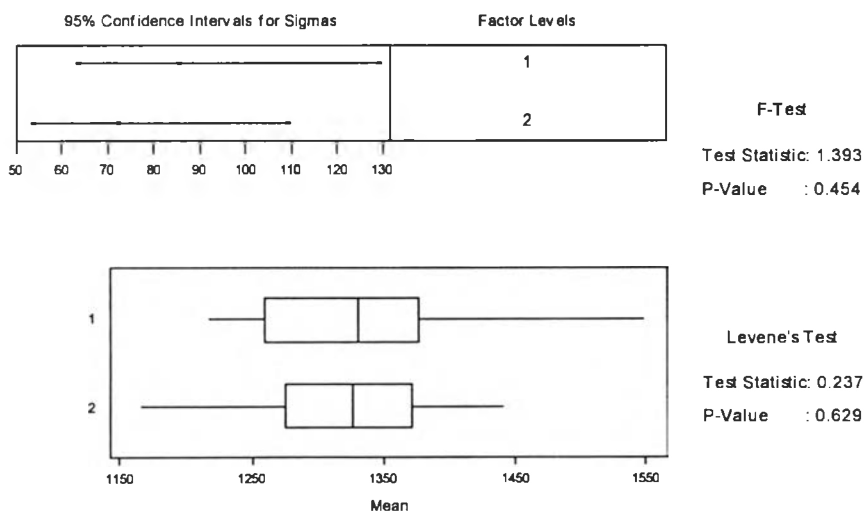


Two Sample T-Test and Confidence Interval

```
Two sample T for Mean

Factor        N       Mean      StDev    SE Mean
1            22     1335.5       85.5         18
2            22     1350.9       73.1         16

95% CI for mu (1) - mu (2): ( -64,  33)
T-Test mu (1) = mu (2) (vs not =): T = -0.64  P = 0.52  DF = 41
```

→ *Own tester & DD*

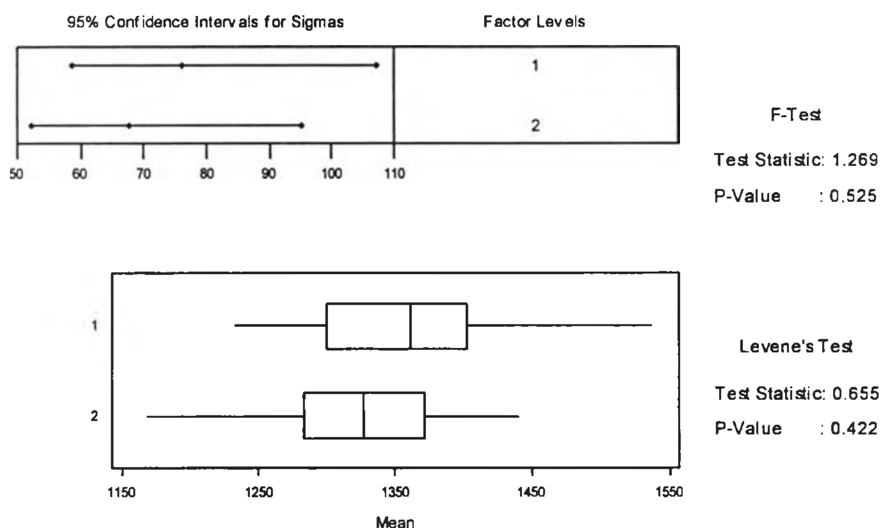
Homogeneity of Variance Test for Mean



Two Sample T-Test and Confidence Interval

```
Two sample T for Mean

Factor        N      Mean      StDev   SE Mean
1            22    1335.5       85.5        18
2            22    1318.0       72.4        15

95% CI for mu (1) - mu (2): ( -31,  66)
T-Test mu (1) = mu (2) (vs not =): T = 0.73  P = 0.47  DF = 40
```

→ ***DS &DD***



Two Sample T-Test and Confidence Interval

```
Two sample T for Mean

Factor        N      Mean      StDev   SE Mean
1            30    1359.2       76.1        14
2            30    1322.4       67.6        12

95% CI for mu (1) - mu (2): ( -0,  74)
T-Test mu (1) = mu (2) (vs not =): T = 1.98  P = 0.052  DF = 57
```

As calculated above by using Minitab, the results of those hypothesis results when SPC is out of control and in control on LFA are summarised in Table 4.3.

Table 4.3: Relationships between out of control / in control and hypothesis testing results on LFA

SPC	Tester	Comparison	Hypothesis result
In Control	ECT624Z	Own tester & SD	Not significant
		Own tester & DS	Not significant
		Own tester & DD	Not significant
		DS & DD	Not significant
	ECT436Z	Own tester & DS	Significant
		Own tester & DD	Not significant
		DS & DD	Not significant
Out of control	ECT435Z	Own tester & SD	Not significant
		Own tester & DS	Significant
		Own tester & DD	Significant
		DS & DD	Not significant
	ECT602Z	Own tester & SD	Not significant
		Own tester & DS	Not significant
		Own tester & DD	Not significant
		DS & DD	Not significant

From this table, it can be seen that when out of control is taken place, the manufacturing tested data of a tester compared to other testers can give hypothesis testing results either significant difference or not significant difference. Likewise, in case of in control, the results of hypothesis testing might be significant difference or not significant difference. If own tester has significant difference when comparing to SD, DS, or DD, tester performance should be investigated. However, DS versus DD should be observed. Since there are less relationship between in control / out of control and hypothesis testing result, it indicates that SPC control charts cannot be used to predict the hypothesis testing results. In the other words, SPC cannot tell about the tester problems that would be indicated when there is the significant difference between own tester and other testers or its own tester on different time frame. However, out of control should be concerned first because it causes more severity.

To monitor tester performance by using knowledge of hypothesis testing which is based on same wafer quad comparison, manufacturing tested data each day of all ET

testing Vail will be plotted on SPC by tester to observe out of control events, and hypothesis testing is implemented on all of those, as well as the example given, to detect the shift happened from tester performance. Since this calculation would be complex because of a lot of data concerned, the system has been created to automatically calculate the above analysis. This system has been implemented on the company's internal webside by loading manufacturing tested data to appear on the webside. Then, those analysis can be shown on this webside. This system is composed of several pages that they are used for monitoring and analysing tester performance. Therefore, each page is next explained for its structures and its uses.

The page that would be firstly appeared when coming into this webside is the *location page* (Figure 4.8). This page shows lists of testers by the selected product at specified parameter when the product and parameter interested can be chosen at the top of the page. The layout of those testers appeared on the webside is arranged according to the real location where testers are situated that four cleanrooms, which is cleanroom A, cleanroom B, cleanroom C, and cleanroom D, are provided. Furthermore, colours of testers also indicate how long those testers have been released into the production.

- Blue tester means new released tester that has been online more than 20 hours but less than 20 shifts.
- Yellow tester means tester that has been online more than 20 shifts but less than 20 days.
- Green tester means tester that has been online more than 20 days.

The most interesting feature of this page is the flashing that indicates the tester's status, out of control and significant difference. The out of control status is obtained from SPC as in X-bar control chart that would be shown on the *graph page*. The significant difference is identified when using statistical inferences or hypothesis testing in comparing the interested tester to SD, DS, and DD as shown on *wafer analysis page*. Flashing colours are used in identifying the tester's status that red indicates out of control and significant difference, pink indicates out of control but no significant difference, green indicates in control but significant difference, and no flashing indicates in control

and no significant difference. This also refers to the priorities when testers are investigated.

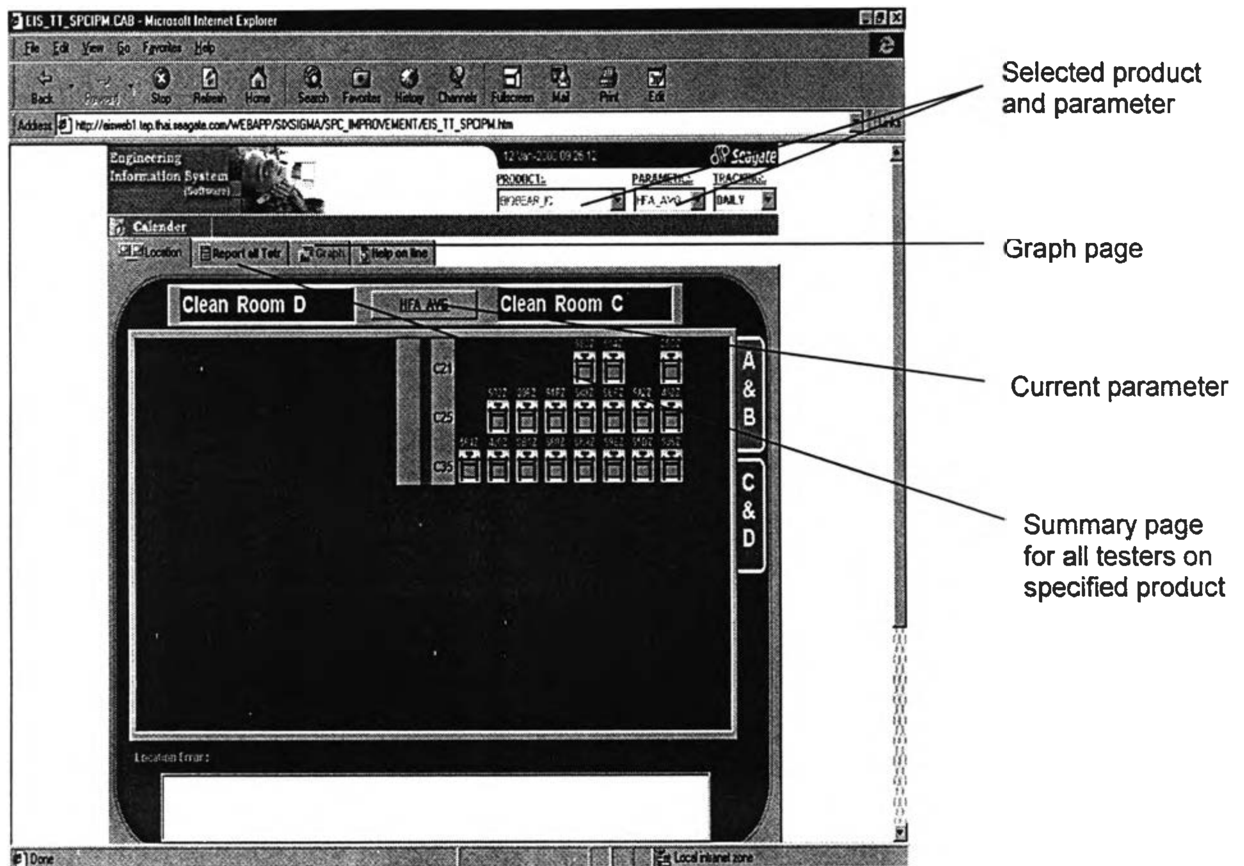


Figure 4.8: Location page

The tester which is flashing can be investigated by clicking at them. Then, the *graph page* (Figure 4.9) is immediately come up that shows SPC graphs, X-bar control chart and sigma chart (S-chart), of the selected tester at specified parameter. On this page, it shows the trend in the latest 25 days on X-bar chart plotted by manufacturing tested data and on sigma chart calculated based on total parts tested. In the table, it also specifies count, mean, sigma, and yield, which is the percentage of pass parts after testing, of manufacturing tested data by daily basis on the selected parameter of interested product. It can be seen that testing manufacturing tested data in a day has to be completed before the analysis of tester performance will be done on that day.

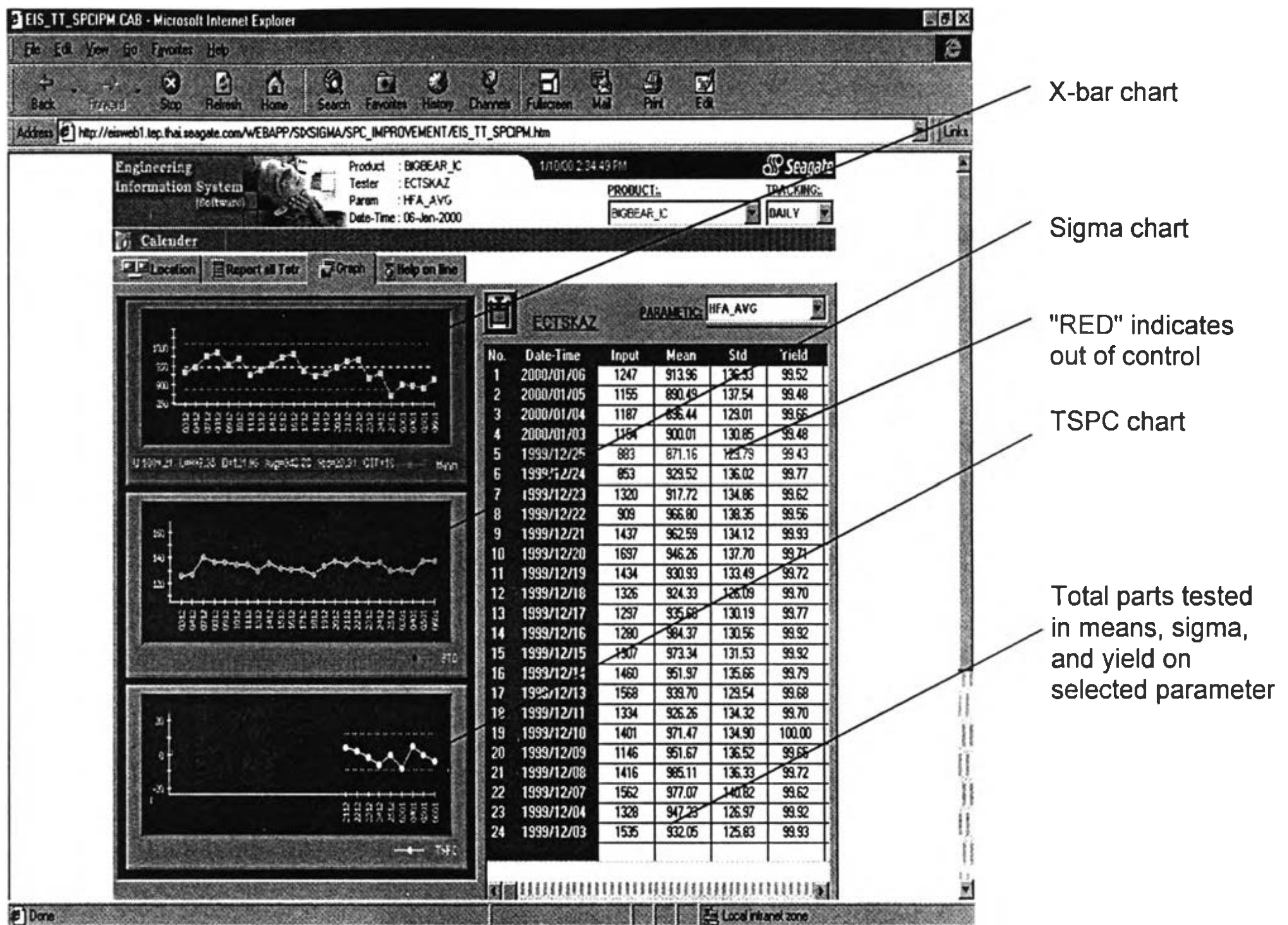


Figure 4.9: Graph page

The control limits of control charts on this page are calculated based on 20 points which is automatically calculated daily to catch up the change in wafer performance or process. The minimum and maximum points are automatically removed to reduce variation that might causes from outliers. The control limits of new release tester that has been released less than 20 days can be calculated from shift calculation that is from 20 shifts. For tester that has been released less than 20 shifts, the control limits are not provided yet until it has been operated for 20 shifts or more.

Basically, out of control on X-bar chart could be from three reasons. Firstly, from the shift or change on wafer performance. By this case, wafer analysis on hypothesis testing will show no significant difference when same wafer quads tested on other testers at same time and other time frames are compared. Secondly, if the change is from the change in process, the hypothesis testing results on other testers will shows the clues. Sometimes, it is shown by the significant difference between DS and DD. Finally, out of

control is caused from the testing system that is the most important thing that this project has focused. In this case, the statistically significant difference will be shown when comparing the interested tester to other testers which tested same wafer quads as shown in *wafer analysis page*.

Wafer analysis page (Figure 4.10) can be come up when any rows in the table on *graph page* is clicked, that the red row indicates out of control status on that tester. The main idea of this page is using the manufacturing tested data on same wafer quad comparison to detect the shift happened statistically so that the root causes of that shift can be investigated. Own tester is compared to SD, DS, and DD by using inference statistical analysis, F-test and 2-sample T-test. F-test is used to compare sigma of two populations while T-test is used to compare the means of two populations. The results of the comparison are expressed in P-value that less than 0.05 is meant significant difference in means of two populations. It indicates that there is a shift in same wafer quad performance that the cause has to be investigated for tester problems. The *wafer analysis page* is including:

- A list of same wafer quads tested on own tester and same wafer quads tested on own tester but other time frame, other testers at same time frame, and other testers at different time frame.
- Sample size of each wafer quad needed based on beta risk (Type II error) and detection difference.
- Numbers of qualified wafer quads, count of tested parts on all qualified wafer quads, mean and sigma of all qualified wafer quads tested on SD, DS, and DD. Furthermore, it also shows count, mean, sigma, and yield of each qualified wafer quad.
- The results of significant difference in P-value when compared own tester against SD, own tester against DS, own tester against DD, and DS against DD based on same wafer quads that sample sizes of each qualified wafer quad meet statistical requirements.

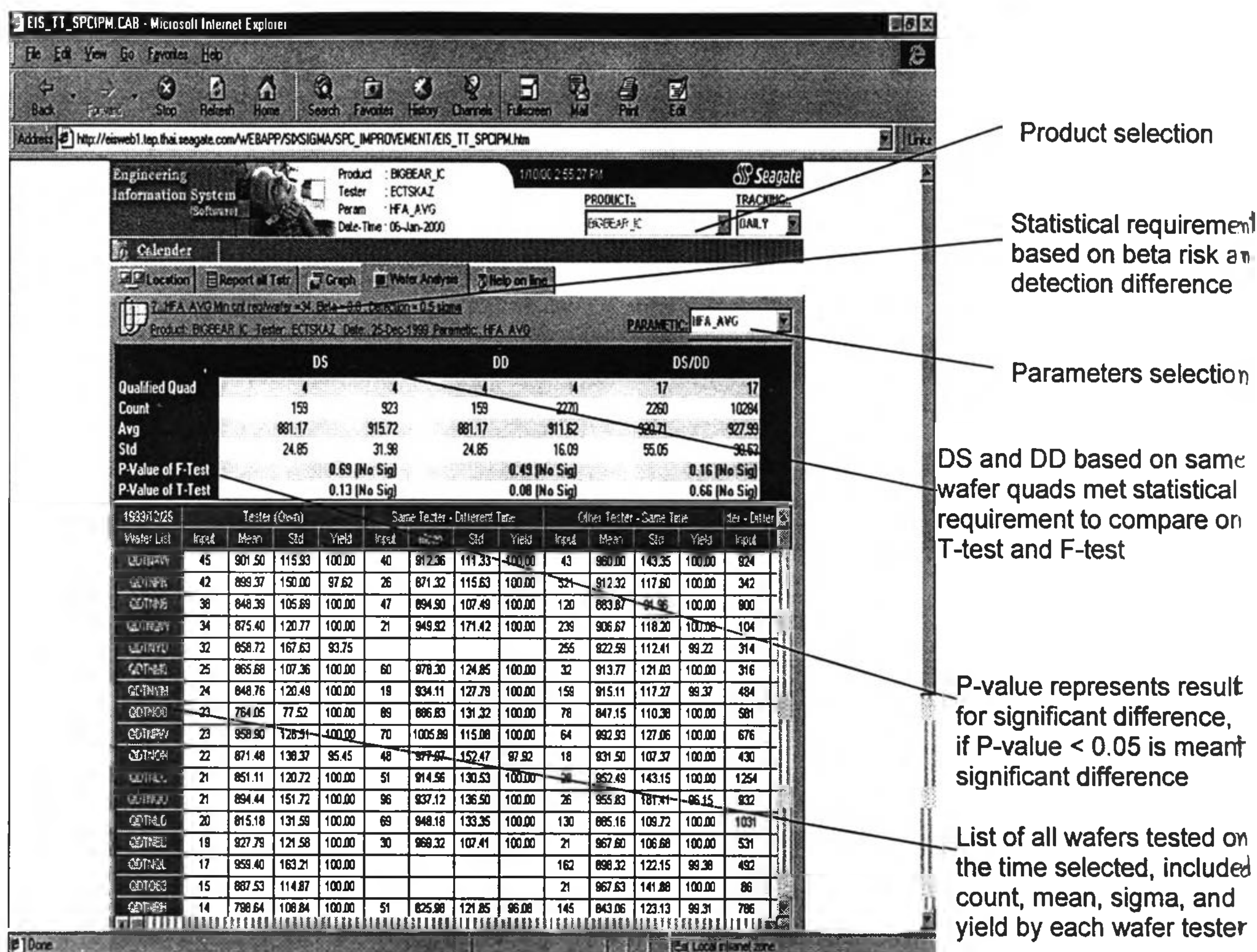


Figure 4.10: Wafer analysis page

As the wafer analysis page shows only the hypothesis results of the selected tester at specified parameter, *report all tester page* (Figure 4.11) is provided. It is the summary of the hypothesis testing results between own tester and SD, DS, and DD of all testers on the specified product for all parameters in one page. For the wafer analysis page, it may take time to observe the hypothesis testing result of each tester because it can be observed only one-by-one parameter on a tester. *Report all tester page* provides a quick look so that time in identifying the tester performance has been shortened.

TESTER	HFA_AVG CL_WD	In/Out	DS	Delta	DD	Delta	DS/DD	Delta	Current SPC	OTC_AVG CL_WD	In/Out	DS
ECT306Z	106.68	In	Pass	12.5	Pass	-13.2	Pass	-10.9	P	3.04	In	Pass
ECT420Z	75.38	In	Pass	30.9	Pass	26.0	Pass	-15.7	-	2.36	In	Fail T-Tes
ECT452Z	86.11	Out	Pass	-1.2	Pass	-6.3	Fail T-Test	-23.9	P	2.19	In	Pass
ECT564Z	80.72	In	Pass	27.6	Pass	25.1	Pass	-15.2	F	2.86	In	Pass
ECTS03Z	52.94	Out	Pass	30.3	Pass	-1.0	Pass	-13.2	P	3.43	In	Pass
ECTS14Z	54.77	Out	Pass	8.9	Pass	-26.7	Pass	-15.6	P	3.04	In	Pass
ECTS1FZ	80.25	Out	Pass	4.2	Pass	-23.6	Pass	-14.5	P	3.26	In	Pass
ECTS2AZ	74.34	Out	Pass	-20.7	Fail T-Test	-41.7	Fail T-Test	-19.3	F	3.13	In	Fail T-Tes
ECTS36Z	69.71	Out	Pass	-15.1	Pass	-29.4	Fail T-Test	-15.7	-	3.05	In	Fail varien
ECTS43Z	62.36	Out	Pass	-17.9	Pass	-48.4	Fail T-Test	-19.4	F	2.86	In	Pass
ECTS5CZ	105.80	In	Pass	1.5	Pass	-12.0	Pass	-9.0	P	2.32	In	Pass
ECTS5DZ	66.22	Out	Pass	-29.8	Fail T-Test	-54.7	Fail T-Test	-25.2	-	2.98	In	Pass
ECTS60Z	144.26	Out	Fail T-Test	-49.4	Fail T-Test	-62.9	Fail T-Test	-18.5	P	2.02	In	Pass
ECTS8BZ	64.79	In	Pass	32.1	Pass	8.8	Pass	-15.3	P	3.07	In	Pass
ECTS9EZ	77.16	In	Pass	-4.7	Pass	-2.4	Pass	-16.9	F	2.76	In	Pass
ECTSA2Z	90.03	In	Pass	-8.6	Pass	-30.8	Fail T-Test	-20.7	P	2.33	In	Pass
ECTSB1Z	74.29	In	Pass	33.4	Pass	-3.4	Fail T-Test	-15.4	P	2.83	In	Pass
ECTSE3Z	59.20	Out	Pass	0.1	Pass	-38.2	Pass	-13.5	-	2.59	In	Pass
ECTSFFZ	60.24	Out	Pass	10.7	Pass	-4.8	Fail T-Test	-21.2	P	2.04	In	Pass

Figure 4.11: Report all tester page

In addition, the differences in mean and in yield of two samples are also shown as "*delta*" which were calculated and gathered for all testers based on same wafer quads found when compared to SD, DS, and DD. Delta in mean shows how much the mean difference between two interested samples. The tester that shows the more difference will be focused first. As well as delta in mean, delta in yield tells that the tester that has much difference in yield between two samples should be investigated. It is expected that the shifts in yield or mean that cause significant difference might cause from the tester performance if the process changes are already verified. Moreover, this page also provides the control limit width of each tester at the specified parameter. The control limit width should be observed to see how they vary from tester to tester based on variation of wafer tested. The testers that have large control limits will be focused. They should be monitored and understood why control limits on some testers are too large. It would be useful in analysing when the root causes are investigated.

When the hypothesis testing result shows significant difference when comparing own tester to SD, DS, and DD, that tester should be investigated for the root causes. However, all testers obtained such a result cannot be examined at all because limited time and effort. Therefore, the priority in implementing should be arranged. The testers that are out of control and provide significant difference on SD, DS, or DD should be investigated first. Then, the next priorities are in control but significant difference. However, the testers that are out of control and provide significant difference are much more than expected. Thus, the tester that has more yield impact will be focused. Yield has affected to the company's benefits because it refers to the number of passed products that would be shipped to the customers. The tester that has a big change in yield should be taken first, especially when the yield of the interested tester reduces. Delta yield, the difference in yield of two samples based on same wafer quads, is the factor in prioritising the urgency of the testers that need to be investigated. *Delta yield graph* (Figure 4.12), which is a part of *report all tester page,* is useful in identifying which tester should be investigated first. This graph also shows the hypothesis testing results based on same wafer quads of a selected product at the specified parameter when comparing to SD, DS, and DD. The points on the graph shows the delta on each tester by ordering based on delta differences so that it is the easy way to observe which testers should be firstly focused.

If yield impact, defined by delta in yield, is big enough and causes significant difference between own tester and SD, DS, or DD (red and green points in Figure 4.12), the tester will be basically examined for the simple things first such as factoring process, media change, re-calibration process, hardware change, and so on. After that, if the root causes are still not recovered, the tester will be further investigated for the other root causes by following the tester troubleshooting guide in Appendix F.

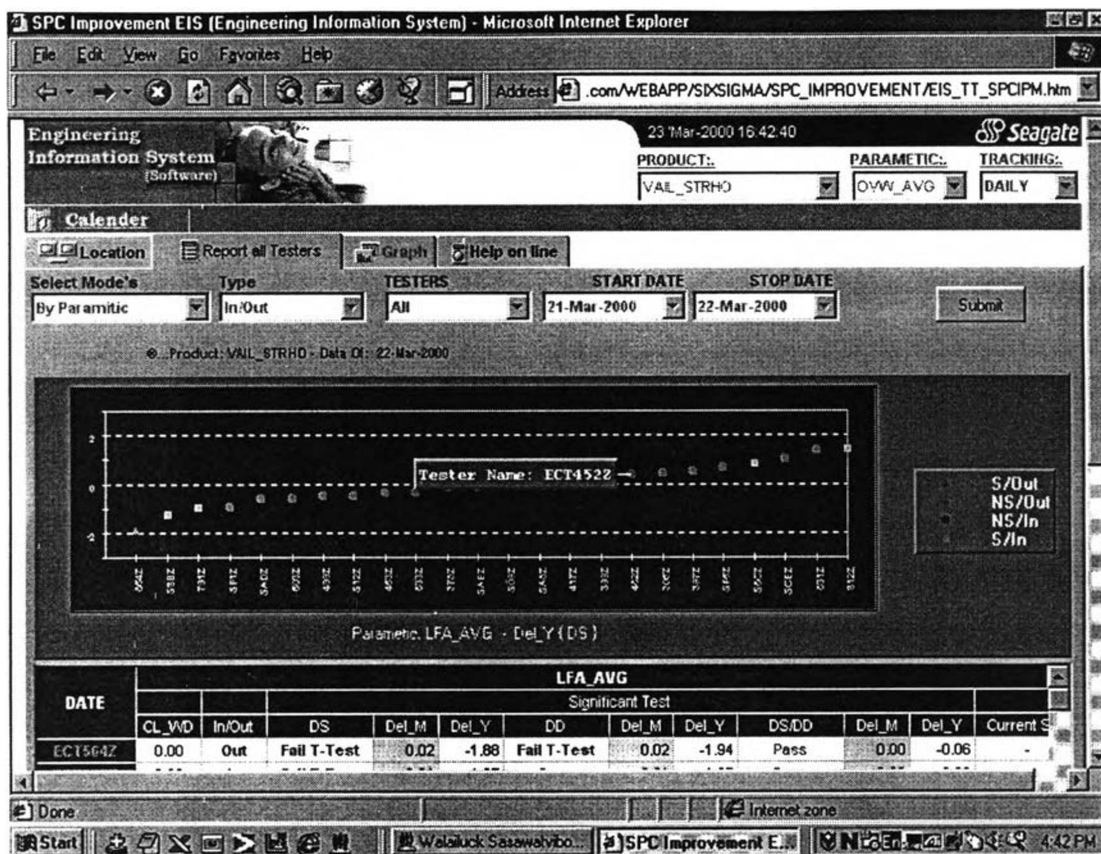


Figure 4.12: Delta yield graph

The preliminary procedure to find out for root causes of tester problems is implemented as following.

- ➔ Factoring result is investigated whether the trend of factoring corresponds to the mean shift. If it corresponds in the same way and offset of factoring shift is in same amount of the mean shift, it can be concluded that the shift is from factoring process that root causes might be factoring part degradation or new lot of factoring parts coming. If the shift is from factoring process and results in lower or higher yield, the tester should be re-calibrated for factoring process or the factoring parts might be changed as appropriate.
- ➔ Tester has to be investigated whether new lot of media is used. If the shift is from new media lot that causing negative impact or lower yield, the new lot has to be replaced.
- ➔ Re-calibration of preventive maintenance group is investigated whether there is re-calibration on that period and whether the root cause is from re-calibration. The possibility that root cause is from re-calibration is examined and verified with

preventive maintenance group. If it is from re-calibration and causes negative effect, the tester should be taken the corrective action.

→ Downtime report is investigated for the hardware changed or replaced in that period of time. If there is a change or replacement of any hardware, it has to be confirmed that the change of that part is real related to the parameter that has been monitored. If the shift is from hardware change and resulting in lower yield, investigation or new replacement should be taken by the responded person.

Since this system that provides the methodology to monitor tester performance used instead of current TSPC is complicated, Figure 4.13 illustrates the steps to follow when using this system. However, experienced engineers might not follow these steps. They can immediately look at *report all tester page* that is the summary page to verify tester performance and other pages for more information.

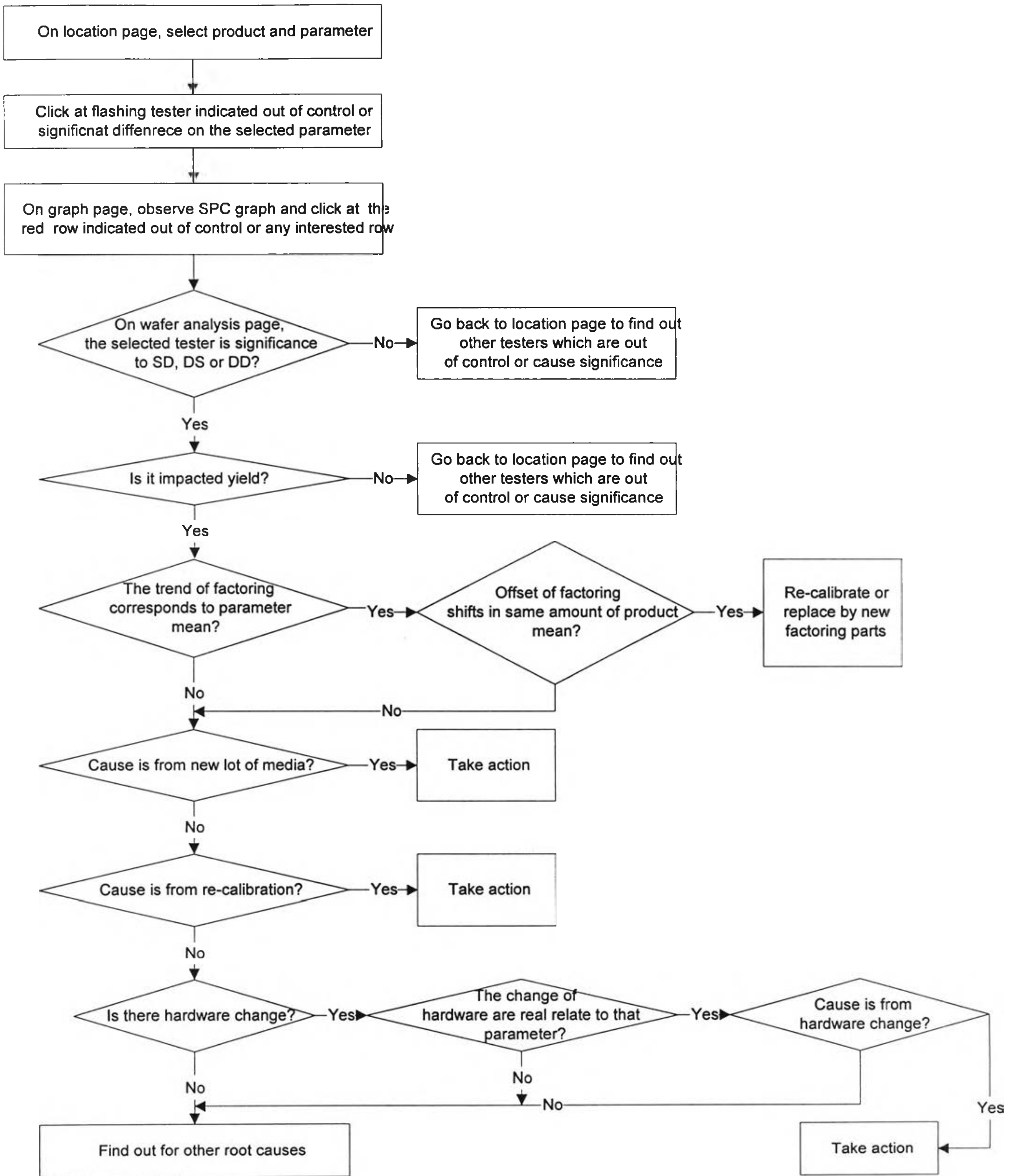


Figure 4.13: Flow diagram of new methodology to monitor tester performance

This new system provides many benefits to the company. The hypothesis testing results are expected to indicate tester performance. When T-test fails, that mean of own tester is significant difference to other testers based on same wafer quad comparison, the cause of that event is likely to come from tester performance if it is not from the process change. However, the results of hypothesis testing will give some ideas if the shift is from process change. The significant difference results might occur on every tester that tests the parts from same assembly line. The process change can also be verified by comparison between DS and DD based on same wafer quad comparison if that change has impact on all assembly lines that produce the same product. If the result of comparison of DS against DD gives significant difference, it means that the process might be changed or the process is not stable over time. As a result, the hypothesis testing results of own tester and SD or DD are not qualified except for DS which does not depend on time.

In conclusion, to increase effectiveness, skills of engineers are necessary when they make the investigation. Furthermore, other information such as control limit width, sample size of qualified wafer quads, delta mean, delta yield, sigma, and so forth should be considered to used as information in making decision about tester problems.

Out of control gives the important information about wafer performance, process, and tester. These are the major causes of out of control events. When tester is out of control and gets significant difference result, the root cause is expected to come from tester performance or process change. After the process change is verified by examining the hypothesis testing result between DS and DD or other testers that test the parts from same assembly line, the cause of shift happened is expected to come from tester problems.

On the other hand, if the tester is out of control but no significant difference when comparing to other testers at same wafer quads, the cause of out of control is likely to be from wafer performance. Hence, SPC can provide the ideas about wafer performance. Out of control might causes from the change in wafer performance that may be from new wafer lot. Therefore, the good or poor wafer lot can then be observed.

Another case is the tester that is in control but gives the significance result. Since comparing at same wafer quads provides the information about tester performance, the tester that has problems is expected to show the significant difference results on either SD, DS, or DD. However, the manufacturing tested data plotted on control chart may be still in control because of some quads that are not coincided to other testers contribute the great impacts more than the qualified quads. As a result, the means of manufacturing tested data does not shift. The tester faced this case needs investigation for tester problem although SPC is in control. The means of two populations are shifted based on same wafer quads which is expected that tester problems cause the shift of same wafer quad performance.

Delta in yield is a factor in making the decision which tester should be investigated first. The tester that has much yield impact should be focused before the others. From the delta yield graph in Figure 4.12, it can be observed that the tester that got large delta in yield usually provides significant difference as comparing to other testers. It can be concluded that size of delta is often related to the tester performance.

The new system is created to monitor tester performance. In addition, it is useful in indicating wafer performance and process analysis. It provides a lot of information that would be useful for the company's production. From information of the system, it should be carefully studied and evaluated to reach the objective of the system that is monitoring tester performance.

4.5 Control Phase

The new methodology in monitoring tester performance is developed. The system is shown on the company internal webside to be convenient in monitoring so that everyone in the company can see it. However, the person who has direct responsibility is Tester Control division. They have to observe the tester performance everyday.

SPC is shown on the new system as on the *graph page* (Figure 4.9). Engineers can make analysis from control charts and other available data such as hypothesis testing results based on same wafer quad relation. The improvement after finding out root causes

and taking corrective action can be seen on the trend of SPC. The special causes are tried to be eliminated. Fixing tester problems is one way to reduce variation and keep SPC stable over time if the cause of variation is from the tester problems.

To control tester performance, when root causes are found, they have to be eliminated. Hence, testers and production process have been optimised. Follow up is necessary to observe what is going on after the testers are taken corrective action or fixed. Currently, the testers that are fixed will be followed up for a week to know their performance. It is essential to speed up the feedback of data and information to improve process quicker with minimised loss.

Furthermore, the process flow has to be reviewed and updated periodically. Likewise, the system can be modified as appropriate when there are better alternatives. When any improvements are added, the related issues should be concerned and modified. The training is always provided and updated for engineers who are responsible and other related personals. For the beginning period of implementation, the meetings are often taken to acknowledge employees including management levels to accustom them to the new methodology and find out the problems that might be taken place from this new methodology. Moreover, all documentation related should be collected. Weekly reports are prepared to know the progress of the project.

For the test operation, appropriate work standards are prepared for operators to increase repeatability and reproducibility. The responsible for test operation should be thoroughly trained, and methods of controlling measurement process are devised. In addition, work standards for cleaning, maintenance, and calibration should be prepared to reduce problems going to occur from tester problems.

To optimise effectiveness in detecting tester performance, causes of ineffectiveness of this methodology has to be concerned and periodically reviewed. It can be done by using cause and effect diagram, Failure Mode and Effect Analysis (FMEA), Pareto diagram, and so on. Then, root causes could be eliminated so that the effectiveness in detecting the tester performance is improved.

Control plan can be used to ensure for consistently operating to achieve the objective. It could be summarised as in Table 4.4.

Table 4.4: Control plan

Characteristics	Specification	Measurement Method	Frequency	Re-action plan	Who Measured	Where Recorded
Technician / Engineer understanding	Understanding in monitoring process	Examination	Monthly	Re-train	Tester control	Paper
Effectiveness	More than 30% effectiveness	Corrective action report	Weekly	Review tester monitoring process and system	Tester control	Weekly report
Saving from yield improved		Saving calculation	Weekly		Tester control	Weekly report
Results of corrective actions	Yield improved	Follow-up	One week after actions	Take other actions	Tester Control	Corrective action report

4.6 Conclusion

New process of monitoring tester performance is using continuous manufacturing tested data. Same wafer quad relation is used as the basis in detecting the shift of wafer quad performance to monitor tester performance.

Measurement phase identifies the problems of current tester monitoring process, TSPC. Main cause is from TSPC part degradation resulting in part repeatability. From this problem, it results in effectiveness of TSPC low as 30%. Thus, new source of data used instead of three part data is from testing operation that is continuous tested data from testing production parts. Benefits of this data is approved by analysis phase that develop same wafer quad relation used as the basis of new process of monitoring tester performance. It is recognised that parts from same wafer quad do not have significant difference in performance. Hence, the shift occurred in means of same wafer quad comparison is expected to be from tester problems, despite of process change that is

seldom occurred. Then, in improvement phase the system which is useful in indicating tester performance is developed based on this analysis. SPC plotted by manufacturing tested data is used for monitoring process. From out of control point, the shift can be detect by hypothesis testing based on same wafer quad that compares the interested tester to its own at different time, other testers at same time, and other testers at different time. If the shift results in significant difference in means of two populations, tester has to be investigated. However, other information such as control limit width, sample size of qualified wafer quads, delta mean, delta yield, sigma, and so forth of the interested tester should be considered to used as information in investigating tester performance. Moreover, in control phase the system and process of monitoring tester should be periodically reviewed to optimise its effectiveness. Training, meeting, following up, control plan and so on are conducted to achieve the intended objective.