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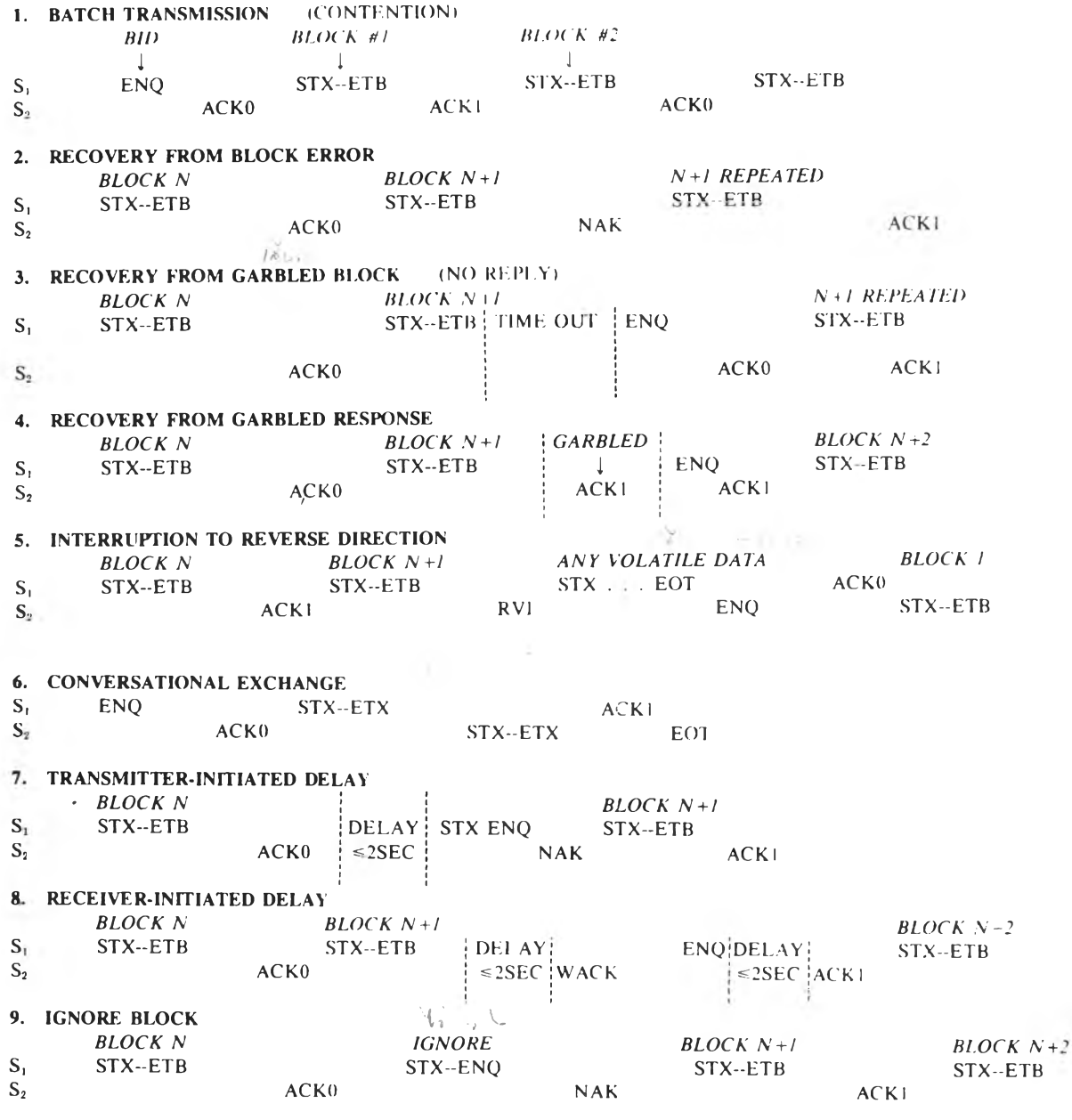
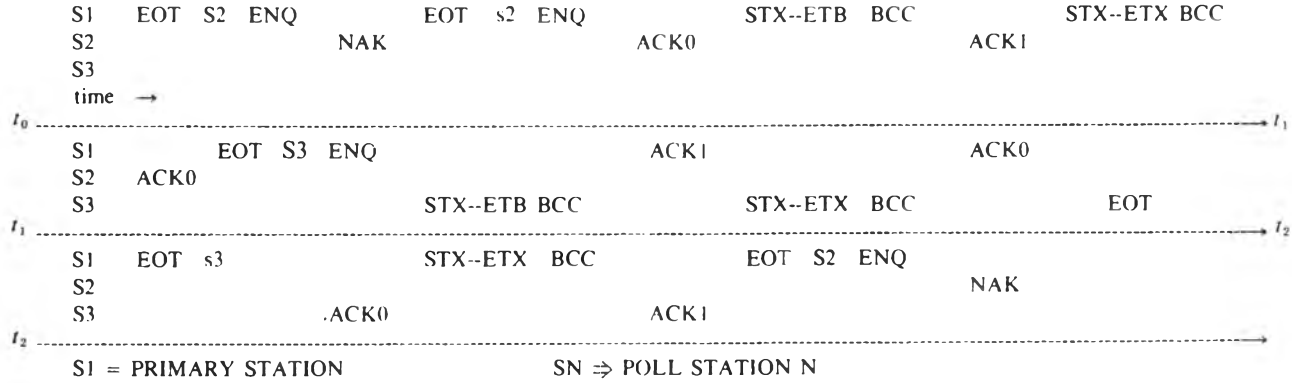
ภาคผนวก ก.



รูปแสดงการโต้ตอบของไบนารี่ซิงค์ แบบจุดต่อจุด



รูปตัวอย่างการโต้ตอบของโพลลิ่ง แบบหลายจุดต่อ

Data Transmission Configuration	Interface Type
Transmit only	A
Transmit only	B
Receive only	C
Half-duplex	D
Duplex	D
Duplex	E
Primary channel transmit only/secondary channel receive only	F
Primary channel transmit only/secondary channel receive only	H
Primary channel receive only/secondary channel transmit only	G
Primary channel receive only/secondary channel transmit only	I
Primary channel transmit only/half-duplex secondary channel	J
Primary channel receive only/half-duplex secondary channel	K
Half-duplex primary channel/half-duplex secondary channel	L
Duplex primary channel/duplex secondary channel	L
Duplex primary channel/duplex secondary channel	M

รูปแสดงระบบการส่งของอีไอเออินเทอร์เฟสที่ทำได้

รูปการางแสดงขาสัญญาณที่ต้องใช้ในแบบอินเทอร์เฟสต่าง ๆ

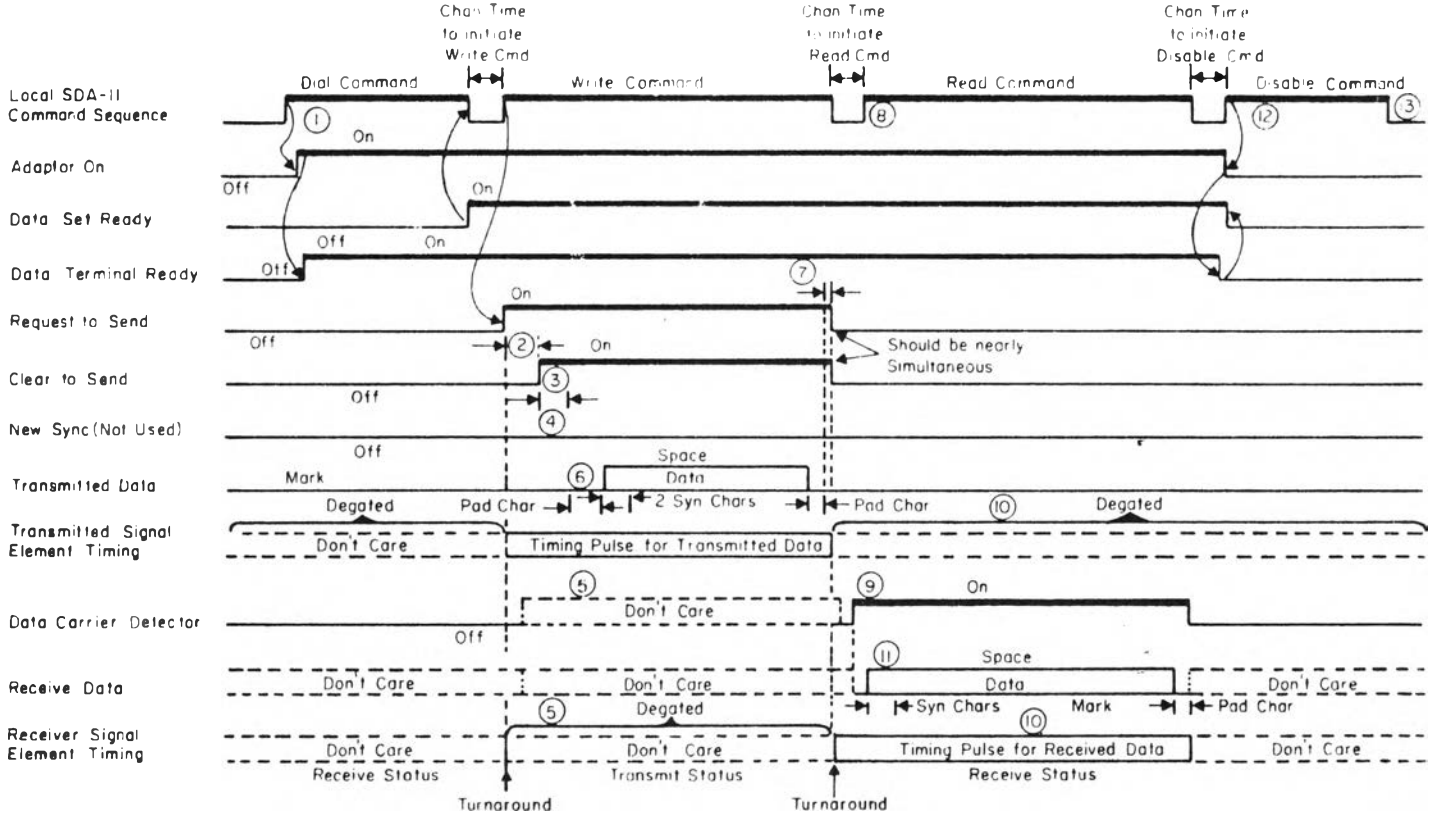
	Interchange Circuit	Interface Type												
		A	B	C	D	E	F	G	H	I	J	K	L	M
AA	Protective ground	—	—	—	—	—	—	—	—	—	—	—	—	—
AB	Signal ground	x	x	x	x	x	x	x	x	x	x	x	x	x
BA	Transmitted data	x	x		x	x	x		x		x		x	x
BB	Received data			x	x	x		x		x		x	x	x
CA	Request to send		x		x		x				x		x	
CB	Clear to send	x	x		x	x	x		x		x			
CC	Data set ready	x	x	x	x	x	x	x	x	x	x	x	x	x
CD	Data terminal ready	s	s	s	s	s	s	s	s	s	s	s	s	s
CE	Ring indicator	s	s	s	s	s	s	s	s	s	s	s	s	s
CF	Received line signal detector			x	x	x		x		x		x	x	x
CG	Signal quality detector													
CH/CI	Data signaling rate selector (DTE)/(DCE)													
DA/DB	Transmitter signal element timing (DTE)/(DCE)	t	t		t	t	t		t		t	t	t	t
DD	Receiver signal element timing (DCE)			t	t	t		t		t		t	t	t
SBA	Secondary transmitted data							x		x	x	x	x	x
SBB	Secondary received data						x		x		x	x	x	x
SCA	Secondary request to send							x			x	x	x	
SCB	Secondary clear to send							x		x	x	x	x	x
SCF	Secondary received line signal detector						x		x		x	x	x	x

[a]s: additional interchange circuits required for switched service; t: additional interchange circuits required for synchronous channel; x: basic interchange circuits, all systems; —: optional.

รูปตารางจัดกลุ่มหน้าที่ของสัญญาณ อีไอเอ

EIA Pin Number	Inter-change Circuit	C.C.I.T.T. Equiv-alent	Description (DCE: Data Communications Equipment. DTE: Data Terminal Equipment)	Ground	Data		Control		Timing	
					From DCE	To DCE	From DCE	To DCE	From DCE	To DCE
1	AA	101	Protective ground	X						
7	AB	102	Signal ground/common return	X						
2	BA	103	Transmitted data			X				
3	BB	104	Received data		X					
4	CA	105	Request to send					X		
5	CB	106	Clear to send				X			
6	CC	107	Data set ready				X			
20	CD	108	Data terminal ready					X		
22	CE	125	Ring indicator				X			
8	CF	109	Received line signal detector				X			
21	CG	110	Signal quality detector				X			
23	CH	111	Data signal rate selector (DTE—driver)					X		
23	CI	112	Data signal rate selector (DCE—driver				X			
24	DA	113	Transmitter signal element timing (DTE)							X
15	DB	114	Transmitter signal element timing (DCE)						X	
17	DD	115	Receiver signal element timing (DCE)						X	
14	SBA	118	Secondary transmitted data			X				
16	SBB	119	Secondary received data		X					
19	SCA	120	Secondary request to send					X		
13	SCB	121	Secondary clear to send				X			
12	SCF	122	Secondary received line signal detector				X			

รูปตารางเวลาทำงานของอินเทอร์เฟส



Bit Positions 1,2,3,4	Bit Positions 5,6,7							
	000	100	010	110	001	101	011	111
0 0 0 0	NUL	DLE	SPACE	0	@	P		p
1 0 0 0	SOH	DC1	!	1	A	Q	a	q
0 1 0 0	STX	DC2	"	2	B	R	b	r
1 1 0 0	ETX	DC3	#	3	C	S	c	s
0 0 1 0	EOT	DC4	$	4	D	T	d	t
1 0 1 0	ENQ	NAK	%	5	E	U	e	u
0 1 1 0	ACK	SYN	&	6	F	V	f	v
1 1 1 0	BEL	ETB	'	7	G	W	g	w
0 0 0 1	BS	CAN	(	8	H	X	h	x
1 0 0 1	HT	EM	)	9	I	Y	i	y
0 1 0 1	LF	SUB	*	:	J	Z	j	z
1 1 0 1	VT	ESC	+	;	K	[	k	{
0 0 1 1	FF	FS	,	<	L	\	l	|
1 0 1 1	CR	GS	-	=	M	]	m	}
0 1 1 1	SO	RS	.	>	N	^	n	~
1 1 1 1	SI	US	/	?	O	-	o	DEL

NUL = All zeroes
SOH = Start of header
STX = Start of text
ETX = End of text
EOT = End of transmission
ENQ = Inquiry
ACK = Acknowledgement
BEL = Bell
BS = Back space
HT = Horizontal tab
LF = Line feed
VT = Vertical tab
FF = Form feed
CR = Carriage return
SO = Shift out
SI = Shift in
DLE = Data link escape

DC1 = Device control #1
DC2 = Device control #2
DC3 = Device control #3
DC4 = Device control #4
NAK = Negative acknowledgement
SYN = Synchronous idle
ETB = End transmitted block
CAN = Cancel
EM = End of medium
SUB = Start special sequence
ESC = Escape or break
FS = File separator
GS = Group separator
RS = Record separator
US = Unit separator
DEL = Delete

ตารางรหัส ASCII

SILICON GATE MOS 8080A

INSTRUCTION SET

Summary of Processor Instructions

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
$MOV_{r1,r2}$	Move register to register	0	1	D	D	D	S	S	S	5
MOV M r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r, M	Move memory to register	0	1	D	D	D	1	1	0	7
HLT	Halt	0	1	1	1	0	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
INR r	Increment register	0	0	D	D	D	1	0	0	5
DCR r	Decrement register	0	0	D	D	D	1	0	1	5
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10
JZ	Jump on zero	1	1	0	0	1	0	1	0	10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10
JP	Jump on positive	1	1	1	1	0	0	1	0	10
JM	Jump on minus	1	1	1	1	1	0	1	0	10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
CALL	Call unconditional	1	1	0	0	1	1	0	1	17
CC	Call on carry	1	1	0	1	1	1	0	0	11/17
CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17
CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
CP	Call on positive	1	1	1	1	0	1	0	0	11/17
CM	Call on minus	1	1	1	1	1	1	0	0	11/17
CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	5/11
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
RP	Return on positive	1	1	1	1	0	0	0	0	5/11
RM	Return on minus	1	1	1	1	1	0	0	0	5/11
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
RST	Restart	1	1	A	A	A	1	1	1	11
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	11
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	11
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	11
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	11
POP B	Pop register pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	18
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
EI	Enable Interrupts	1	1	1	1	1	0	1	1	4
DI	Disable interrupt	1	1	1	1	0	0	1	1	4
NOP	No operation	0	0	0	0	0	0	0	0	4

NOTES 1. DDD or SSS – 000 B – 001 C – 010 D – 011 E – 100 H – 101 L – 110 Memory – 111 A.
2. Two possible cycle times, (5/11) indicate instruction cycles dependent on condition flags.

ภาคผนวก ข.

โปรแกรมควบคุมลำดับการทำงานของซีอาร์ทีเทอร์มินอล

```
                        ;
                        ;       MONITOR  CRT  PROGRAM
                        ;         5  SEPTEMBER  1980
                        ;
0000                            ORG     0
0000 3E8A               .       MVI     A,8AH
0002 D360                       OUT     ME3
0004 210004                     LXI     H,0400H
0007 31FF0B                     LXI     SP,STACK
000A C33300                     JMP     INA75
0030                            ORG     30H
0030 C3FA01                     JMP     INTSUM
                        ;
                        ;       INITIAL ROUTINE  "8275 CRT"
                        ;
0033 3E00               INA75   MVI     A,00H
0035 D391                       OUT     SUC
0037 3EBF                       MVI     A,0BFH
0039 D390                       OUT     SUP
003B 3E8F                       MVI     A,8FH
003D D390                       OUT     SUP
003F 3E77                       MVI     A,77H
0041 D390                       OUT     SUP
0043 3E09                       MVI     A,09H
0045 D390                       OUT     SUP
0047 3EA0                       MVI     A,0A0H
0049 D391                       OUT     SUC
004B 3E2F                       MVI     A,2FH
004D D391                       OUT     SUC
                        ;
                        ;       POWER  UP
                        ;       CLEAR MEMORY & HOME CURSOR
                        ;
004F 3E20               LOPP    MVI     A,20H
0051 77                         MOV     M,A
0052 7C                         MOV     A,H
0053 FE0B                       CPI     0BH
0055 CA5C00                     JZ      CMMHP
0058 23                 CMMLP   INX     H
0059 C34F00                     JMP     LOPP
005C 7D                 CMMHP   MOV     A,L
005D FEFF                       CPI     0FFH
005F CA6500                     JZ      CHOM1
0062 C35800                     JMP     CMMLP
0065 210004             CHOM1   LXI     H,0400H
0068 010000                     LXI     B,0000H
```

```
                        ;
                        ;       INITIALIZE INTERFACE
                        ;
006B D3F4       PINIT   OUT     PREST
006D D3F5               OUT     PBOUD
006F DBF4               IN      PREG2
0071 E608               ANI     08H
0073 CA7B00             JZ      HALFD
0076 3E04               MVI     A,04H
0078 C37D00             JMP     SFLAG
007B 3E06       HALFD   MVI     A,06H
007D D3F6       SFLAG   OUT     PREG3
007F FB                 EI
                        ;
                        ;       MONITOR  START
                        ;
0080 CD7602     INPUT   CALL    PIST
0083 CDED00             CALL    INKEY
0086 FE0F       PCHK    CPI     0FH
0088 CA8000             JZ      INPUT
008B FE03               CPI     03H     ; CURSOR RIGHT
008D CAC300             JZ      CRT
0090 FE17               CPI     17H     ; CURSOR  LEFT
0092 CAC900             JZ      CLEF
0095 FE04               CPI     04H     ; CLEAR MOMERY
0097 CACF00             JZ      CLR
009A FE18               CPI     18H     ; HOME
009C CAD500             JZ      CHOM
009F FE02               CPI     02H     ; CURSOR DOWN
00A1 CADB00             JZ      CROLD
00A4 FE01               CPI     01H     ; CURSOR UP
00A6 CAE100             JZ      CUP
00A9 FE08               CPI     08H     ; ENTER
00AB CAE700             JZ      ENT
00AE CD1E02             CALL    PSEND
00B1 DBF4               IN      PREG2
00B3 E608               ANI     08H     ;FULL  DUPLEX
00B5 C28000             JNZ     INPUT
00B8 77                 MOV     M,A     ; DATA KB TO MM
00B9 D300               OUT     ME0
00BB CD4901             CALL    CRITE
00BE D3F4               OUT     PREST
00C0 C38000             JMP     INPUT
                        ;
                        ;       CALL SUBROUTINE
                        ;
00C3 CD4901     CRT     CALL    CRITE
00C6 C38000             JMP     INPUT
```

```
                                ;
00C9 CD2001     CLEF    CALL    CLEFT
00CC C38000             JMP     INPUT
                                ;
00CF CDAA01     CLR     CALL    CLEAR
00D2 C38000             JMP     INPUT
                                ;
00D5 CDFC00     CHOM    CALL    HOME
00D8 C38000             JMP     INPUT
                                ;
00DB CD7501     CROLD   CALL    RDOWN
00DE C38000             JMP     INPUT
                                ;
00E1 CD0301     CUP     CALL    CURUP
00E4 C38000             JMP     INPUT
                                ;
00E7 CDCA01     ENT     CALL    ENTER
00EA C38000             JMP     INPUT
                                ;
                                ;
                                ;       INKEY
                                ;
00ED DB20       INKEY   IN      ME1
00EF B7                 ORA     A
00F0 F2ED00     LOPKB   JP      INKEY
00F3 DB20               IN      ME1
00F5 B7                 ORA     A
00F6 FAF000             JM      LOPKB
00F9 DB20               IN      ME1
00FB C9                 RET
                                ;
                                ;       HOME
                                ;
00FC 010000     HOME    LXI     B,0000H
00FF 210004             LXI     H,0400H
0102 C9                 RET
                                ;
                                ;       CURSOR  UP
                                ;
0103 114000     CURUP   LXI     D,0040H
0106 3E00               MVI     A,B
0108 FE00               CPI     00H
010A CA1701             JZ      UPCR
010D 05                 DCR     B
010E 7D                 MOV     A,L
010F 9B                 SBB     E
0110 6F                 MOV     L,A
0111 7C                 MOV     A,H
```

```
0112 9A                 SBB     D
0113 67                 MOV     H,A
0114 C31F01             JMP     UPRET
0117 21C007     UPCR    LXI     H,07C0H
011A 79                 MOV     A,C
011B 85                 ADD     L
011C 6F                 MOV     L,A
011D 060F               MVI     B,0FH
011F C9         UPRET   RET
                        ;
                        ;       CURSOR  LEFT
                        ;
0120 78         CLEFT   MOV     A,B
0121 FE00               CPI     0CH
0123 CA3101             JZ      CTEST
0126 79                 MOV     A,C
0127 FE00               CPI     0CH
0129 CA4401             JZ      CBCR
012C 0D         CDCR    DCR     C
012D 2B                 DCX     H
012E C34801             JMP     CLRET
0131 79         CTEST   MOV     A,C
0132 FE00               CPI     00H
0134 CA3A01             JZ      CBEGIN
0137 C32C01             JMP     CDCR
013A C60F       CBEGIN  MVI     B,0FH
013C 0E3F               MVI     C,3FH
013E 21FF07             LXI     H,07FFH
0141 C34801             JMP     CLRET
0144 05         CBCR    DCR     B
0145 0E3F               MVI     C,3FH
0147 2B                 DCX     H
0148 C9         CLRET   RET
                        ;
                        ;       MOVE  CURSOR  RIGHT
                        ;
0149 78         CRITE   MOV     A,B
014A FE0F               CPI     0FH
014C CA5A01             JZ      CREND
014F 79                 MOV     A,C
0150 FE3F               CPI     3FH
0152 CA6301             JZ      CRINR
0155 0C         CRNEXT  INR     C
0156 23                 INX     H
0157 C37401             JMP     CRRET
015A 79         CREND   MOV     A,C
015B FE3F               CPI     3FH
015D CA6A01             JZ      CRLRP
```

```
0160 C35501              JMP       CRNEXT
0163 23          CRINR   INX       H
0164 04                  INR       B
0165 0E00                MVI       C,00H
0167 C37401              JMP       CRRET
016A CD9401      CRLRP   CALL      ROLLUP
016D 060F                MVI       B,0FH
016F 0E00                MVI       C,00H
0171 21C007              LXI       H,07C0H
0174 C9          CRRET   RET

                 ;
                 ;       CURSOR    DOWN
                 ;
0175 114000      RDOWN   LXI       D,0040H
0178 78                  MOV       A,B
0179 FE0F                CPI       0FH
017B CA8601              JZ        ROBIN
017E C4                  INR       B
017F 7D                  MOV       A,L
0180 83                  ADD       E
0181 6F                  MOV       L,A
0182 7C                  MOV       A,H
0183 8A                  ADC       D
0184 67                  MOV       H,A
0185 C9          DORET   RET
0186 CD9401      ROBIN   CALL      ROLLUP
0189 21C007              LXI       H,07C0H
018C 79                  MOV       A,C
018D 85                  ADD       L
018E 6F                  MOV       L,A
018F 060F                MVI       B,0FH
0191 C38501              JMP       DORET
                 ;
                 ;       SCROLL    MODE
                 ;
0194 214004      ROLLUP  LXI       H,0440H
0197 110004              LXI       D,0400H

019A 7C          LOPUP   MOV       A,H
019B FE0B                CPI       0BH
019D CAA901              JZ        LOPRET
01A0 7E                  MOV       A,M
01A1 EB                  XCHG
01A2 77                  MOV       M,A
01A3 23                  INX       H
01A4 13                  INX       D
```

```
01A5 EB                 XCHG
01A6 C39A01             JMP       LOPUP
01A9 C9         LOPRET  RET
                ;
                ;       CLEAR  MEMORY
                ;
01AA 210004     CLEAR   LXI       H,0400H
01AD 3E20       LOP     MVI       A,20H
01AF 77                 MOV       M,A
01B0 7C                 MOV       A,H
01B1 FE0B               CPI       0BH

01B3 CABA01     CMML    JZ        CMMH
01B6 23                 INX       H
01B7 C3AB01             JMP       LOP
01BA 7D         CMMH    MOV       A,L
01BB FEFF               CPI       0FFH
01BD CAC301             JZ        BEGIN
01C0 C3B301             JMP       CMML
01C3 210004     BEGIN   LXI       H,0400H
01C6 010000             LXI       B,0000H
01C9 C9                 RET
                ;
                ;       ENTER
                ;
01CA 7D         ENTER   MOV       A,L
01CB 91                 SUB       C
01CC 6F                 MOV       L,A
01CD 0E00               MVI       C,00H
01CF C9                 RET
01D0 FE0D       PCHA    CPI       0DH
01D2 C2DB01             JNZ       PLF
01D5 CDFC00             CALL      HOME
01D8 C3F901             JMP       PRRT
01DB FE0A       PLF     CPI       0AH
01DD C2EA01             JNZ       PBS
01E0 CDFC00             CALL      HOME
01E3 00                 NOP
01E4 CD7301             CALL      RDOWN
01E7 C3F901             JMP       PRRT
01EA FE08       PBS     CPI       08H
01EC C2F501             JNZ       PSAVE
01EF CD2001             CALL      CLEFT
01F2 C3F901             JMP       PRRT
01F5 77         PSAVE   MOV       M,A
01F6 CD4701             CALL      CRITE
01F9 C9         PRRT    RET
```

```
                        ;
                        ;       INTERRUPT  ROUTINE  "INITIAL  8257  DMA"
                        ;
01FA F5         INTSUM  PUSH    PSW
01FB DB91               IN      SUC
01FD 3E00               MVI     A,00H
01FF D380               OUT     SUA
0201 3E04               MVI     A,04H
0203 D380               OUT     SUA
0205 3E00               MVI     A,00H
0207 D381               OUT     SUT
0209 3E84               MVI     A,84H
020B D381               OUT     SUT
020D 3E41               MVI     A,41H
020F D388               OUT     SUS
0211 3E80               MVI     A,80H
0213 D391               OUT     SUC
0215 79                 MOV     A,C
0216 D390               OUT     SUP
0218 78                 MOV     A,B
0219 D390               OUT     SUP
021B F1                 POP     PSW
021C FB                 EI
021D C9                 RET

                        ;
                        ;       SEND CHARACTER
                        ;
021E F5         PSEND   PUSH    PSW
021F DBF4               IN      PREG2
0221 E608               ANI     08H
0223 C23702             JNZ     PPOUT
0226 3E04               MVI     A,04H
0228 D3F6               OUT     PREG3
022A DBF4               IN      PREG2
022C E640               ANI     40H
022E CA3702             JZ      PPOUT
0231 DBF4       PCTS    IN      PREG2
0233 17                 RAL
0234 D23102             JNC     PCTS
0237 DBF6       PPOUT   IN      PREG1
0239 E604               ANI     04H
023B CA3702             JZ      PPOUT
023E F1                 POP     PSW
023F D3F7               OUT     POUTP
0241 F5                 PUSH    PSW
0242 DBF4               IN      PREG2
0244 E608               ANI     08H
```

```
0246 C25002             JNZ     RETN
0249 F1                 POP     PSW
024A FE0D               CPI     0DH
024C CA5202             JZ      HREST
024F C9                 RET
0250 F1         RETN    POP     PSW
0251 C9                 RET
0252 DBF5       HREST   IN      PEOC
0254 17                 RAL
0255 D25202             JNC     HREST
0258 D5                 PUSH    D
0259 1E50               MVI     E,50H
025B 1D         PLOOP   DCR     E
025C 00                 NOP
025D 00                 NOP
025E 00                 NOP
025F 00                 NOP
0260 00                 NOP
0261 00                 NOP
0262 00                 NOP
0263 00                 NOP
0264 00                 NOP
0265 00                 NOP
0266 00                 NOP
0267 00                 NOP
0268 00                 NOP
0269 00                 NOP
026A 00                 NOP
026B 00                 NOP
026C 00                 NOP
026D C25B02             JNZ     PLOOP
0270 D1                 POP     D
0271 3E06               MVI     A,06H
0273 D3F6               OUT     PREG3
0275 C9                 RET
                ;
                ;       RECEIVE  CHARACTER
                ;
0276 DBF6       PIST    IN      PREG1
0278 1F                 RAR
0279 D0                 RNC
027A DBF7       PIIN    IN      PINP
027C E67F               ANI     7FH
027E CD0C01             CALL    PCHA
0281 C37602             JMP     PIST
08FF =          STACK   EQU     08FFH
0000 =          ME0     EQU     00H
0020 =          ME1     EQU     20H
```

```
0060 =          ME3     EQU     60H
0091 =          SUC     EQU     91H
0090 =          SUP     EQU     90H
0080 =          SUA     EQU     80H
0081 =          SUT     EQU     81H
0088 =          SUS     EQU     88H
00F6 =          PREG1   EQU     0F6H
00F4 =          PREG2   EQU     0F4H
00F6 =          PRE03   EQU     0F6H
00F4 =          PREST   EQU     0F4H
00F5 =          PBOUD   EQU     0F5H
00F5 =          PEOC    EQU     0F5H
00F7 =          PINP    EQU     0F7H
00F7 =          POUTP   EQU     0F7H
0294                    END
```

ภาคผนวก ค.

รายละเอียดไอซีที่ใช้ในวงจรอินเทอร์เฟส

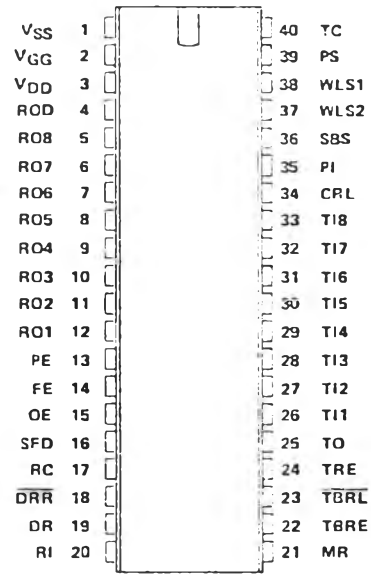
MOS
LSI

TMS 6011 JC, NC
ASYNCHRONOUS DATA INTERFACE (UART)

BULLETIN NO. DL-S 7512275, REVISED NOVEMBER 1977

- Transmits, Receives, and Formats Data
- Full-Duplex or Half-Duplex Operation
- Operation from DC to 200 kHz
- Static Logic
- Buffered Parallel Inputs and Outputs
- Programmable Word Lengths . . . 5, 6, 7, 8 Bits
- Programmable Information Rate
- Programmable Parity Generation/Verification
- Programmable Parity Inhibit
- Automatic Data Formatting
- Automatic Status Generation
- 3-State Push-Pull Buffers
- Low-Threshold Technology
- Standard Power Supplies . . . 5 V, −12 V
- Full TTL Compatibility . . . No External Components

40-PIN CERAMIC AND PLASTIC
DUAL-IN-LINE PACKAGES
(TOP VIEW)



description

The TMS 6011 JC, NC is an MOS/LSI subsystem designed to provide the data interface between a serial communications link and data processing equipment such as a peripheral or a computer. The device is often referred to as an asynchronous data interface or as a universal asynchronous receiver/transmitter (UART).

The receiver section of the TMS 6011 will accept serial data from the transmission line and convert it to parallel data. The serial word will have start, data, and stop bits. Parity may be generated and verified. The receiver section will validate the received data transmission by checking proper start, parity, and stop bits, and will convert the data to parallel.

The transmitter section will accept parallel data, convert it to serial form, and generate the start, parity, and stop bits.

The TMS 6011 is a fully programmable circuit allowing maximum flexibility of operation, defined as follows:

- The receiver and transmitter sections are separate and can operate either in full-duplex (simultaneous transmission and reception) or in half-duplex mode (alternate transmission and reception).
- The data word may be externally selected to be 5, 6, 7, or 8 bits long.
- Baud rate is externally selected by the clock frequency. Clock frequency can vary between 0 and 200 kHz.
- Parity, which is generated in the transmit mode and verified in the receive mode, can be selected as either odd or even. It is also possible to disable the parity bit by inhibiting the parity generation and verification.
- The stop bit can be selected as either a single- or a double-bit stop.
- Static logic is used to maximize flexibility of operation and to simplify the task of the user. The data holding registers are static and will hold a data word until it is replaced by another word.
- Asynchronous operation allows the use of a single transmission line. The clock period has to be within ±4% of 1/16 of the time for one bit for the transmitter and/or receiver but no phase relationship is required.

To allow for a wide range of possible configurations, three-state push-pull buffers have been used on all outputs except Transmitter Output (TO) and Transmitter Register Empty (TRE). They allow the wire-OR configuration.

TMS 6011 JC,NC
ASYNCHRONOUS DATA INTERFACE (UART)

description (continued)

The TMS 6011 can be used in a wide range of data handling equipment such as modems, peripherals, printers, data displays, and minicomputers. By taking full advantage of the latest MOS/LSI design and processing techniques, it has been possible to implement the entire transmit, receive, and format function necessary for digital data communication in a single package, avoiding the cumbersome circuitry previously necessary.

P-channel enhancement-type low-threshold technology permits the use of standard power supplies (5 V, −12 V) as well as direct TTL interface. No external components are needed.

The TMS 6011 is offered in both 40-pin dual-in-line ceramic (JC suffix) and plastic (NC suffix) packages designed for insertion in mounting-hole rows on 600-mil centers. The device is characterized for operation from −25°C to 85°C.

operation

The operation can be best understood by visualizing the TMS 6011 as three separate sections: 1) common control, 2) transmitter, and 3) receiver. The transmitter and receiver sections are independent while the control section directs both receive and transmit.

common control section

The common control section will direct both the receiver and the transmitter sections.

The initialization of the TMS 6011 is performed through the Master Reset (MR) terminal. The MR terminal is strobed to a high level after power turn-on to reset all status and transmitter registers and to reset Transmitter Output (TO) to a high level. The Receiver Outputs (RO1-RO8) are not controlled by the MR terminal.

Status flags Parity Error, Framing Error, Overrun Error, Data Ready, and Transmitter Buffer Register Empty are disabled when the Status Flags Disable (SFD) is at a high level. When disabled, the status flags float (three-state buffers are in the high-impedance state). The Transmitter Register Empty (TRE) status flag is not a three-state output.

The number of bits per word is controlled by the Word Length Select 1 (WLS1) and Word Length Select 2 (WLS2) inputs. The word length may be 5, 6, 7, or 8 bits. Selection is as follows:

WORD LENGTH	WLS1	WLS2
5	Low	Low
6	High	Low
7	Low	High
8	High	High

The parity to be checked by the receiver and generated by the transmitter is determined by the Parity Select (PS) input. A high level on the PS input selects even parity and a low level selects odd parity.

The parity will not be checked or generated if a high level is applied to Parity Inhibit (PI); in this case the stop bit or bits will immediately follow the data bit.

When a high level is applied to PI, the Parity Error (PE) status flag is brought to a low level indicating a no-parity error because parity is disregarded in this mode.

To select either one or two stop bits, the Stop Bit(s) Select (SBS) terminal is used. A high level at this terminal will result in two stop bits while a low level will produce only one.

To load the control bits (WLS1, WLS2, PS, PI, and SBS) a high level is applied to the Control Register Load (CRL) terminal. This terminal may be strobed or hard wired to a high level.

operation (continued)

transmitter section

The transmitter section will accept data in parallel form, then serialize, format, and transmit the data in serial form.

Parallel input data is received through the Transmitter Inputs (TI1-TI8).

Serial output data is transmitted from the Transmitter Output (TO) terminal.

Input data is stored in the transmitter-buffer register. A low level at the Transmitter Buffer Register Load ($\overline{\text{TBRL}}$) command terminal will load a word in the transmitter-buffer register. The length of this word is determined by Word Length Select 1 (WLS1) and Word Length Select 2 (WLS2). If a word of length greater than this appears at TI8 through TI1, only the least significant bits are accepted. The word is justified into the least significant bit, TI1.

The data is transferred to the transmitter register when the $\overline{\text{TBRL}}$ terminal goes from low to high. The loading of the transmitter register is delayed if the transmitter section is presently transmitting data. In this case the loading of the transmitter register is delayed until the transmission has been performed.

Output serial data (transmitted from the TO terminal) is clocked out by Transmitter Clock (TC). The clock rate is 16 times faster than the data rate.

The data is formatted as follows: start bit, data, parity bit, stop bits (1 or 2). Start bits, parity bits, and stop bits are generated by the TMS 6011. When no data is transmitted the output TO remains at a high level.

The start of transmission is defined as the transition of TO from a high to a low logic level.

Two flags are provided. A high level at the Transmitter Buffer Register Empty (TBRE) flag indicates that a word has been transferred to the transmitter/receiver and that the transmitter buffer register is now ready to accept a new word. A high level at the Transmitter Register Empty (TRE) flag indicates that the transmitter section has completed the transmission of a complete word including stop bits. The TRE flag will remain at a high level until the start of transmission of a new word.

Both the transmitter buffer register and the transmitter register are static and will perform long-term storage of data.

receiver section

The data is received in serial form at the Receiver Input (RI). The data from RI enters the receiver register at a point determined by the character length, the parity, and the number of stop bits. RI must be maintained high when no data is being received. The data is clocked by the Receiver Clock (RC). The clock rate is 16 times faster than the data rate.

Data is transferred from the receiver register to the receiver buffer register. The output data is then presented in parallel form at the eight Receiver Outputs (RO1 through RO8). The MOS output buffers used for the eight RO terminals are three-state push-pull output buffers that permit the wire-OR configuration through use of the Receiver Output Disable (ROD) terminal. When a high level is applied to ROD the RO outputs are floating. If the word length is less than 8 bits, the most significant bits will be at a low level. The output word is right justified. RO1 is the least significant bit and RO8 is the most significant bit.

A low level applied to the Data Ready Reset ($\overline{\text{DRR}}$) terminal resets the Data Ready (DR) output to a low level.

Several flags are provided in the receiver section. There are three error flags (Parity Error, Framing Error, and Overrun Error) and a DR flag. These status flags may be disabled by a high level at the Status Flags Disable (SFD) terminal.

A high level at the Parity Error (PE) terminal indicates an error in parity.

A high level at the Framing Error (FE) terminal indicates a framing error that is an invalid or nonexistent stop bit in the received word.

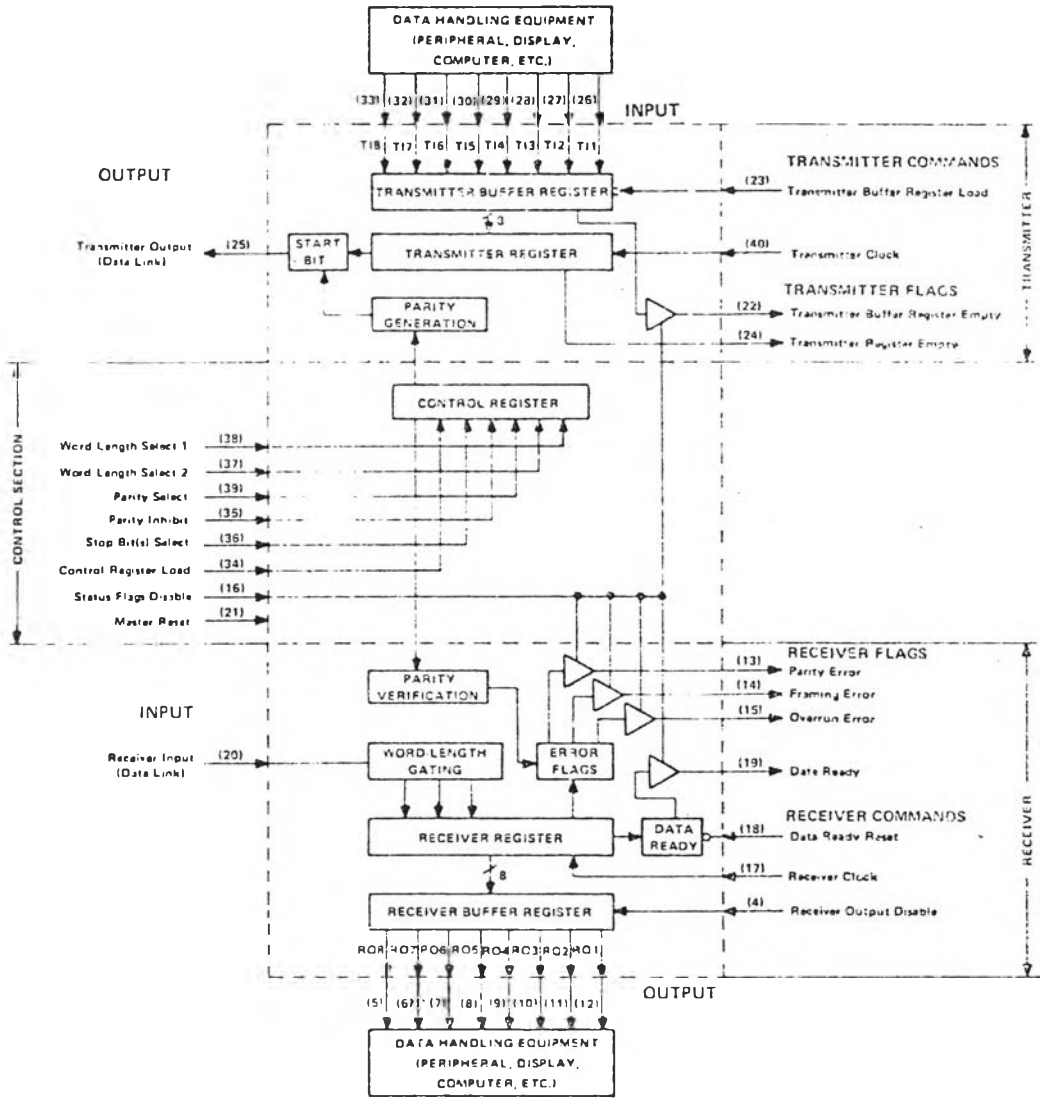
TMS 6011 JC,NC
ASYNCHRONOUS DATA INTERFACE (UART)

operation (continued)

A high level at the Overrun Error (OE) terminal indicates an overrun. An overrun occurs when the previous word has not been read, i.e., when the DR output has not been reset before the present data was transferred to the receiver buffer register.

A high level at the DR terminal indicates that a word has been received, stored in the receiver-buffer register and that the data is available at outputs RO1 through RO8. The DR terminal can be reset through the $\overline{DRR}$ terminal.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{DD} (see Note 1)	−20 V to 0.3 V
Supply voltage, V_{GG} (see Note 1)	−20 V to 0.3 V
Input voltage (any input) (see Note 1)	−20 V to 0.3 V
Operating free-air temperature range	−25°C to 85°C
Storage temperature range	−55°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the normally most positive supply, V_{SS} (substrate). Throughout the remainder of this data sheet voltage values are with respect to V_{DD}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}			0		V
Supply voltage, V_{GG}		−11.5	−12	−12.5	V
Supply voltage, V_{SS}		4.75	5	5.25	V
High-level input voltage, all inputs, V_{IH} (see Notes 2 and 3)		V_{SS} −1.5		V_{SS} +0.3	V
Low-level input voltage, all inputs, V_{IL} (see Notes 2 and 3)		−12		0.8	V
Pulse width, t_w	Clock	2.5			µs
	Transmitter buffer register load	400			ns
	Control register load	250			ns
	Parity inhibit (see Notes 4 and 5)	400			ns
	Parity select (see Notes 4 and 5)	300			ns
	Word length select and stop bit select (see Notes 4 and 5)	300			ns
	Master reset	1.5			µs
	Data ready reset	250			ns
Data setup time, $t_{su(da)}$		10↓			ns
Data hold time, $t_{h(da)}$		20↑			ns
Clock frequency, f_c (see Note 6)		0		200	kHz
Operating free-air temperature, T_A		−25		85	°C

NOTES: 2. All data, clock, and command inputs have internal pull-up resistors to allow direct clocking by any TTL circuit.

3. The algebraic convention where the most negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

4. Inputs to PI, PS, WLS1, WLS2, and SBS are normally static signals. A minimum pulse width has been indicated for possible pulsed operation.

5. All control signal pulses should be centered with respect to CRL to ensure maximum setup and hold time.

6. Clock frequency is 16 times the baud rate.

↑↓The arrow indicates the edge of the $\overline{TBRL}$ pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −100 µA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.6	V
I_{IH}	High-level input current, all inputs	V_I = 5 V			10	µA
I_{IL}	Low-level input current, all inputs	V_I = 0 V			−1.6	mA
I_{GG}	Supply current from V_{GG}	All inputs at a high level		11	16	mA
I_{SS}	Supply current from V_{SS}	All inputs at a high level		20	35	mA
P_D	Power dissipation	All inputs at a high level		240	385	mW
C_i	Input capacitance, all inputs	V_I = V_{SS}, f = 1 MHz		10	20	pF

†All typical values are at T_A = 25°C and nominal voltages.

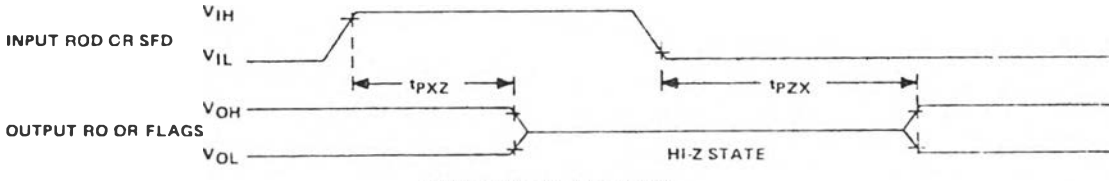
TMS 6011 JC,NC
ASYNCHRONOUS DATA INTERFACE (UART)

switching characteristics over full ranges of recommended operating conditions (unless otherwise noted)

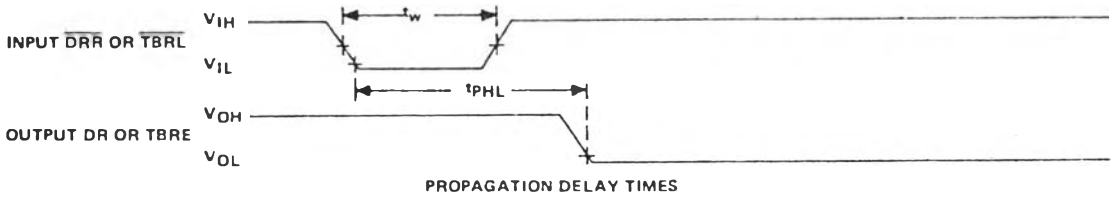
PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low level DR output from $\overline{DRR}$	1 Series 74 TTL load		800	1000	ns
t_{PHL}	Propagation delay time, high-to-low level TBRE output from $\overline{TBRL}$			800	1000	ns
t_{PZX}	Enable time, receiver output from ROD			300	500	ns
t_{PXZ}	Disable time, receiver output from ROD			300	500	ns
t_{PZX}	Enable time, outputs PE, FE, OE, DR, or TBRE from SFD			300	500	ns
t_{PXZ}	Disable time, outputs PE, FE, OE, DR, or TBRE from SFD			300	500	ns

†All typical values are at $T_A = 25°C$ and nominal voltages.

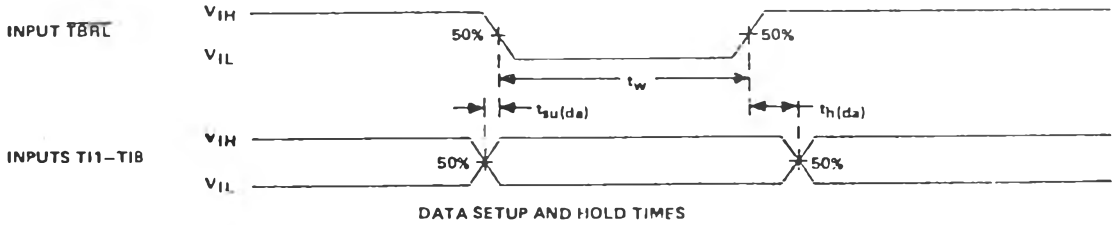
voltage waveforms



ENABLE AND DISABLE TIMES



PROPAGATION DELAY TIMES

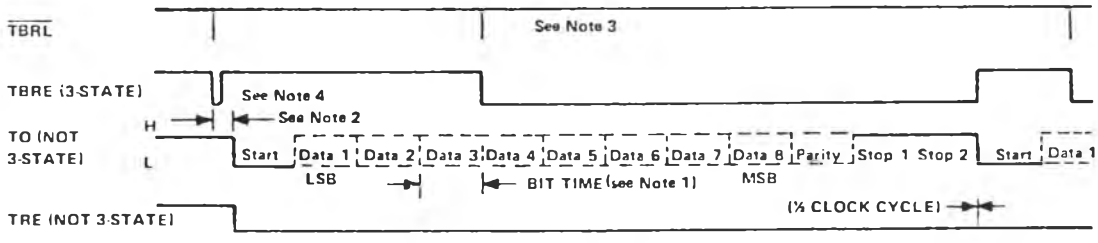


DATA SETUP AND HOLD TIMES

NOTE: All enable, disable, and propagation delay times are referenced to the 90% or 10% points. All pulse widths are referenced to the 50% points.

operation timing diagram

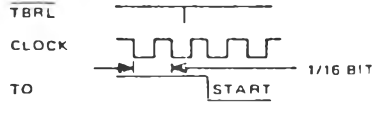
TRANSMITTER TIMING†



† Transmitter initially assumed inactive at start of diagram, shown for 8 level code and parity and 2 stops.

NOTES 1. Bit time is 16 clock cycles.

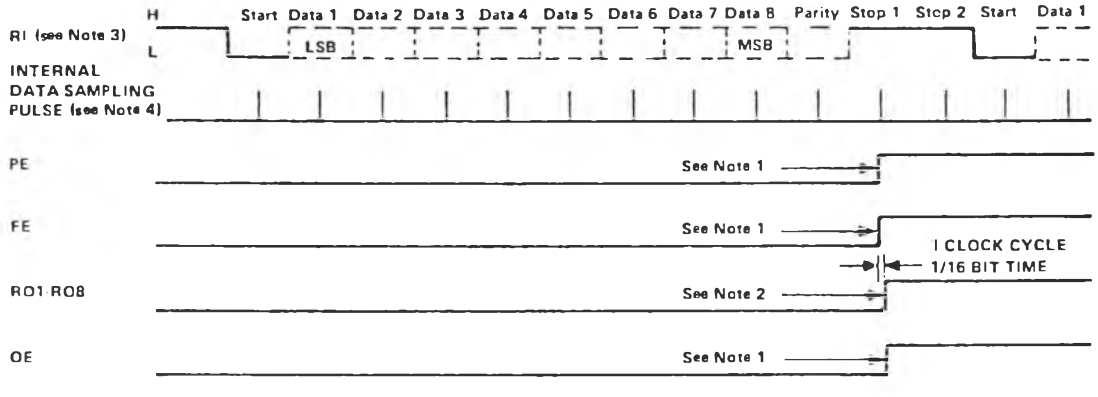
2. If transmitter is inactive the start pulse will appear on line within one clock cycle of time data strobe occurs (see detail below).



3. Because transmitter is double buffered, another data strobe can occur anywhere during transmission of character 1.

4. TBRE goes to a low for a period of approximately one clock cycle following a TBRL pulse.

RECEIVER TIMING



NOTES: 1. This is the point at which the error condition is detected, if error occurs.

2. A high-to-low transition on the DR pin indicates that the contents of the receiver register has been transferred to the receiver buffer register and that the three error-flag signals are valid. Output data remains valid until the next word is transferred into the receiver buffer register.

3. The RI waveform illustrates an eight-bit word with parity and two stop bits. If parity is inhibited, the stop bits immediately follow the last data bit. For all word lengths, the data in the buffer register must be right justified, i.e., RO1 (pin 12) is the least significant bit.

4. Data sampling occurs at the center of each data bit (8 clock cycles after the beginning of the bit).

COM 5016

Preliminary Specifications

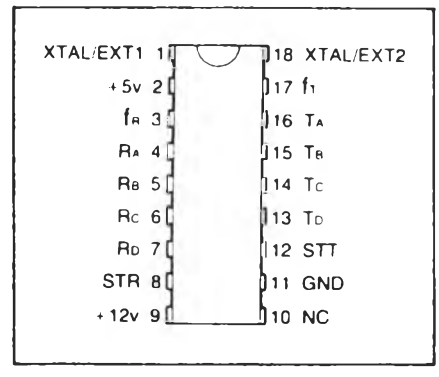
Dual Baud Rate Generator

Programmable Divider

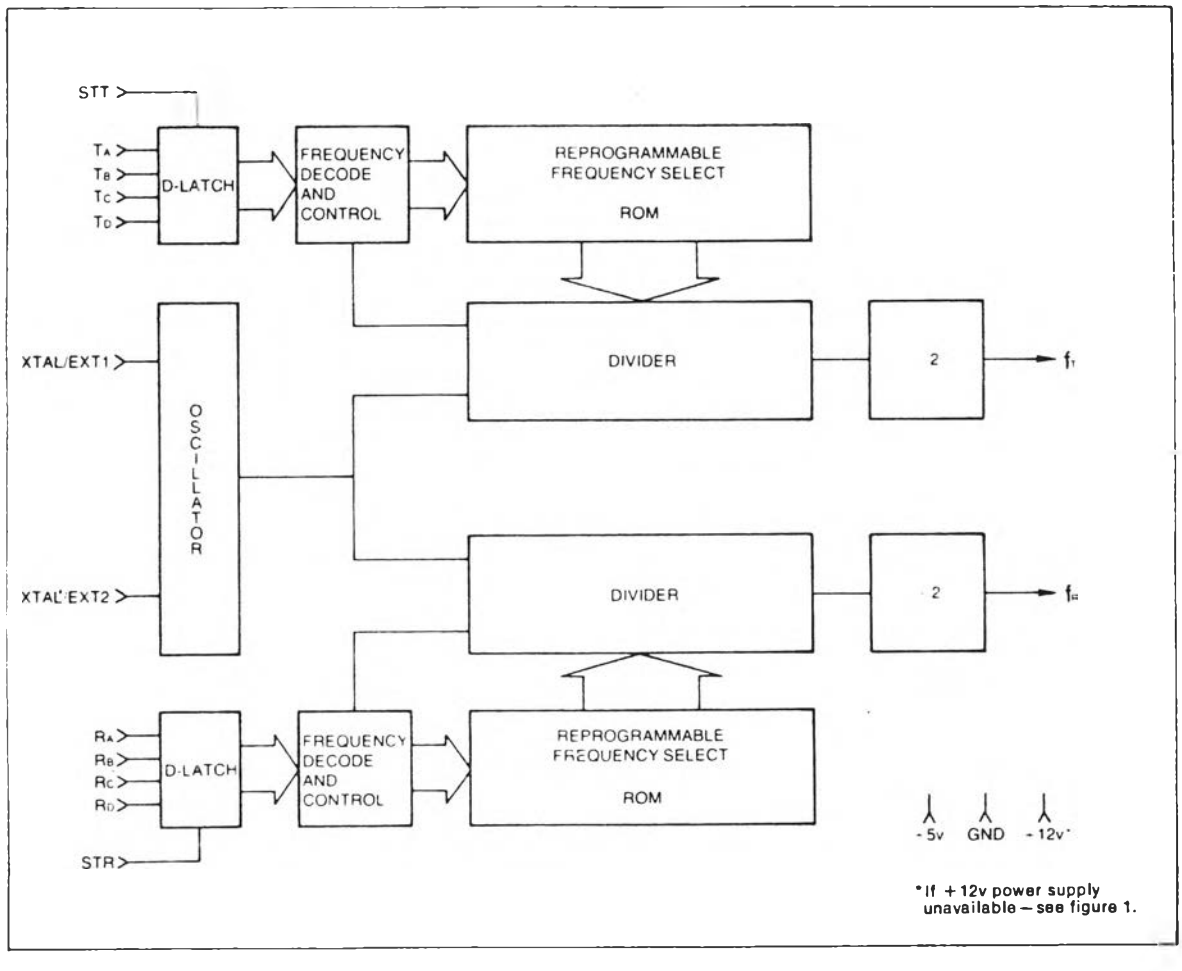
FEATURES

- ☐ On chip crystal oscillator or external frequency input
- ☐ Choice of 2 X 16 output frequencies
- ☐ 16 asynchronous/synchronous baud rates
- ☐ Direct UART/USRT compatibility
- ☐ Full duplex communication capability
- ☐ Re-programmable ROM allows generation of other frequencies
- ☐ TTL, MOS compatibility
- ☐ On chip input pull-up resistors
- ☐ 0.01% accuracy—typical
- ☐ 50% Duty Cycle
- ☐ 18 pin ceramic DIP package

PIN CONFIGURATION



BLOCK DIAGRAM



General Description

The Standard Microsystems COM 5016 Dual Baud Rate Generator/Programmable Divider is an N-channel COPLAMOS® MOS/LSI device which, from a single crystal (on-chip oscillator) or input frequency is capable of generating 32 externally selectable frequencies.

The COM 5016 is specifically dedicated to generating the full spectrum of 16 asynchronous/synchronous data communication frequencies as shown in Table 1. One of the sixteen output frequencies is externally selected by four address inputs, on each of the independent dividers, as shown in Table 1.

Internal re-programmable ROM allows the generation of other frequencies from other crystal frequencies or input frequencies. The four address inputs on each divider section may be strobe (150ns) or DC loaded. As the COM 5016 is a dual baud rate generator, full duplex (independent receive and transmit frequencies) operation is possible.

The COM 5016 is basically a programmable 15-stage feedback shift register capable of dividing any modulo up to $(2^{15}-1)$.

By using one of the frequency outputs it is possible to generate additional divisions of the master clock frequency by cascading COM 5016's. The frequency output is fed into the XTAL/EXT input on a subsequent device. In this way one crystal or input frequency may be used to generate numerous output frequencies.

The COM 5016 can be driven by either an external crystal or TTL logic level inputs; COM 5016T is driven by TTL logic level inputs only.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−55°C to + 150°C
Lead Temperature (soldering, 10 sec.)	+ 325°C
Positive Voltage on any Pin, with respect to ground	+ 18.0V
Negative Voltage on any Pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = +12V ±5%, unless otherwise noted)

Parameter	Min.	Typ.	Max	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	excluding XTAL inputs
High-level, V_{IH}	$V_{CC}-1.5$		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL} = 3.2mA
High-level, V_{OH}	$V_{CC}-1.5$	4.0		V	I_{OH} = 100μA
INPUT CURRENT					
Low-level, I_{IL}			0.3	mA	V_{IN} = GND, excluding XTAL inputs
INPUT CAPACITANCE					
All inputs, C_{IN}		5	10	pf	V_{IN} = GND, excluding XTAL inputs
EXT INPUT LOAD		8	10		Series 7400 unit loads
POWER SUPPLY CURRENT					
I_{CC}		28	45	mA	
I_{DD}		12	22	mA	
A.C. CHARACTERISTICS					T_A = +25°C
CLOCK FREQUENCY		5.0688		MHz	XTAL, EXT
PULSE WIDTH					
Clock					50% Duty Cycle ±5%
Receiver strobe	150		DC	ns	See Note 1.
Transmitter strobe	150		DC	ns	See Note 1.
INPUT SET-UP TIME					
Address	50			ns	See Note 1.
INPUT HOLD TIME					
Address	50			ns	
STROBE TO NEW FREQUENCY DELAY		2.0	2.5	μs	$=1/f_{IN}$ (12)

Note 1: Input set-up time can be decreased to ≥ 0ns by increasing the minimum strobe width by 50ns to a total of 200ns.

Table 1.

CRYSTAL FREQUENCY = 5.0688 MHz

Transmit/Receive Address D	C	B	A	Baud Rate	Theoretical Frequency 16X Clock	Actual Frequency 16X Clock	Percent Error	Duty Cycle %	Divisor
0	0	0	0	50	0 8 KHz	0 8 KHz	—	50/50	6336
0	0	0	1	75	1 2	1.2	—	50/50	4224
0	0	1	0	110	1 76	1.76	—	50/50	2880
0	0	1	1	134 5	2 152	2 1523	0 016	*	2355
0	1	0	0	150	2 4	2.4	—	50/50	2112
0	1	0	1	300	4.8	4 8	—	50 50	1056
0	1	1	0	600	9 6	9.6	—	50/50	528
0	1	1	1	1200	19.2	19 2	—	50/50	264
1	0	0	0	1800	28 8	28 8	—	50 50	176
1	0	0	1	2000	32 0	32 081	0 253	50 50	158
1	0	1	0	2400	38 4	38 4	—	50/50	132
1	0	1	1	3600	57 6	57.6	—	50 50	88
1	1	0	0	4800	76 8	76 8	—	50 50	66
1	1	0	1	7200	115 2	115 2	—	50 50	44
1	1	1	0	9600	153 6	153 6	—	*	33
1	1	1	1	19.200	307 2	316 8	3 125	50 50	16

* When Duty Cycle is not exactly 50%, it is 50% ± 10%.

Description of Pin Functions

Pin No.	Symbol	Name	Function
1	XTAL/EXT1	Crystal or External Input 1	This input is either one pin of the crystal package or one polarity of the external input
2	V_{CC}	Power Supply	+5 volt Supply
3	f_R	Receiver Output Frequency	This output runs at a frequency as selected by the Receiver Address
4-7	R_A, R_B, R_C, R_D	Receiver Address	The logic level on these inputs, as shown in Table 1, selects the receiver output frequency, f_R
8	STR	Strobe-Receiver Address	A high-level input strobe loads the receiver address (R_A, R_B, R_C, R_D) into the receiver address register. This input may be strobed or hard wired to a high-level
9	V_{DD}	Power Supply	+12 volt Supply
10	NC	No Connection	
11	GND	Ground	Ground
12	STT	Strobe-Transmitter Address	A high-level input strobe loads the transmitter address (T_A, T_B, T_C, T_D) into the transmitter address register. This input may be strobed or hard wirec to a high-level
13-16	T_D, T_C, T_B, T_A	Transmitter Address	The logic level on these inputs, as shown in Table 1, selects the transmitter output frequency, f_T
17	f_T	Transmitter Output Frequency	This output runs at a frequency as selected by the Transmitter Address
18	XTAL/EXT2	Crystal or External Input 2	This input is either the other pin of the crystal package or the other polarity of the external input

Table 2.

COM 5016-5
COM 5016T-5
CRYSTAL FREQUENCY = 4.9152 MHz

Transmit/Receive Address				Baud	Theoretical Frequency	Actual Frequency	Percent	Duty Cycle	
D	C	B	A	Rate	16X Clock	16X Clock	Error	%	Divisor
0	0	0	0	50	0.8 KHz	0.8 KHz	—	50/50	6144
0	0	0	1	75	1.2	1.2	—	50/50	4096
0	0	1	0	110	1.76	1.7598	−0.01	*	2793
0	0	1	1	134.5	2.152	2.152	—	50/50	2284
0	1	0	0	150	2.4	2.4	—	50/50	2048
0	1	0	1	300	4.8	4.8	—	50/50	1024
0	1	1	0	600	9.6	9.6	—	50/50	512
0	1	1	1	1200	19.2	19.2	—	50/50	256
1	0	0	0	1800	28.8	28.7438	−0.19	*	171
1	0	0	1	2000	32.0	31.9168	−0.26	50/50	154
1	0	1	0	2400	38.4	38.4	—	50/50	128
1	0	1	1	3600	57.6	57.8258	0.39	*	85
1	1	0	0	4800	76.8	76.8	—	50/50	64
1	1	0	1	7200	115.2	114.306	−0.77	*	43
1	1	1	0	9600	153.6	153.6	—	50/50	32
1	1	1	1	19,200	307.2	307.2	—	50/50	16

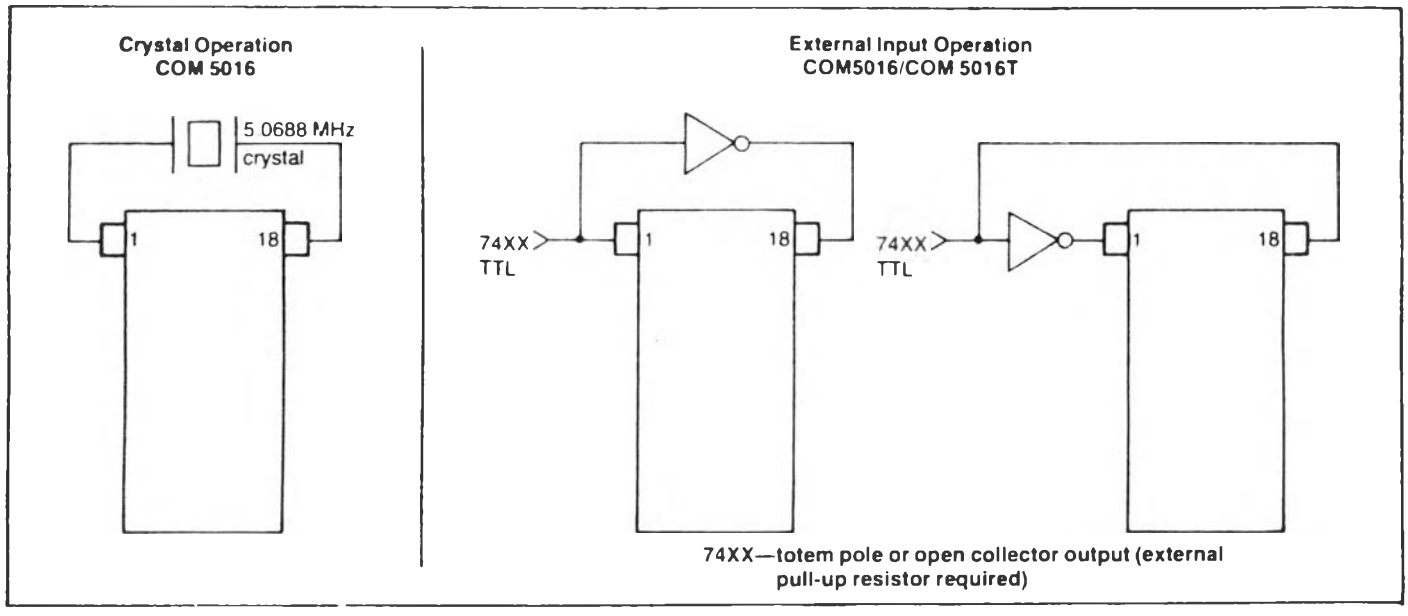
*When the duty cycle is not exactly 50% it is 50% ± 10%

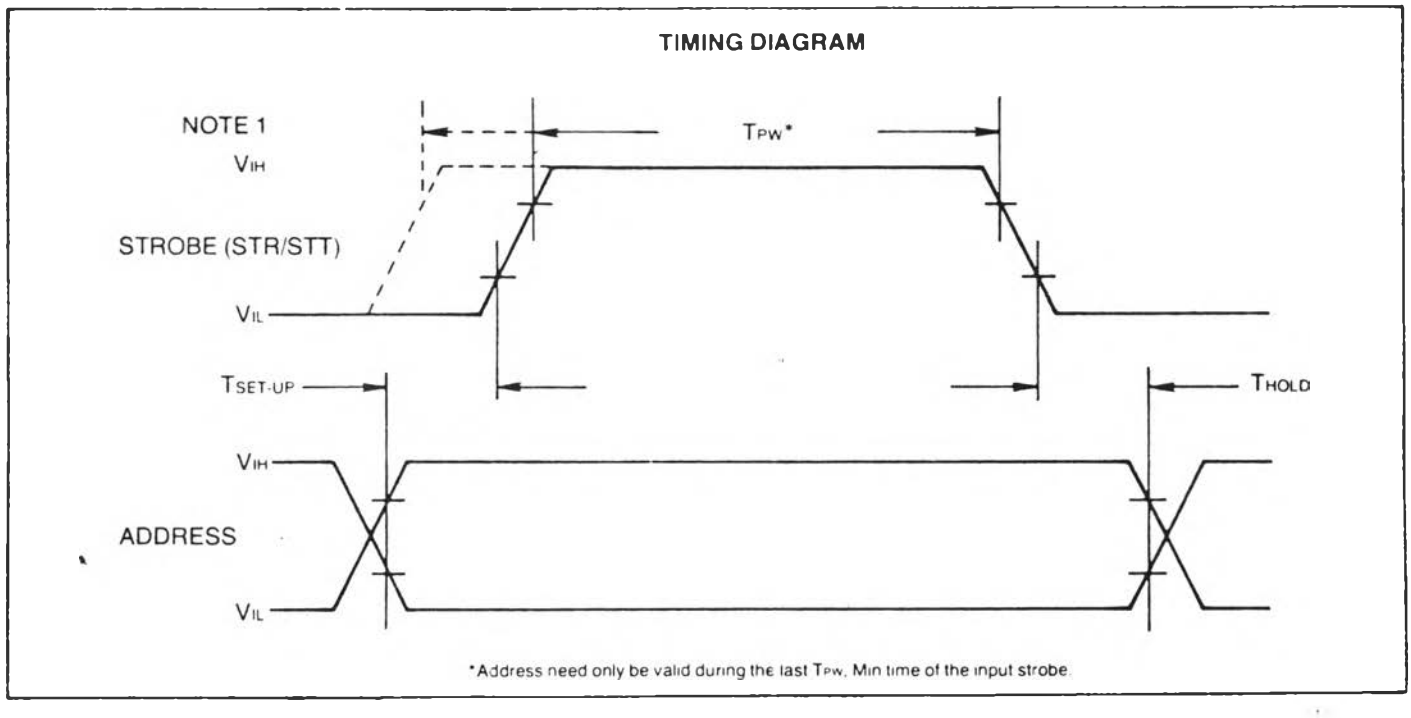
Table 3.

COM 5016-6
COM 5016T-6
CRYSTAL FREQUENCY = 5.0688 MHz

Transmit/Receive Address				Baud	Theoretical Frequency	Actual Frequency	Percent	Duty Cycle	
D	C	B	A	Rate	32X Clock	32X Clock	Error	%	Divisor
0	0	0	0	50	1.6 KHz	1.6 KHz	—	50/50	3168
0	0	0	1	75	2.4	2.4	—	50/50	2112
0	0	1	0	110	3.52	3.52	—	50/50	1440
0	0	1	1	134.5	4.304	4.306	.06	*	1177
0	1	0	0	150	4.8	4.8	—	50/50	1056
0	1	0	1	200	6.4	6.4	—	50/50	792
0	1	1	0	300	9.6	9.6	—	50/50	528
0	1	1	1	600	19.2	19.2	—	50/50	264
1	0	0	0	1200	38.4	38.4	—	50/50	132
1	0	0	1	1800	57.6	57.6	—	50/50	88
1	0	1	0	2400	76.8	76.8	—	50/50	66
1	0	1	1	3600	115.2	115.2	—	50/50	44
1	1	0	0	4800	153.6	153.6	—	*	33
1	1	0	1	7200	230.4	230.4	—	50/50	22
1	1	1	0	9600	307.2	316.8	3.125	50/50	16
1	1	1	1	19,200	614.4	633.6	3.125	50/50	8

*When the duty cycle is not exactly 50% it is 50% ± 10%





For ROM re-programming SMC has a computer program available whereby the customer need only supply the input frequency and the desired output frequencies. The ROM programming is automatically generated.

Crystal Specifications

User must specify termination (pin, wire, other)
Frequency — 5.0688 MHz, AT cut
Temperature range 0°C to 70°C
Series resistance - 50 Ω
Series Resonant
Overall tolerance ± .01%
or as required

Crystal manufacturers (Partial List)

Northern Engineering Laboratories
357 Beloit Street
Burlington, Wisconsin 53105
(414) 763-3591

Bulova Frequency Control Products
61-20 Woodside Avenue
Woodside, New York 11377
(212) 335-6000

CTS Knights Inc.
101 East Church Street
Sandwich, Illinois 60548
(815) 786-8411

APPLICATIONS INFORMATION

Charge pump techniques using the +5 volt power supply can be used to generate the +12 volt power supply required by the COM 5016. The +12 volt power supply of figure 1 will supply the 22 milliamps that is typically required.

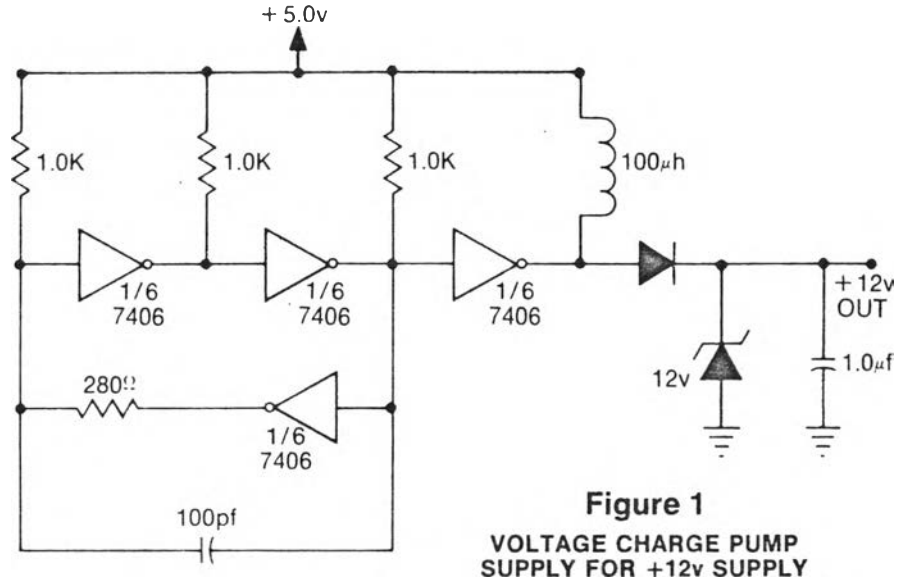


Figure 1
VOLTAGE CHARGE PUMP SUPPLY FOR +12v SUPPLY

When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that the clamp circuit of figure 2 or a Semtech* bi-polarity silicon transient suppressor such as the 1N6110 be used.

*SEMTECH CORPORATION
652 Mitchel Road
Newbury Park, California 91320
213-628-5392

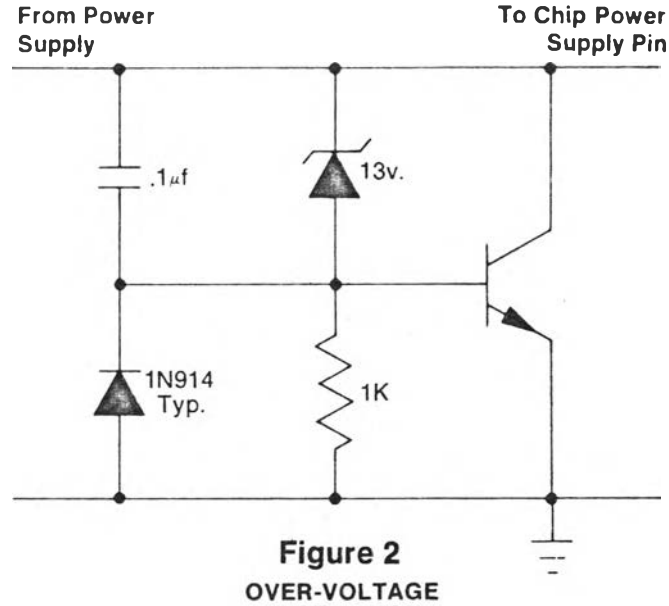
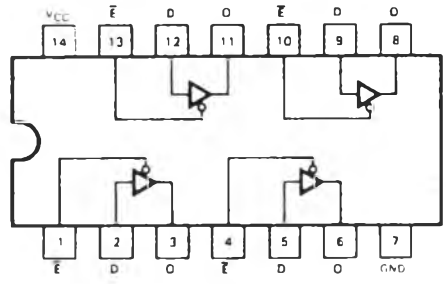


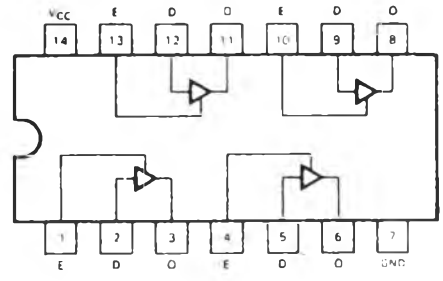
Figure 2
OVER-VOLTAGE PROTECTION CIRCUIT

SN54LS125A/SN74LS125A • SN54LS126A/SN74LS126A (formerly LS125, LS126)

QUAD 3-STATE BUFFERS WITH ACTIVE HIGH ENABLES



LS125A



LS126A

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE			TEMPERATURE
	MIN	TYP	MAX	
SN54LS125AX SN54LS126AX	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS125AX SN74LS126AX	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type; W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1		V	I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, V_E = V_{IL}	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, V_E = V_{IL}	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)		−30		−130	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current, Outputs LOW	LS125A			16	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 0 V	
		LS126A			20	mA	V_{CC} = MAX, V_{IN} = 0 V, V_E = 4.5 V	
	Power Supply Current, Outputs Off	LS125A			20	mA	V_{CC} = MAX, V_{IN} = 0 V, V_E = 4.5 V	
		LS126A			24	mA	V_{CC} = MAX, V_{IN} = 0 V, V_E = 0 V	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

TRUTH TABLES

LS125A

INPUTS		OUTPUT
$\overline{E}$	D	
L	L	L
L	H	H
H	X	(Z)

LS126A

INPUTS		OUTPUT
E	D	
H	L	L
H	H	H
L	X	(Z)

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
(Z) = High Impedance (off)

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output				10 16	ns	Fig. 2	V_{CC} = 5.0 V C_L = 45 pF
t_{PZH}	Output Enable Time to HIGH Level	LS125A			20	ns	Figs. 4, 5	
		LS126A			25			
t_{PZL}	Output Enable Time to LOW Level	LS125A			30	ns	Figs. 3, 5	
		LS126A			35			
t_{PLZ}	Output Disable Time from LOW Level				15	ns	Figs. 3, 5	V_{CC} = 5.0 V C_L = 5 pF R_L = 667 Ω
t_{PHZ}	Output Disable Time from HIGH Level				23	ns	Figs. 4, 5	

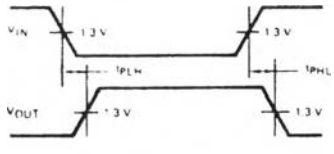


Fig. 1

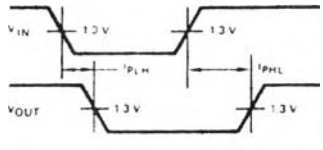


Fig. 2

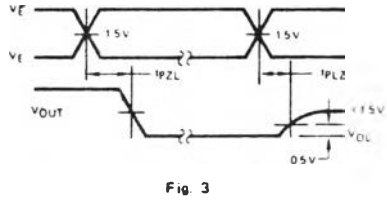


Fig. 3

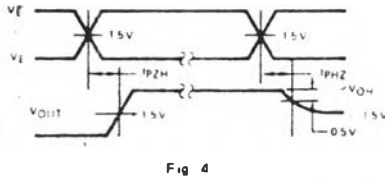
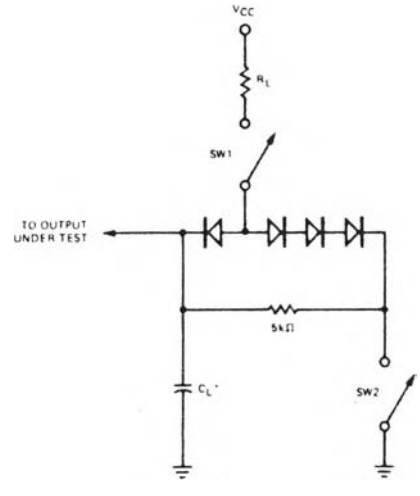


Fig. 4



SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 5

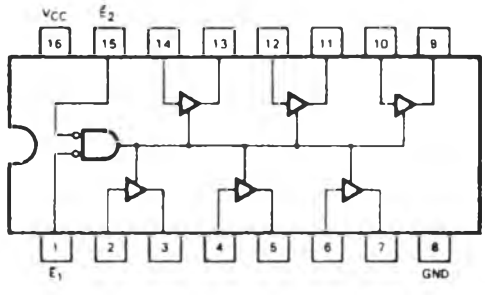
SN54LS365A/SN74LS365A • SN54LS366A/SN74LS366A
SN54LS367A/SN74LS367A • SN54LS368A/SN74LS368A

3-STATE HEX BUFFERS
(Formerly LS365, LS366, LS367, LS368)

DESCRIPTION — These devices are high speed hex buffers with 3-state outputs. They are organized as single 6-bit or 2-bit/4-bit, with inverting or non-inverting data (D) paths. The outputs are designed to drive 15 TTL Unit Loads or 60 Low Power Schottky loads when the Enable (E) is LOW.

When the Output Enable Input (E) is HIGH, the outputs are forced to a high impedance "off" state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

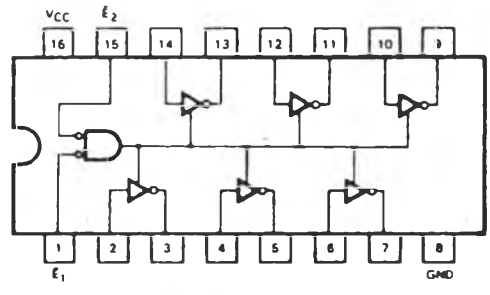
SN54LS365A/SN74LS365A
HEX 3-STATE BUFFER WITH COMMON 2-INPUT NOR ENABLE



TRUTH TABLE

INPUTS			OUTPUT
$\bar{E}_1$	$\bar{E}_2$	D	
L	L	L	L
L	L	H	H
H	X	X	(Z)
X	H	X	(Z)

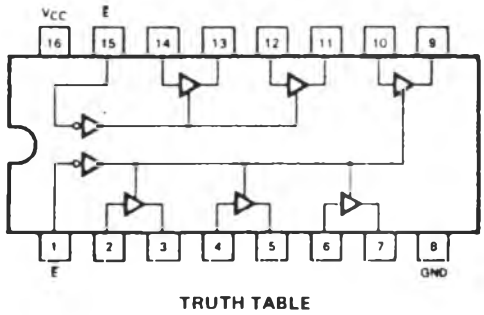
SN54LS366A/SN74LS366A
HEX 3-STATE INVERTER BUFFER WITH COMMON 2-INPUT NOR ENABLE



TRUTH TABLE

INPUTS			OUTPUT
$\bar{E}_1$	$\bar{E}_2$	D	
L	L	L	H
L	L	H	L
H	X	X	(Z)
X	H	X	(Z)

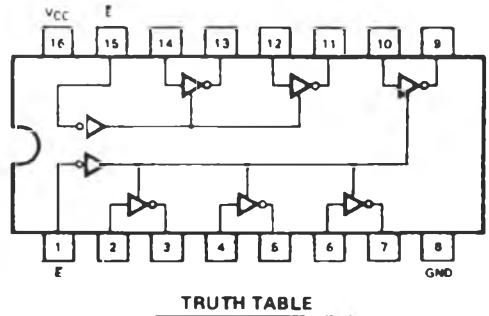
SN54LS367A/SN74LS367A
HEX 3-STATE BUFFER SEPARATE 2-BIT AND 4-BIT SECTIONS



TRUTH TABLE

INPUTS		OUTPUT
$\bar{E}$	D	
L	L	L
L	H	H
H	X	(Z)

SN54LS368A/SN74LS368A
HEX 3-STATE INVERTER BUFFER SEPARATE 2-BIT AND 4-BIT SECTIONS



TRUTH TABLE

INPUTS		OUTPUT
$\bar{E}$	D	
L	L	H
L	H	L
H	X	(Z)

SN54LS365A/SN74LS365A • SN54LS366A/SN74LS366A
SN54LS367A/SN74LS367A • SN54LS368A/SN74LS368A

GUARANTEED OPERATING RANGES

PART NUMBERS		SUPPLY VOLTAGE MIN	SUPPLY VOLTAGE TYP	SUPPLY VOLTAGE MAX	TEMPERATURE
SN54LS365AX SN54LS367AX	SN54LS366AX SN54LS368AX	4.5 V	5.0 V	5.5 V	−55°C to 125°C
SN74LS365AX SN74LS367AX	SN74LS366AX SN74LS368AX	4.75 V	5.0 V	5.25 V	0°C to 70°C

X = package type. W for Flatpak, J for Ceramic Dip, N for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{CD}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4			I_{OH} = −1.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.4	3.1			I_{OH} = −2.6 mA	
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V, $V_{\overline{E}}$ = 2.0 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 10 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Output Short Circuit Current (Note 3)		−30		−130	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current	LS365A/367A		13.5	24	mA	V_{CC} = MAX, V_{IN} = 0 V, $V_{\overline{E}}$ = 4.5 V	
		LS366A/368A		11.8	21			

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, T_A = 25°C.
3. Not more than one output should be shorted at a time.

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V (See SN54LS125A for Waveforms)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
t_{PLH} t_{PHL}	Propagation Delay, Data to Output (LS365A • LS367A)			10 16	ns	Fig. 2	C_L = 45 pF
t_{PLH} t_{PHL}	Propagation Delay, Data to Output (LS366A • LS368A)			10 16	ns	Fig. 1	C_L = 45 pF
t_{PZH}	Output Enable Time to HIGH Level			16	ns	Figs. 4, 5	C_L = 45 pF
t_{PZL}	Output Enable Time to LOW Level			30	ns	Figs. 3, 5	R_L = 667 Ω
t_{PLZ}	Output Disable Time from LOW Level			15	ns	Figs. 3, 5	C_L = 5.0 pF
t_{PHZ}	Output Disable Time from HIGH Level			23	ns	Figs. 4, 5	R_L = 667 Ω

HEX D-TYPE FLIP-FLOP WITH CLEAR 54/74174

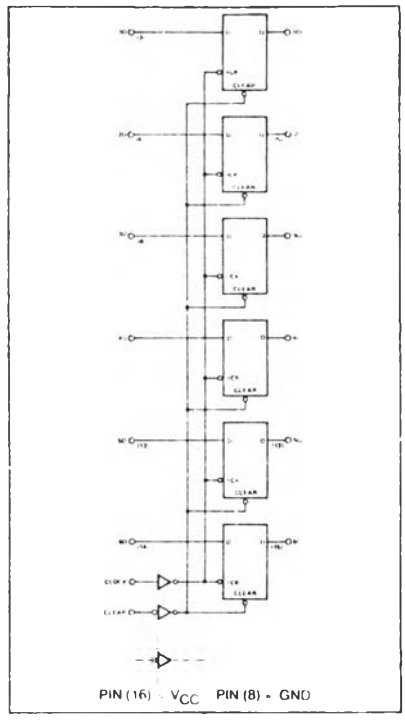
SPEED/PACKAGE AVAILABILITY

54	F,W	74	B
54LS	F,W	74LS	B
		74S	B

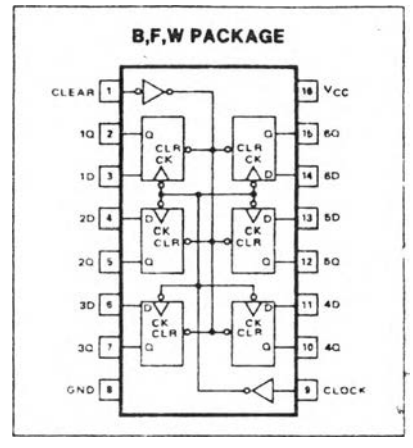
DESCRIPTION

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the input signal has no effect at the output.

BLOCK DIAGRAM



PIN CONFIGURATION



TRUTH TABLE (Each Flip-Flop)

INPUTS			OUTPUTS
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established

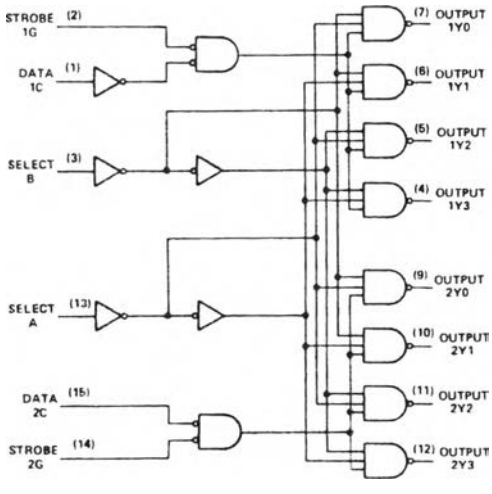
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L = 15pF R_L = 400Ω			54/74LS C_L = 15pF R_L = 2kΩ			54/74S C_L = 15pF R_L = 280Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			25	35		30	40		75	110		MHz
t_w	Width of pulse Clock			20			20			12			ns
	Clear												
t_{Setup}	Input setup time												ns
	Data			20			20↑			8			
	Clear inactive			25			25↑			15			
t_{Hold}	Input hold time			0			5↑			2			ns
Propagation delay time													
t_{PLH}	Low-to-high	Clock			20	30		20	30		9	12	ns
t_{PHL}	High-to-low				21	30		21	35		11	17	
t_{PHL}	High-to-low	Clear	Q		23	35		23	35		13	22	

Load circuit and typical waveforms are shown at the front of section

TYPES SN54155, SN54156, SN54LS155, SN54LS156, SN74155, SN74156, SN74LS155, SN74LS156
DUAL 2-LINE-TO-4-LINE DECODERS/DEMULTIPLEXERS

functional block diagram and logic



FUNCTION TABLES
2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

FUNCTION TABLE
3-LINE-TO-8-LINE DECODER
OR 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together
H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '155, '156 . . . . . 5.5 V
'LS155, 'LS156 . . . . . 7 V
Off-state output voltage: '155 . . . . . 5.5 V
'LS155 . . . . . 7 V
Operating free-air temperature range: SN54', SN54LS' Circuits . . . . . −55°C to 125°C
SN74', SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54155			SN74155			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54155 SN74155			UNIT
				MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54155	−20		−56	mA
			SN74155	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	SN54155		25	35	mA
			SN74155		26	40	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, 2C, 1G, or 2G	Y	2	C_L = 15 pF, R_L = 400 Ω, See Note 3		13	20	ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2			18	27	ns
t_{PLH}	A or B	Y	3			21	32	ns
t_{PHL}	A or B	Y	3			21	32	ns
t_{PLH}	1C	Y	3			16	24	ns
t_{PHL}	1C	Y	3			20	30	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

TYPES SN54LS155, SN74LS155
DUAL 2-LINE-TO-4-LINE DECODERS/DEMULTIPLEXERS

REVISED OCTOBER 1976

recommended operating conditions

	SN54LS155			SN74LS155			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS155			SN74LS155			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\ max}$, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\ max}$	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			6.1	10		6.1	10	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	SN54LS155 SN74LS155			UNIT
					MIN	TYP	MAX	
t_{PLH}	A, B, 2C, 1G, or 2G	Y	2	C_L = 15 pF, R_L = 2 kΩ, See Note 4		10	15	ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2			19	30	ns
t_{PLH}	A or B	Y	3			17	26	ns
t_{PHL}	A or B	Y	3			19	30	ns
t_{PLH}	1C	Y	3			18	27	ns
t_{PHL}	1C	Y	3			18	27	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 3-11.

QUAD LINE DRIVER — MC1438

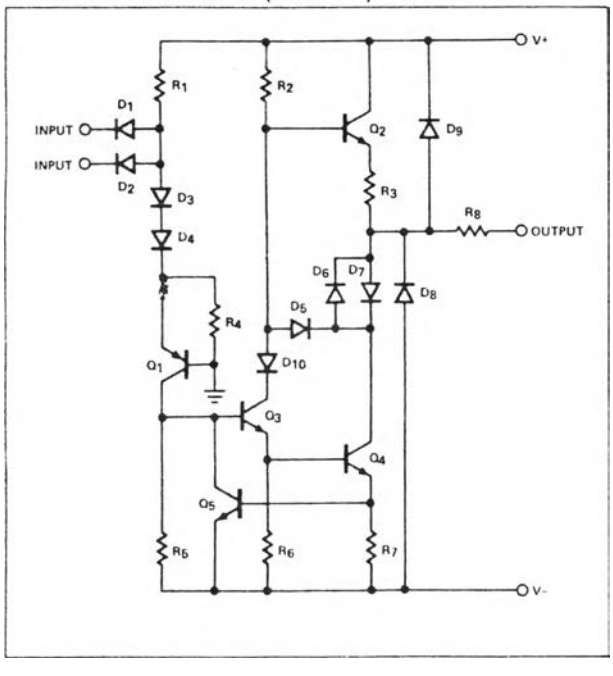
FEATURES

- CURRENT LIMITED OUTPUT: ±10mA TYP
- POWER-OFF SOURCE IMPEDANCE: 300Ω MIN
- SIMPLE SLEW RATE CONTROL WITH EXTERNAL CAPACITOR
- FLEXIBLE OPERATING SUPPLY RANGE
- INPUTS ARE DTL/TTL COMPATIBLE

ABSOLUTE MAXIMUM RATINGS (Note 1)

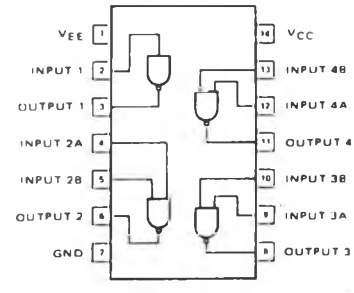
Supply Voltage V+	+15V
V−	−15V
Input Voltage (VIN)	−15V ≤VIN ≤7.0V
Output Voltage	±15V
Power Dissipation	1000mW
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +175°C
Lead Temperature (Soldering, 10 sec)	300°C

CIRCUIT SCHEMATIC (¼CIRCUIT)

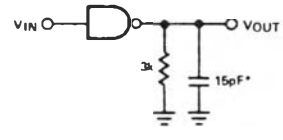


PIN CONFIGURATION

F PACKAGE

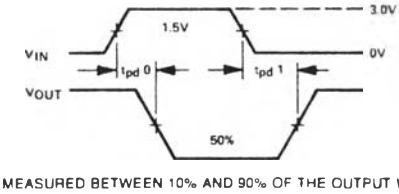


AC LOAD CIRCUIT



*CL INCLUDES PROBE AND JIG CAPACITANCE

SWITCHING WAVEFORMS



tr and tf ARE MEASURED BETWEEN 10% AND 90% OF THE OUTPUT WAVEFORM

SWITCHING CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay to "1" (tpd1)	RL = 3.0kΩ, CL = 15pF, TA = 25°C		230	300	ns
Propagation Delay to "0" (tpd0)	RL = 3.0kΩ, CL = 15pF, TA = 25°C		70	175	ns
Rise Time (tr)	RL = 3.0kΩ, CL = 15pF, TA = 25°C		75	100	ns
Fall Time (tf)	RL = 3.0kΩ, CL = 15pF, TA = 25°C		40	75	ns

NOTES

1. Voltage values shown are with respect to network ground terminal. Positive current is defined as current into the referenced pin.
2. These specifications apply for V+ = +9.0V ± 1%, V− = −9.0V ± 1%, TA = 0°C to +75°C unless otherwise noted. All typicals are for V+ = 9.0V, V− = −9.0V, and TA = 25°C.

QUAD LINE DRIVER — MC1488

APPLICATIONS

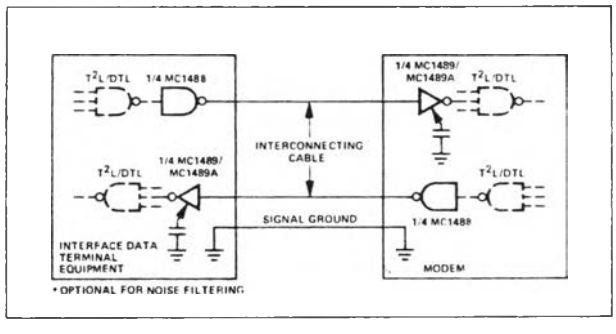
By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the MC1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

$$C = I_{SC}\,(\Delta T/\Delta V)$$

where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate

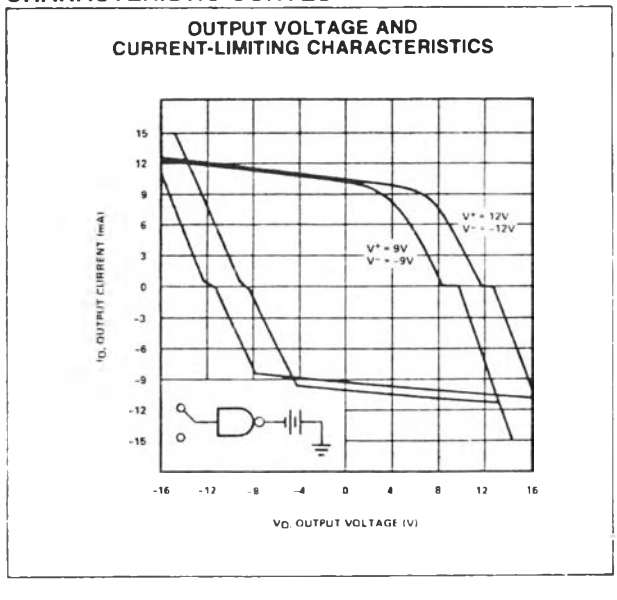
RS232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12mA in the above equation, calculations result in a required capacitor of 400pF connected to each output.

RS232C DATA TRANSMISSION



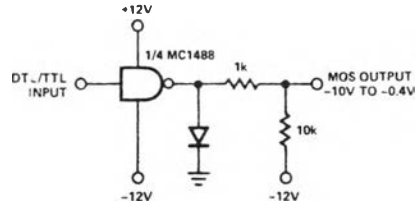
CHARACTERISTIC CURVES

OUTPUT VOLTAGE AND CURRENT-LIMITING CHARACTERISTICS

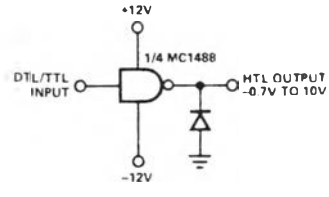


TYPICAL APPLICATIONS

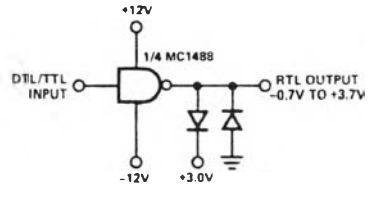
DTL/TTL-TO-MOS TRANSLATOR



DTL/TTL-TO-HTL TRANSLATOR



DTL/TTL-TO-RTL TRANSLATOR



QUAD LINE RECEIVERS — MC1489/MC1489A

MC1489F MC1489A-F

FEATURES

- FOUR TOTALLY SEPARATE RECEIVERS PER PACKAGE
- PROGRAMMABLE THRESHOLD
- BUILT-IN INPUT THRESHOLD HYSTERESIS
- "FAIL SAFE" OPERATING MODE
- INPUTS WITHSTAND ±30V

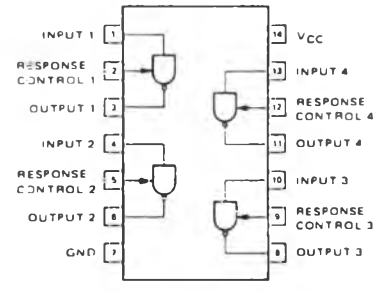
ABSOLUTE MAXIMUM RATINGS

The following apply for TA = 25°C unless otherwise specified

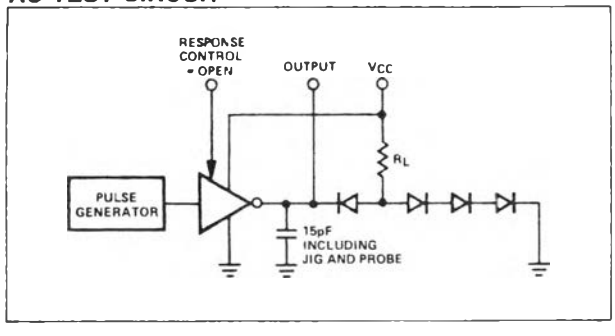
Power Supply Voltage	10V
Input Voltage Range	±30V
Output Load Current	20mA
Power Dissipation	1W
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +175°C

PIN CONFIGURATION

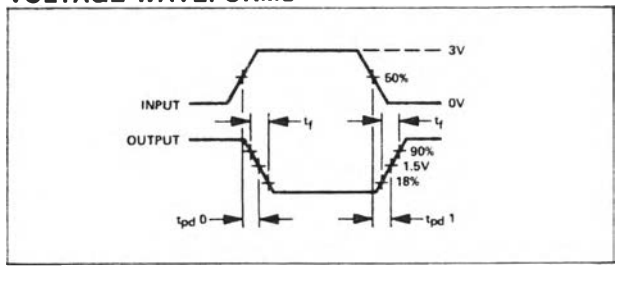
F PACKAGE



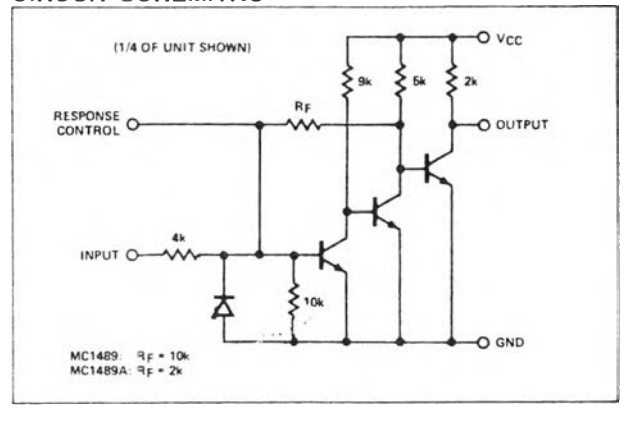
AC TEST CIRCUIT



VOLTAGE WAVEFORMS



CIRCUIT SCHEMATIC



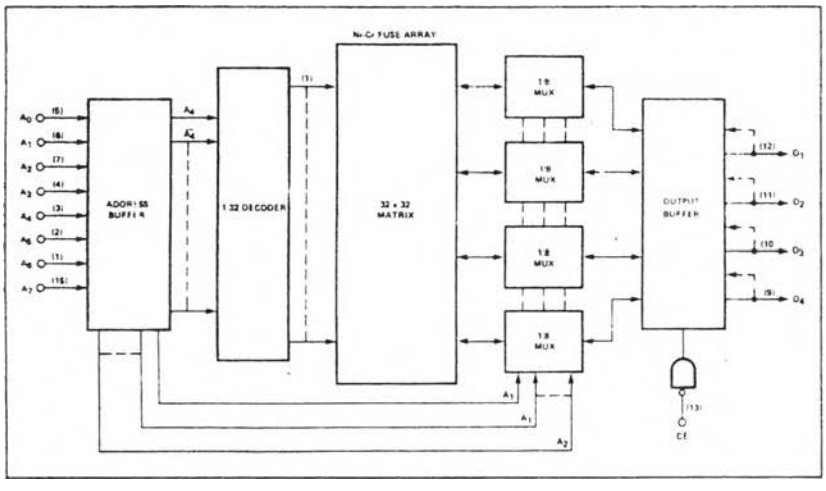
SWITCHING CHARACTERISTICS MC1489/MC1489A V_{CC} = 5.0V ±1%, T_A = 25°C

PARAMETER	CONDITIONS	MC1489			MC1489A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input to Output "High" Propagation Delay (t_{pd1})	R_L = 3.9k (AC Test Circuit)		25	85		25	85	ns
Input to Output "Low" Propagation Delay (t_{pd0})	R_L = 390Ω (AC Test Circuit)		20	50		20	50	ns
Output Rise time	R_L = 3.9k (AC Test Circuit)		110	175		110	175	ns
Output Fall Time	R_L = 390Ω (AC Test Circuit)		9	20		9	20	ns

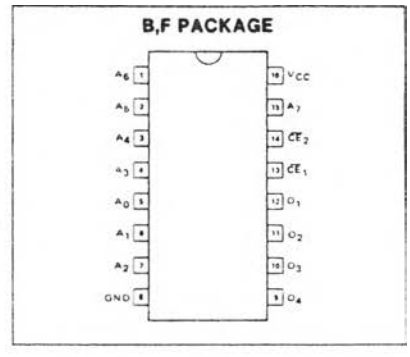
1024-BIT BIPOLAR PROM (256x4) — 82S126/129

N82S126/129-B,F. • S82S126/129F

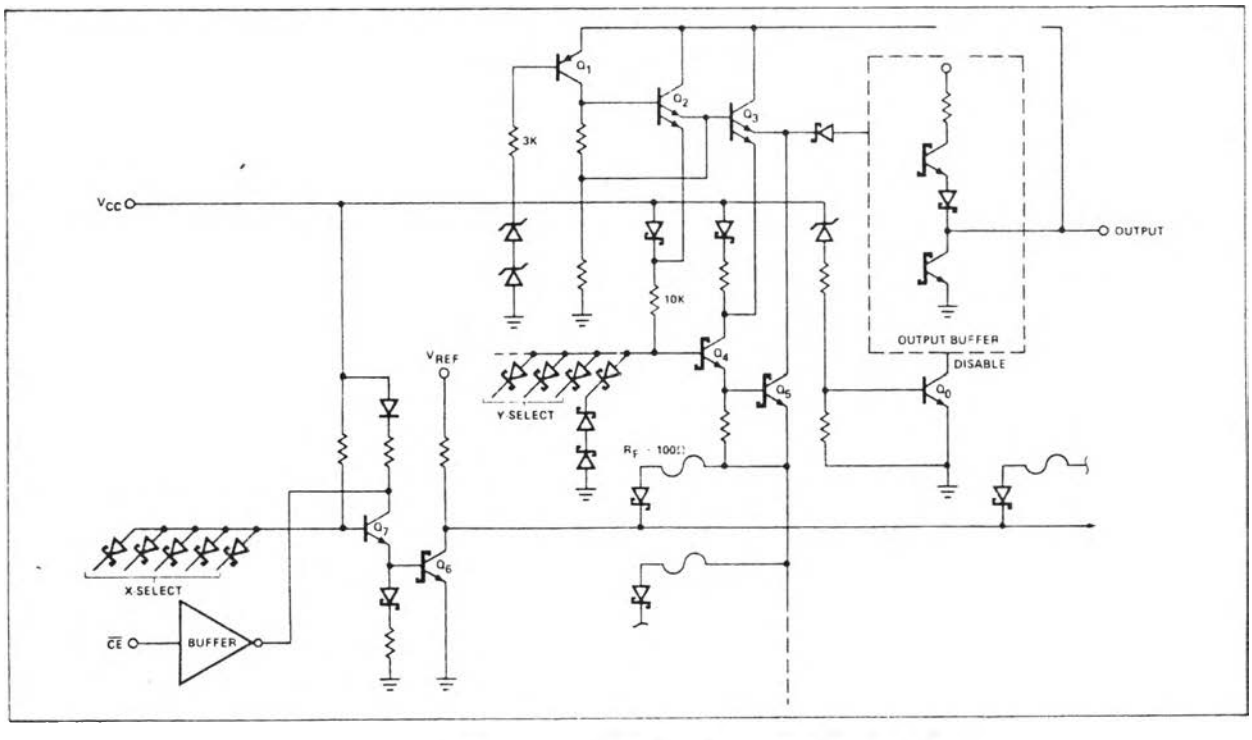
BLOCK DIAGRAM



PIN CONFIGURATION



TYPICAL FUSING PATH



AC ELECTRICAL CHARACTERISTICS

S82S126/129 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S126/129 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S82S126/129			N82S126/129			UNIT
			MIN	TYP2	MAX	MIN	TYP2	MAX	
Propagation Delay									
T_{AA}	Address to Output	C_L = 30pF		35	70		35	50	ns
T_{CD}	Chip Disable to Output	R_1 = 270Ω		15	35		15	20	ns
T_{CE}	Chip Enable to Output	R_2 = 600Ω		15	35		15	20	ns

NOTES
1. Positive current is defined as into the terminal referenced
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) T_A = +25°C

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	I_{CCP} 350 ± 50mA (Transient or steady state)	8.5	8.75	9.0	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	V_{CCP} = +8.75 ± .25V	300	350	400	mA
Input Voltage						
V_{IH}	Logical "1"		2.4		5.5	V
V_{IL}	Logical "0"		0	0.4	0.8	V
Input Current						
I_{IH}	Logical "1"	V_{IH} = +5.5V			50	µA
I_{IL}	Logical "0"	V_{IL} = +0.4V			-500	µA
V_{OUT}[2]	Output Programming Voltage	I_{OUT} = 200 ± 20mA (Transient or steady state)	16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	V_{OUT} = 17 ± 1V	180	200	220	mA
T_R	Output Pulse Rise Time		10		50	µs
t_p	$\overline{CE}$ Programming Pulse Width		1		2	ms
t_D	Pulse Sequence Delay		10			µs
T_{PR}	Programming Time	V_{CC} = V_{CCP}			2.5	sec
T_{PS}	Programming Pause	V_{CC} = 0V	5			sec
$\frac{T_{PR}}{T_{PR} + T_{PS}}$[4]	Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10KΩ resistor to V_{CC}.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP} = 8.75 ± .25V.
3. After 10µs delay, apply V_{OUT} = +17 ± 1V to the output to be programmed. Program one output at the time.
4. After 10µs delay, pulse both $\overline{CE}$ inputs to logic "0" for 1 to 2 ms.
5. After 10µs delay, remove +17V from the programmed output.
6. To verify programming, after 10µs delay, lower V_{CC} to V_{CCH} = +5.5 ± .2V and apply a logic "0" level to both $\overline{CE}$ inputs. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the "1" state.
7. Raise V_{CC} to V_{CCP} = 8.75 ± .25V, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10µs delay, repeat steps 2 through 7 to program all other address locations.

NOTES

1. Bypass V_{CC} to GND with a 0.01µF capacitor to reduce voltage spikes.
2. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program Verify cycle with a Rest period (V_{CC} = 0V) of 4ms.

ประวัติผู้เขียน

นายเพ็ชรัตน์ อารีรักษ์ เกิดเมื่อวันที่ 17 ธันวาคม พ.ศ. 2495 ที่จังหวัดพิจิตร สำเร็จการศึกษาปริญญาครุศาสตรอุตสาหกรรมบัณฑิต สาขาวิชาไฟฟ้า – อีเล็กโทรนิคส์ จากวิทยาลัยเทคโนโลยีและอาชีวศึกษา ปีการศึกษา 2520 ปัจจุบันรับราชการที่ภาควิชาวิศวกรรมคอมพิวเตอร์ คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย