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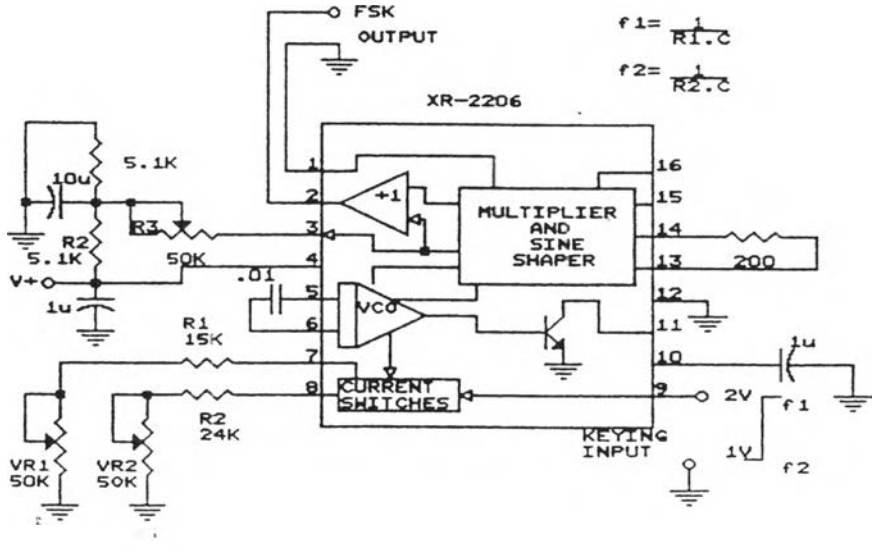
ภาคผนวก ก.

รายละเอียดการคำนวนค่าอุปกรณ์ที่ใช้ในวงจร

การออกแบบวงจร FSK modulation

เลือกใช้วงจรไมโครของ EXAR No. XR-2206 จากวงจรแบบ sinusoidal FSK generator ดังรูป ก.1 และใช้ XR-2211 ในการ demodulator ดังรูป ก.2



รูปที่ ก.1 วงจร modulation ของ IC เบอร์ XR-2206

ก.1) การคำนวนค่าที่ใช้ในวงจร FSK modulation

ในการออกแบบได้กำหนดความเร็วในการส่งสัญญาณ คือ Baud Rate ไว้ที่ความเร็ว 1200 bps. และกำหนดให้สัญญาณลอจิก High (1) ให้เป็น f_1 ในขณะที่กำหนดสัญญาณลอจิก Low (0) ให้เป็น f_2

กำหนดให้ $f_1 = 2 \times$ Baud rate

$= 2 \times 1200$

$= 2400$ Hz

$f_2 = 3000$ Hz

ค่า $C = 0.1\ \mu F$

จะได้ค่า R_1 จากสูตร $f_1 = 1/R_1C$

$$R_1 = 1/(2400 \times 0.1 \times 10^{-6})$$

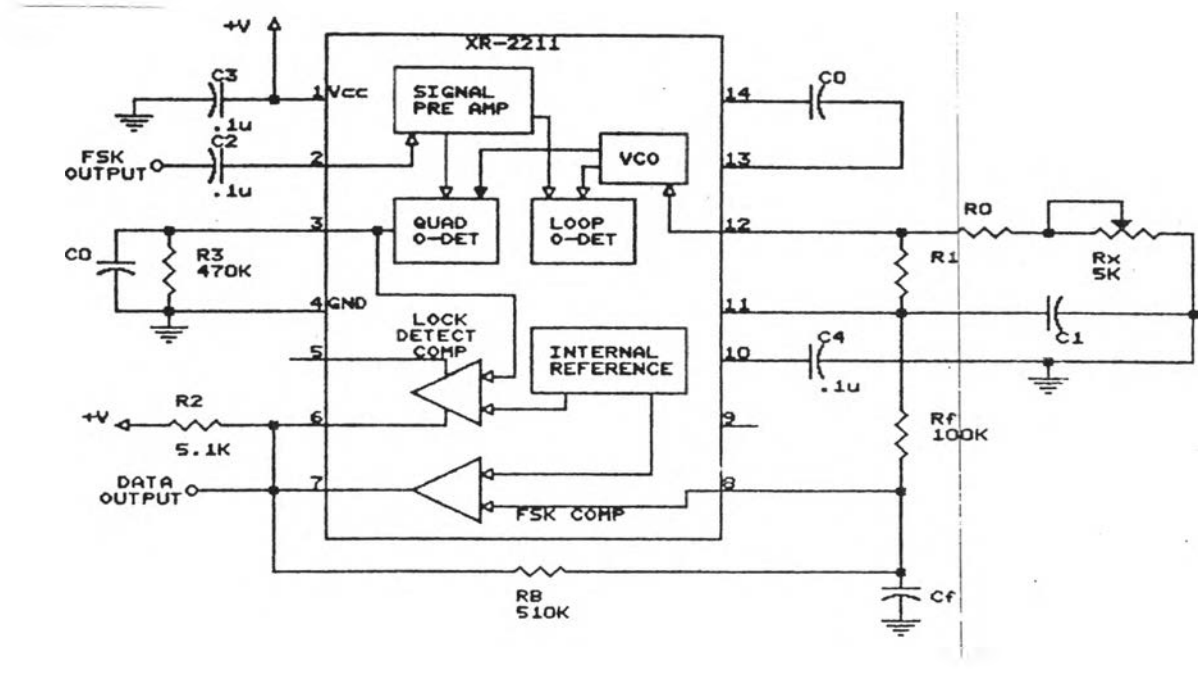
$= 4.1\ k\Omega$ ใช้ $5\ k\Omega$

ในทำนองเดียวกัน

$$R_2 = 1/(3000 \times 0.1 \times 10^{-6})$$
$$= 3.3\ k$$

แต่การใช้งานได้ใช้ R_1 และ R_2 แบบปรับค่าได้เพื่อใช้ในการปรับแต่งสัญญาณ

ก.2) การคำนวนค่าที่ใช้ในวงจร FSK demodulator



รูปที่ ก.2 วงจร demodulator ของวงจรเบอร์ XR-2211

ในการคำนวนมีขั้นตอนดังต่อไปนี้

หา $f_0 = (f_1+f_2)/2$; f_0 = PLL Center Frequency

$f_1 = 2400$ Hz ; จาก FSK modulation

$f_2 = 3000$ Hz

$f_0 = (2400+3000)/2$

$= 2700$ Hz

เลือกค่า R_0 ที่อยู่ระหว่าง 10 kΩถึง 100 kΩแต่ที่นิยมใช้กันคือ 20 kΩ

หาค่า C_0 จาก $C_0 = 1/(R_0 F_0)$

$C_0 = 1/(20 \times 10^3 \times 2700)$

$= 0.018 \ \mu F$ เลือกใช้ค่า $0.022 \ \mu F$

หาค่า R_1 ซึ่งหามาจากความถี่ MARK และ SPACE ของ FSK

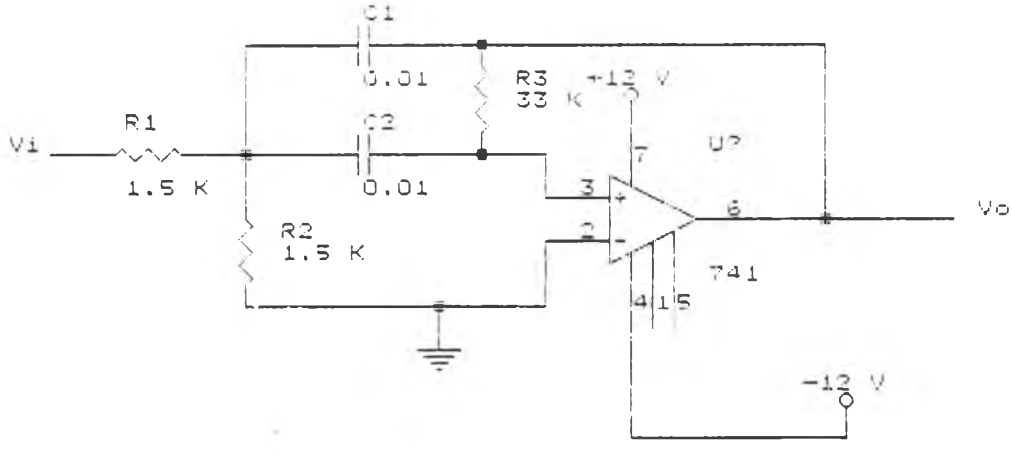
$R_1 = R_0 \times f_0/(f_2-f_1)$

$R_1 = 20k \times 2700 /(3000-2400)$

$= 90.0 \ k\Omega$

ก.3 การออกแบบวงจรกรองความถี่[9]

เนื่องจากระบบที่ทำการออกแบบใช้ความถี่ในการมอดูเลตสัญญาณโดยที่ลอจิก 0 ที่ระดับสัญญาณ 1 โวลต์ ใช้ความถี่ 2 kHz และลอจิก 1 ที่ระดับสัญญาณ 2 โวลต์ ใช้ความถี่ 3 MHz แต่หลังจากที่เครื่องส่งรับสัญญาณมาแล้วทางเอาท์พุตจะมีสัญญาณรบกวนสูงจึงต้องทำการกรองความถี่โดยเลือกเฉพาะช่วง 2 kHz ถึง 3 kHz เท่านั้น ฉะนั้นจึงต้องมีการออกแบบวงจรกรองความถี่ แบบ band pass filter ซึ่งมีขั้นตอนการออกแบบดังนี้



รูปที่ ก.3 วงจร band pass filter

กำหนดให้ f_0 = 2500 Hz

H = 10 [gain]

Q = $f_0/\Delta f$ =2500/1000 = 2.5

V_{oo} = 1 V

$A_v(f_0)$ = 1(2500 Hz) = 2500

I_b = 10^{-8} A

ให้ C_1 = C_2 = 0.01 μF

จากสูตร R_3 = $2Q/2\pi f_0 CH$

= (2 x 2.5)/(2 x π x 2500 x 10^{-8}

= 31.8 kΩ

และ R_1 = $Q/2\pi f_0 CH$ = $2.5/(2x\pi x2500x0.01x10^{-6}x10)$

= 1.59 k

ดังนั้น R_2 = $Q/(2\pi f_0 C)(2Q^2 - H)$

= $2.5/(2\pi x2500x0.01x10^{-6})[2(2.5)^2 - 2.5]$

= 1.59 kΩ

ทดสอบค่า V_{oo}

ให้ I_b = 10^{-8} A

จากสูตร V_{oo} = $I_b R_3$

= 10^{-8} x 31.8 x 10^3

= 0.3 mV

จะเห็นได้ว่า ค่า V_{oo} ซึ่งเป็นค่า output offset voltage ใกล้เคียงกับค่าที่กำหนดไว้

เมื่อ

f_0 = resonant frequency of circuit

Δf = frequency difference between -3 dB

H = voltage gain of circuit at f_0

Q = quality factor of circuit

I_b = input bias current if op-amp

V_{oo} = circuit output offset voltage

ภาคผนวก ข.

ลักษณะเฉพาะของอุปกรณ์ที่ใช้

ANALOG DEVICES

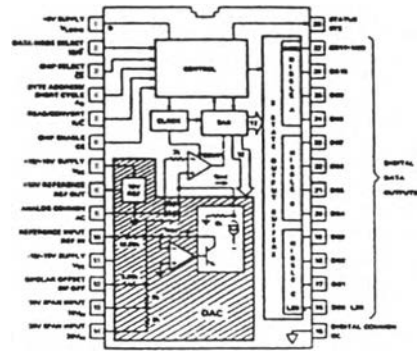
Fast, Complete 12-Bit A/D Converter with Microprocessor Interface

AD574A

FEATURES

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8- or 16-Bit Microprocessor Bus Interface
- 250ns Bus Access Time
- Guaranteed Linearity Over Temperature
  - 0 to +70°C – AD574AJ, AK, AL
  - −55°C to +125°C – AD574AS, AT, AU
- No Missing Codes Over Temperature
- Fast Successive Approximation Conversion – 25µs
- Buried Zener Reference for Long-Term Stability and Low Gain T.C. 10ppm/°C max AD574AL 12.5ppm/°C max AD574AU
- Low Profile 28-Pin Ceramic DIP
- Low Power: 390mW

AD574A FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD574A is a complete 12-bit successive-approximation analog-to-digital converter with 3-state output buffer circuitry for direct interface to an 8-, 12-or 16-bit microprocessor bus. The AD574A design is implemented with two LSI chips each containing both analog and digital circuitry, resulting in the maximum performance and flexibility at the lowest cost.

One chip is the high performance AD565A 12-bit DAC and voltage reference. It contains the high speed current output switching circuitry, laser-trimmed thin film resistor network, low T.C. buried zener reference and the precision input scaling and bipolar offset resistors. This chip is laser-trimmed at the wafer stage (LWT) to adjust ladder network linearity, voltage reference tolerance and temperature coefficient, and the calibration accuracy of input scaling and bipolar offset resistors.

The second chip uses the proven LCI linear-compatible integrated injection logic process to provide the low-power I^2L successive-approximation register, converter control circuitry, clock, bus interface, and the high performance latching comparator. The precision, low-drift comparator is adjusted for initial input offset error at the wafer stage by the "zener-zap" technique which trims the comparator input stage to 1/10 LSB typical error. This form of trimming, while cumbersome for complex ladder networks, is an attractive alternative to thin film resistor trimming for a simple offset adjustment and eliminates the need for thin film processing for this portion of the circuitry.

The AD574A is available in six different grades. The AD574AJ, AK, and AL grades are specified for operation over the 0 to +70°C temperature range. The AD574AS, AT, and AU are specified for the −55°C to +125°C range. All grades are packaged in a low-profile, 0.600 inch wide, 28-pin hermetically-sealed ceramic DIP.

PRODUCT HIGHLIGHTS

10

1. The AD574A interfaces to most popular microprocessors with an 8-, 12-, or 16-bit bus without external buffers or peripheral interface controllers. Multiple-mode three-state output buffers connect directly to the data bus while the read and convert commands are taken from the control bus. The 12-bits of output data can be read either as one 12-bit word or as two 8-bit bytes (one with 8 data bits, the other with 4 data bits and 4 trailing zeros).
2. The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges, 0 to +10 and 0 to +20 volts unipolar, or −5 to +5 and −10 to +10 volts bipolar. Typical bipolar offset and full scale calibration of ±0.1% can be trimmed to zero with one external component each.
3. The internal buried zener reference is trimmed to 10.00 volts with 1% maximum error and 15ppm/°C typical T.C. The reference is available externally and can drive up to 1.5mA beyond that required for the reference and bipolar offset resistors.

SPECIFICATIONS (@ = 25°C with V_{CC} = +15V, V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise indicated)

Model	AD574AJ Min	AD574AJ Typ	AD574AJ Max	AD574AK Min	AD574AK Typ	AD574AK Max	AD574AL Min	AD574AL Typ	AD574AL Max	Units
RESOLUTION			12			12			12	Bits
LINEARITY ERROR										
25°C (max)			±1			±1/2			±1/2	LSB
T_{min} to T_{max}			±1			±1/2			±1	LSB
DIFFERENTIAL LINEARITY ERROR (Minimum resolution for which no missing codes are guaranteed)										
25°C	11			12			12			Bits
T_{min} to T_{max}	11			12			12			Bits
UNIPOLAR OFFSET (max) (Adjustable to zero)			±2			±2			±2	LSB
BIPOLAR OFFSET (max) (Adjustable to zero)			±10			±4			±4	LSB
FULL SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF OUT TO REF IN)										
(Adjustable to zero) 25°C (max)			0.25			0.25			0.25	% of F.S.
T_{min} to T_{max} (Without Initial Adjustment)		0.47			0.37			0.30		% of F.S.
(With Initial Adjustment)		0.22			0.12			0.05		% of F.S.
TEMPERATURE RANGE	0		+70	0		+70	0		+70	°C
TEMPERATURE COEFFICIENTS (Using internal reference) T_{min} to T_{max}										
Unipolar Offset			±2			±1			±1	LSB
			10			5			5	ppm/°C
Bipolar Offset			±2			±1			±1	LSB
			10			5			5	ppm/°C
Full Scale Calibration			±9			±5			±2	LSB
			50			27			10	ppm/°C
POWER SUPPLY REJECTION Max change in Full Scale Calibration										
$+13.5 \le V_{CC} \le +16.5V$ or $-11.4V \le V_{CC} \le -12.6V$			±2			±1			±1	LSB
$+4.5 \le V_{LOGIC} \le +5.5V$			±1/2			±1/2			±1/2	LSB
$-16.5 \le V_{EE} \le -13.5V$ or $-12.6V \le V_{EE} \le -11.4V$			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar		−5 to +5			−5 to +5			−5 to +5		Volts
		−10 to +10			−10 to +10			−10 to +10		Volts
Unipolar		0 to +10			0 to +10			0 to +10		Volts
		0 to +20			0 to +20			0 to +20		Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
POWER SUPPLIES										
Operating Range										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−11.4		−16.5	−11.4		−16.5	−11.4		−16.5	Volts
Operating Current										
I_{LOGIC}		30	40		30	40		30	40	mA
I_{CC}		2	5		2	5		2	5	mA
I_{EE}		18	30		18	30		18	30	mA
POWER DISSIPATION		390	725		390	725		390	725	mW
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1	9.9	10.0	10.1	Volts
Output current (available for external loads, *External load should not change during conversion.)			1.5*			1.5*			1.5*	mA
PACKAGE OPTION[2] (D28A) – Ceramic DIP		AD574AJD			AD574AKD			AD574ALD		

NOTES
[1] The reference should be buffered for operation on ±12V supplies.
[2] See Section 19 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD574AS Min	AD574AS Typ	AD574AS Max	AD574AT Min	AD574AT Typ	AD574AT Max	AD574AU Min	AD574AU Typ	AD574AU Max	Units
RESOLUTION			12			12			12	Bits
LINEARITY ERROR										
25°C (max)			±1			±1/2			±1/2	LSB
T_{min} to T_{max}			±1			±1/2			±1	LSB
DIFFERENTIAL LINEARITY ERROR (Minumum resolution for which no missing codes are guaranteed)										
25°C	11			12			12			Bits
T_{min} to T_{max}	11			12			12			Bits
UNIPOLAR OFFSET (max) (Adjustable to zero)			±2			±2			±2	LSB
BIPOLAR OFFSET (max) (Adjustable to zero)			±10			±4			±4	LSB
FULL SCALE CALIBRATION ERROR (with fixed 50Ω resistor from REF OUT TO REF IN)										
(Adjustable to zero) 25°C (max)			0.25			0.25			0.25	% of F.S.
T_{min} to T_{max} (Without Initial Adjustment)		0.75			0.5			0.37		% of F.S.
(With Initial Adjustment)		0.5			0.25			0.12		% of F.S.
TEMPERATURE RANGE	−55		+125	−55		+125	−55		+125	°C
TEMPERATURE COEFFICIENTS (Using internal reference) T_{min} to T_{max}										
Unipolar Offset			±2			±1			±1	LSB
			5			2.5			2.5	ppm/°C
Bipolar Offset			±4			±2			±1	LSB
			10			5			2.5	ppm/°C
Full Scale Calibration			±20			±10			±5	LSB
			50			25			12.5	ppm °C
POWER SUPPLY REJECTION										
Max change in Full Scale Calibration										
$+13.5 \le V_{CC} \le +16.5V$ or $+11.4V \le V_{CC} \le +12.6V$			±2			±1			±1	LSB
$+4.5 \le V_{LOGIC} \le +5.5V$			±1/2			±1/2			±1/2	LSB
$-16.5 \le V_{EE} \le -13.5V$ or $-12.6V \le V_{EE} \ge -11.4V$			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar		−5 to +5			−5 to +5			−5 to +5		Volts
		−10 to +10			−10 to +10			−10 to +10		Volts
Unipolar		0 to +10			0 to +10			0 to +10		Volts
		0 to +20			0 to +20			0 to +20		Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
POWER SUPPLIES										
Operating Range										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	−11.4		−16.5	−11.4		−16.5	−11.4		−16.5	Volts
Operating Current										
I_{LOGIC}		30	40		30	40		30	40	mA
I_{CC}		2	5		2	5		2	5	mA
I_{EE}		18	30		18	30		18	30	mA
POWER DISSIPATION		390	725		390	725		390	725	mW
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1	9.9	10.0	10.1	Volts
Output current (available for external loads, (External load should not change during conversion)			1.5[1]			1.5[1]			1.5	mA
PACKAGE OPTION[2]										
D (D28A) – Ceramic DIP		AD574ASD			AD574ATD			AD574AUD		

NOTES

[1] The reference should be buffered for operation on ±12V supplies.

[2] See Section 19 for package outline information.

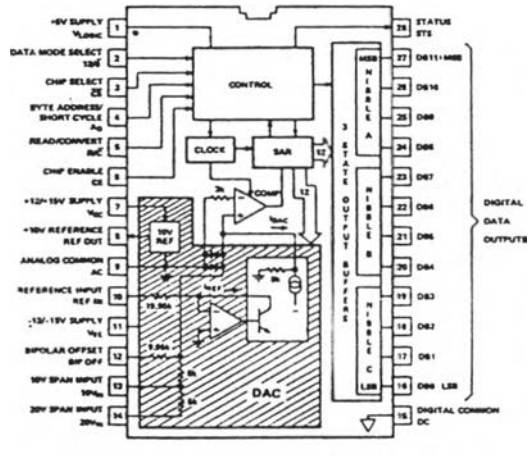
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed. Although only those shown in boldface are tested on all production units.

DIGITAL CHARACTERISTICS[1] (All grades, T_{min} – T_{max})

	Min	Typ	Max	
Logic Inputs[2] (CE, $\overline{CS}$, R/$\overline{C}$, A_0)				
Voltages				
Logic "1"	+2.0V		+5.5V	
Logic "0"	−0.5V		+0.8V	
Current	−50μA		+50μA	
Capacitance		5pF		
Logic Outputs (DB11–DB0, STS)				
Logic "0"			+0.4V	$I_{SINK} \leq 1.6mA$
Logic "1"	2.4V			$I_{SOURCE} \leq 500\mu A$
Leakage (When in high-Z state)	−40μA		+40μA	DB11 – DB0 Only
Capacitance		5pF		

[1]Detailed Timing Specifications appear in the Digital Interface Section.
[2]12/$\overline{8}$ Input is not TTL-compatible and must be hard-wired to V_{LOGIC} or DIGITAL COMMON.



AD574A Block Diagram and Pin Configuration

ABSOLUTE MAXIMUM RATINGS
(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common . . . . . 0 to +16.5V
V_{EE} to Digital Common . . . . . 0 to −16.5V
V_{LOGIC} to Digital Common . . . . . 0 to +7V
Analog Common to Digital Common . . . . . ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to
Digital Common . . −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to
Analog Common . . . . . ±16.5V
$20V_{IN}$ to Analog Common . . . . . ±24V
REF OUT . . . . . Indefinite short to common
Momentary short to V_{CC}
Chip Temperature (J, K, L grades) . . . . . 100°C
(S, T, U grades) . . . . . 150°C
Power Dissipation 1000mW
Lead Temperature, Soldering . . . . . 300°C, 10 sec.
Storage Temperature . . . . . −65°C to +150°C
Thermal Resistance, θ_{JA} . . . . . 60°C/W

AD574A ORDERING GUIDE

Model	Temp. Range	Linearity Error Max (T_{min} to T_{max})	Resolution No Missing Codes (T_{min} to T_{max})	Max Full Scale T.C. (ppm/°C)
AD574AJD	0 to +70°C	±1LSB	11 Bits	50.0
AD574AKD	0 to +70°C	±1/2LSB	12 Bits	27.0
AD574ALD	0 to +70°C	±1/2LSB	12 Bits	10.0
AD574ASD	−55°C to +125°C	±1LSB	11 Bits	50.0
AD574ATD	−55°C to +125°C	±1LSB	12 Bits	25.0
AD574AUD	−55°C to +125°C	±1LSB	12 Bits	12.5

THE AD574A OFFERS GUARANTEED MAXIMUM LINEARITY ERROR OVER THE FULL OPERATING TEMPERATURE RANGE

DEFINITIONS OF SPECIFICATIONS

LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The AD574AK, AL, AT, and AU grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The AD574AJ and AS grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the AD574AK, AL, AT, and AU grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The AD574AJ and AS grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following two pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT–JUSTIFIED DATA

The data format used in the AD574A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1 1/2LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 3 and 4. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

10

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

POWER SUPPLY REJECTION

The standard specifications for the AD574A assume use of −5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

CIRCUIT OPERATION

The AD574A is a complete 12-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD574A is shown in Figure 1. The device consists of two chips, one containing the precision 12-bit DAC with voltage reference, the other containing the comparator, successive-approximation register, clock, output buffers and control circuitry.

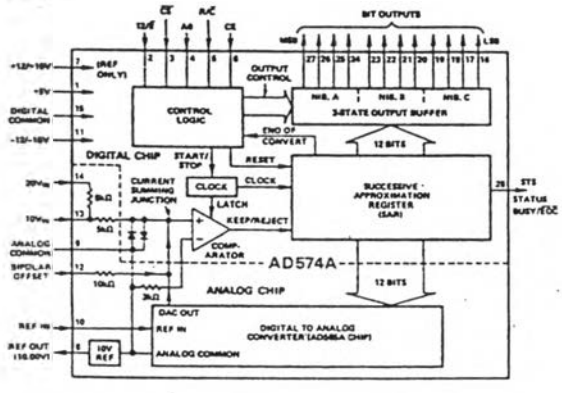


Figure 1. Block Diagram of AD574A 12-Bit A-to-D Converter

When the control section is commanded to initiate a conversion (as described later), it then enables the clock and resets the successive-approximation register (SAR) to all zeros. Once a conversion cycle has begun, it cannot be stopped or re-started and data is not available from the output buffers. The SAR, timed by the clock, will then sequence through the conversion cycle and return an end-of-convert flag to the control section. The control section will then disable the clock, bring the output status flag low, and enable control functions to allow data read functions by external command.

During the conversion cycle, the internal 12-bit current output DAC is sequenced by the SAR from the most-significant-bit (MSB) to least-significant-bit (LSB) to provide an output current which accurately balances the input signal current through the 5kΩ (or 10kΩ) input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±½LSB.

The temperature-compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The reference is trimmed to 10.00 volts ± 1%; it can supply up to 1.5mA to an external load in addition to that required to drive the reference input resistor (0.5mA) and bipolar offset resistor (1mA) when the AD574A is powered from ±15V supplies. If the AD574A is used with ±12V supplies, or if external current must be supplied over the full temperature range, an external buffer amplifier is recommended. Any external load on the AD574A reference must remain constant during conversion. The thin film application resistors are trimmed to match the full scale output current of the DAC. There are two 5kΩ input scaling resistors to allow either a 10 volt or 20 volt span. The 10kΩ bipolar offset resistor is grounded for unipolar operation or connected to the 10 volt reference for bipolar operation.

DRIVING THE AD574A ANALOG INPUT

The AD574A is a successive-approximation type analog-to-digital converter. During the conversion cycle, the ADC input current is modulated by the DAC test current at approximately a 500kHz rate. Thus it is important to recognize that the signal source driving the AD574A must be capable of holding a constant output voltage under dynamically-changing load conditions.

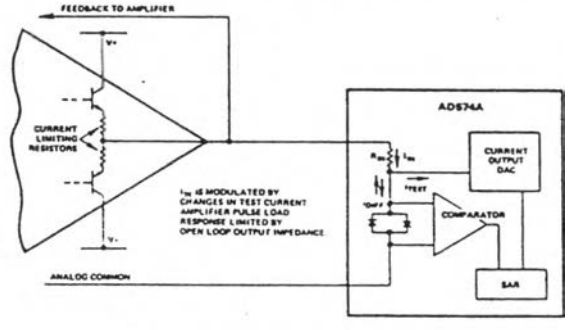


Figure 2. Op Amp – AD574A Interface

The closed loop output impedance of an op amp is equal to the open loop output impedance (usually a few hundred ohms) divided by the loop gain at the frequency of interest. It is often assumed that the loop gain of a follower-connected op amp is sufficiently high to reduce the closed loop output impedance to a negligibly small value, particularly if the signal is low frequency. However, the amplifier driving an AD574A must either have sufficient loop gain at 500kHz to reduce the closed loop output impedance to a low value or have low open loop output impedance.

This can be accomplished either by using a wideband op amp or by placing a discrete-transistor or integrated buffer inside the amplifier's feedback loop.

SUPPLY DECOUPLING AND LAYOUT CONSIDERATIONS

It is critically important that the AD574A power supplies be filtered, well-regulated, and free from high frequency noise. Use of noisy supplies will cause unstable output codes to be generated. Switching power supplies are not recommended for circuits attempting to achieve 12-bit accuracy unless great care is used in filtering any switching spikes present in the output. Remember that a few millivolts of noise represents several counts of error in a 12-bit ADC.

Decoupling capacitors should be used on all power supply pins; the +5V supply decoupling capacitor should be connected directly from pin 1 to pin 15 (digital common) and the $-V_{EE}$ and $-V_{EE}$ pins should be decoupled directly to analog common (pin 9). A suitable decoupling capacitor is a 47μF tantalum type in parallel with a 0.1μF disc ceramic type.

Circuit layout should attempt to locate the AD574A, associated analog input circuitry, and interconnections as far as possible from logic circuitry. For this reason, the use of wire-wrap circuit construction is not recommended. Careful printed-circuit construction is preferred.

AD574A Analog Circuit Details

UNIPOLAR RANGE CONNECTIONS FOR THE AD574A

The AD574A contains all the active components required to perform a complete 12-bit A/D conversion. Thus, for most situations, all that is necessary is connection of the power supplies (+5, +12/+15 and −12/−15 volts), the analog input, and the conversion initiation command, as discussed on the next page. Analog input connections and calibration are easily accomplished; the unipolar operating mode is shown in Figure 4.

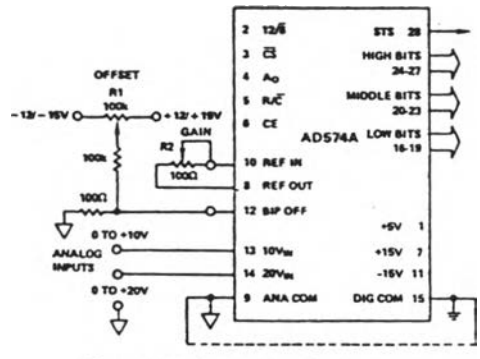


Figure 3. Unipolar Input Connections

All of the thin film application resistors of the AD574A are trimmed for absolute calibration. Therefore, in many applications, no calibration trimming will be required. The absolute accuracy for each grade is given in the specification tables. For example, if no trims are used, the AD574AK guarantees ±2LSB max zero offset error and ±0.25% (10LSB) max full scale error. (Typical full scale error is ±2LSB.) If the offset trim is not required, pin 12 can be connected directly to pin 9; the two resistors and trimmer for pin 12 are then not needed. If the full scale trim is not needed, a 50Ω ±1% metal film resistor should be connected between pin 8 and pin 10.

The analog input is connected between pin 13 and pin 9 for a 0 to +10V input range, between 14 and pin 9 for a 0 to +20V input range. The AD574A easily accommodates an input signal beyond the supplies. For the 10 volt span input, the LSB has a nominal value of 2.44mV, for the 20 volt span, 4.88mV. If a 10.24V range is desired (nominal 2.5mV/bit), the gain trimmer (R2) should be replaced by a 50Ω resistor, and a 200Ω trimmer inserted in series with the analog input to pin 13 (for a full scale range of 20.48V (5mV/bit), use a 500Ω trimmer into pin 14). The gain trim described below is now done with these trimmers. The nominal input impedance into pin 13 is 5kΩ, and 10kΩ into pin 14

UNIPOLAR CALIBRATION

The AD574A is intended to have a nominal ½LSB offset so that the exact analog input for a given code will be in the middle of that code 'halfway between the transitions to the codes above and below it). Thus, when properly calibrated, the first transition (from 0000 0000 0000 to 0000 0000 0001) will occur for an input level of +1/2LSB (1.22mV for 10V range).

If pin 12 is connected to pin 9, the unit typically will behave in this manner, within specifications. If the offset trim (R1) is used, it should be trimmed as above, although a different offset can be set for a particular system requirement. This circuit will give approximately ±15mV of offset trim range.

The full scale trim is done by applying a signal 1 1/2LSB below the nominal full scale (9.9963 for a 10V range). Trim R2 to give the last transition (1111 1111 1110 to 1111 1111 1111).

BIPOLAR OPERATION

The connections for bipolar ranges are shown in Figure 4. Again, as for the unipolar ranges, if the offset and gain specifications are sufficient, one or both of the trimmers shown can be replaced by a 50Ω ±1% fixed resistor. The analog input is applied as for the unipolar ranges. Bipolar calibration is similar to unipolar calibration. First, a signal ½LSB above negative full scale (−4.9988V for the ±5V range) is applied and R1 is trimmed to give the first transition (0000 0000 0000 to 0000 0000 0001). Then a signal 1½LSB below positive full scale (+4.9963V for the ±5V range) is applied and R2 trimmed to give the last transition (1111 1111 1110 to 1111 1111 1111).

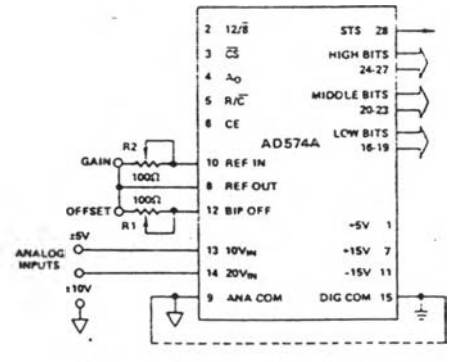


Figure 4. Bipolar Input Connections

GROUNDING CONSIDERATIONS

The analog common at pin 9 is the ground reference point for the internal reference and is thus the "high quality" ground for the AD574A; it should be connected directly to the analog reference point of the system. In order to achieve all of the high accuracy performance available from the AD574A in an environment of high digital noise content, it is required that the analog and digital commons be connected together at the package. In some situations, the digital common at pin 15 can be connected to the most convenient ground reference point; analog power return is preferred.

CONVERSION START/DATA READ CONTROL LOGIC

The AD574A contains on-chip logic to provide conversion initiation and data read operations from signals commonly available in microprocessor systems. Figure 5 shows the internal logic circuitry of the AD574A.

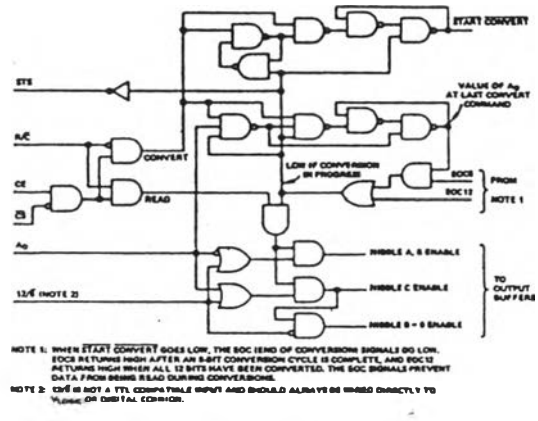


Figure 5. AD574A Control Logic

The control signals CE, $\overline{CS}$, and R/$\overline{C}$ control the operation of the converter. The state of R/$\overline{C}$ when CE and $\overline{CS}$ are both asserted determines whether a data read (R/$\overline{C}$ = 1) or a convert (R/$\overline{C}$ = 0) is in progress. The register control inputs A_0 and 12/$\overline{8}$ control conversion length and data format. The A_0 line is usually tied to the least significant bit of the address bus. If a conversion is started with A_0 low, a full 12-bit conversion cycle is initiated. If A_0 is high during a convert start, a shorter 8-bit conversion cycle results. During data-read operations, A_0 determines whether the three-state buffers containing the 8 MSBs of the conversion result (A_0 = 0) or the 4 LSBs (A_0 = 1) are enabled. The 12/$\overline{8}$ pin determines whether the output data is to be organized as two 8-bit words (12/$\overline{8}$ tied to DIGITAL COMMON) or a single 12-bit word (12/$\overline{8}$ tied to VLOGIC). The 12/$\overline{8}$ pin is not TTL-compatible and must be hard-wired to either VLOGIC or DIGITAL COMMON. In the 8-bit mode, the byte addressed when A_0 is high contains the 4 LSBs from the conversion followed by four trailing zeroes. This organization allows the data lines to be overlapped for direct interface to 8-bit buses without the need for external three-state buffers.

It is not recommended that A_0 change state during a data read operation. Asymmetrical enable and disable times of the three-state buffers could cause internal bus contention resulting in potential damage to the AD574A.

An output signal, STS, indicates the status of the converter. STS goes high at the beginning of a conversion and returns low when the conversion cycle is complete.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-Bit Conversion
1	0	0	X	1	Initiate 8-Bit Conversion
1	0	1	Pin 1	X	Enable 12-Bit Parallel Output
1	0	1	Pin 15	0	Enable 8 Most Significant Bits
1	0	1	Pin 15	1	Enable 4LSBs + 4 Trailing Zeroes

Table I. AD574A Truth Table

TIMING

The AD574A is easily interfaced to a wide variety of microprocessors and other digital systems. Discussion of the timing requirements of the AD574A control signals will provide the system designer with useful insight into the operation of the device.

Figure 6 shows a complete timing diagram for the AD574A convert start operation. R/$\overline{C}$ should be low before both CE and $\overline{CS}$ are asserted; if R/$\overline{C}$ is high, a read operation will momentarily occur, possibly resulting in system bus contention. Either CE or $\overline{CS}$ may be used to initiate a conversion. As shown in Figure 6,

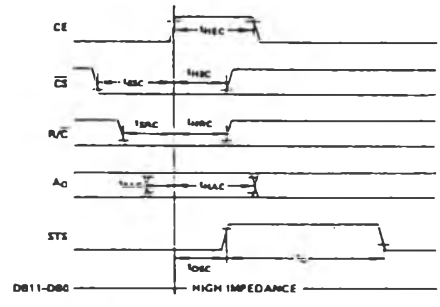


Figure 6. Convert Start Timing

CE is used. If $\overline{CS}$ is used to trigger conversion or if the specified set-up times are not met, appropriately longer pulses are necessary (to provide at least 200ns when R/$\overline{C}$, CE, and $\overline{CS}$ are all valid). Note that CE includes one less propagation delay than $\overline{CS}$ and is therefore the faster input.

Once a conversion is started and the STS line goes high, convert start commands will be ignored until the conversion cycle is complete. The output data buffers cannot be enabled during conversion.

CONVERT START TIMING – FULL CONTROL MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DSC}	STS Delay from CE			300	ns
t_{HEC}	CE Pulse Width	300			ns
t_{SSC}	$\overline{CS}$ to CE Setup	300			ns
t_{HSC}	$\overline{CS}$ Low During CE High	200			ns
t_{SRC}	R/$\overline{C}$ to CE Setup	250			ns
t_{HRC}	R/$\overline{C}$ Low During CE High	200			ns
t_{SAC}	A_0 to CE Setup	0			ns
t_{HAC}	A_0 Valid During CE High	300			ns
t_C	Conversion Time				
	8-Bit Cycle	10		24	µs
	12-Bit Cycle	15		35	µs

Figure 7 shows the timing for data read operations. The AD574A differs from the original AD574 design in that the three-state output buffers feature faster access time and shorter data latency

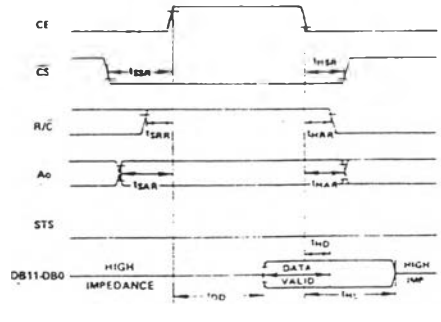


Figure 7. Read Cycle Timing

times. This speed improvement simplifies the interface to faster microprocessors. During data read operations, access time is measured from the point where CE and R/$\overline{C}$ both are high (assuming $\overline{CS}$ is already low). If $\overline{CS}$ is used to enable the device, access time is extended by 100ns.

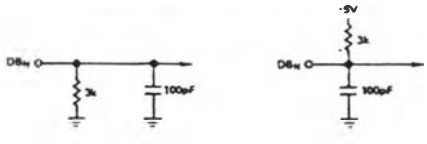
In the 8-bit bus interface mode (12/$\overline{8}$ input wired to DIGITAL COMMON), the address bit, A_0, must be stable at least 150ns prior to $\overline{CE}$ going high and must remain stable during the entire read cycle. If A_0 is allowed to change, damage to the AD574A output buffers may result.

READ TIMING – FULL CONTROL MODE

Symbol	Parameter	Min	Typ	Max	Units
t_{DD}[1]	Access Time (from CE)		210	250	ns
t_{HD}	Data Valid after CE Low	25			ns
t_{HL}[2]	Output Float Delay		110	150	ns
t_{CSR}	$\overline{CS}$ to CE Setup	150			ns
t_{SAR}	R/$\overline{C}$ to CE Setup	0			ns
t_{AAR}	A_0 to CE Setup	150			ns
t_{HSR}	$\overline{CS}$ Valid After CE Low	50			ns
t_{HDR}	R/$\overline{C}$ High After CE Low	0			ns
t_{HAR}	A_0 Valid After CE low	50			ns

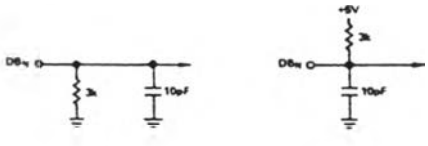
[1] t_{DD} is measured with the load circuit of Figure 8 and defined as the time required for an output to cross 0.4V or 2.4V.

[2] t_{HL} is defined as the time required for the data lines to change 0.5V when loaded with the circuit of Figure 9.



a. High-Z to Logic 1 b. High-Z to Logic 0

Figure 8. Load Circuit for Access Time Test



a. Logic 1 to High-Z b. Logic 0 to High-Z

Figure 9. Load Circuit for Output Float Delay Test

"STAND-ALONE" OPERATION

The AD574A can be used in a "stand-alone" mode, which is useful in systems with dedicated input ports available and thus not requiring full bus interface capability.

In this mode, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and conversion is controlled by R/$\overline{C}$. The three-state buffers are enabled when R/$\overline{C}$ is high and a conversion starts when R/$\overline{C}$ goes low. This gives rise to two possible control signals–a high pulse or a low pulse. Operation with a low pulse is shown in Figure 10. In this case, the outputs are forced into the high-impedance state in response to the falling edge of R/$\overline{C}$ and return to valid logic levels after the conversion cycle is completed. The STS line goes high 500ns after R/$\overline{C}$ goes low and returns low 300ns after data is valid.

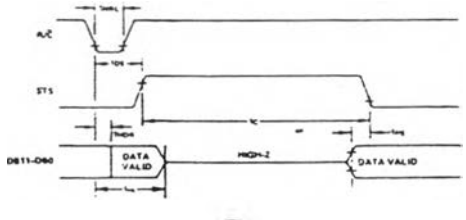


Figure 10. Low Pulse for R/$\overline{C}$ – Outputs Enabled After Conversion

If conversion is initiated by a high pulse as shown in Figure 11, the data lines are enabled during the time when R/$\overline{C}$ is high. The falling edge of R/$\overline{C}$ starts the next conversion and the data lines return to three-state (and remain three-state) until the next high pulse of R/$\overline{C}$.

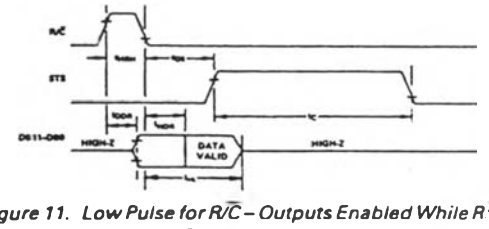


Figure 11. Low Pulse for R/$\overline{C}$ – Outputs Enabled While R/$\overline{C}$ High, Otherwise High-Z

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	350			ns
t_{DS}	STS Delay from R/$\overline{C}$			500	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HL}	Output Float Delay		110	150	ns
t_{HS}	STS Delay After Data Valid	300		1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	250			ns
t_{DDR}	Data Access Time			250	ns

INTERFACING THE AD574A TO MICROPROCESSORS

The control logic of the AD574A makes direct connection to most microprocessor system buses possible. While it is impossible to describe the details of the interface connections for every microprocessor type, several representative examples will be described here.

GENERAL A/D CONVERTER INTERFACE CONSIDERATIONS

Analog-to-digital converters, like any I/O device, may be interfaced to microprocessors by several methods. These methods include (but are not limited to) direct memory access, isolated or accumulator I/O, and memory-mapped I/O. Direct memory access (DMA) is the fastest, since conversions occur automatically and data updates into memory are transparent to the processor. DMA logic is very processor-dependent and makes use of dedicated specialized hardware.

Memory-mapped and accumulator I/O are more often used and somewhat easier to understand. Memory-mapped I/O assigns the I/O device to one or more locations in the memory space of the microprocessor. This technique has the advantage that the full range of memory reference instructions may be used to operate on the data. The potential disadvantages include limiting the memory space available for program and data memory, somewhat more complex address decoding and more difficult isolation of device select pulses for system debugging. Many processors offer only memory-mapped I/O.

Accumulator I/O uses a set of control signals which are distinct and different from the memory control signals. These control signals, combined with the address bus, serve to define a totally

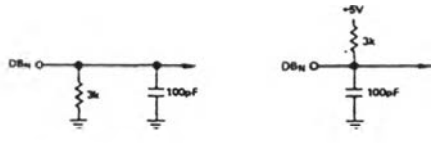
times. This speed improvement simplifies the interface to faster microprocessors. During data read operations, access time is measured from the point where CE and R/$\overline{C}$ both are high (assuming $\overline{CS}$ is already low). If $\overline{CS}$ is used to enable the device, access time is extended by 100ns.

In the 8-bit bus interface mode (12/$\overline{8}$ input wired to DIGITAL COMMON), the address bit, A_0, must be stable at least 150ns prior to $\overline{CE}$ going high and must remain stable during the entire read cycle. If A_0 is allowed to change, damage to the AD574A output buffers may result.

READ TIMING – FULL CONTROL MODE

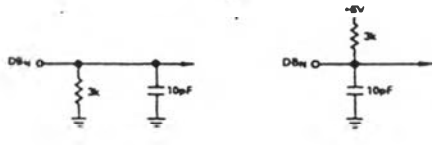
Symbol	Parameter	Min	Typ	Max	Units
t_{DD}[1]	Access Time (from CE)		210	250	ns
t_{HD}	Data Valid after CE Low	25			ns
t_{HL}[2]	Output Float Delay		110	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup	150			ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0			ns
t_{SAR}	A_0 to CE Setup	150			ns
t_{HSR}	$\overline{CS}$ Valid After CE Low	50			ns
t_{HRR}	R/$\overline{C}$ High After CE Low	0			ns
t_{HAR}	A_0 Valid After CE low	50			ns

[1] t_{DD} is measured with the load circuit of Figure 8 and defined as the time required for an output to cross 0.4V or 2.4V.
[2] t_{HL} is defined as the time required for the data lines to change 0.5V when loaded with the circuit of Figure 9.



a. High-Z to Logic 1 *b. High-Z to Logic 0*

Figure 8. Load Circuit for Access Time Test



a. Logic 1 to High-Z *b. Logic 0 to High-Z*

Figure 9. Load Circuit for Output Float Delay Test

"STAND-ALONE" OPERATION

The AD574A can be used in a "stand-alone" mode, which is useful in systems with dedicated input ports available and thus not requiring full bus interface capability.

In this mode, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and conversion is controlled by R/$\overline{C}$. The three-state buffers are enabled when R/$\overline{C}$ is high and a conversion starts when R/$\overline{C}$ goes low. This gives rise to two possible control signals–a high pulse or a low pulse. Operation with a low pulse is shown in Figure 10. In this case, the outputs are forced into the high-impedance state in response to the falling edge of R/$\overline{C}$ and return to valid logic levels after the conversion cycle is completed. The STS line goes high 500ns after R/$\overline{C}$ goes low and returns low 300ns after data is valid.

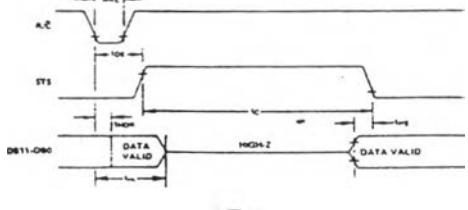


Figure 10. Low Pulse for R/$\overline{C}$ – Outputs Enabled After Conversion

If conversion is initiated by a high pulse as shown in Figure 11, the data lines are enabled during the time when R/$\overline{C}$ is high. The falling edge of R/$\overline{C}$ starts the next conversion and the data lines return to three-state (and remain three-state) until the next high pulse of R/$\overline{C}$.

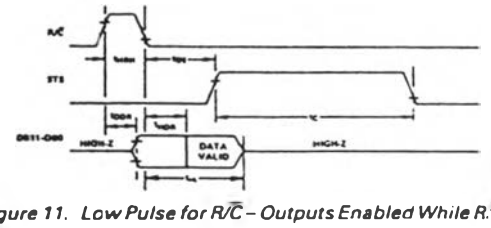


Figure 11. Low Pulse for R/$\overline{C}$ – Outputs Enabled While R/$\overline{C}$ High, Otherwise High-Z

STAND-ALONE MODE TIMING

Symbol	Parameter	Min	Typ	Max	Units
t_{HRL}	Low R/$\overline{C}$ Pulse Width	350			ns
t_{DS}	STS Delay from R/$\overline{C}$			500	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	25			ns
t_{HL}	Output Float Delay		110	150	ns
t_{HS}	STS Delay After Data Valid	300		1000	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	250			ns
t_{DDR}	Data Access Time			250	ns

INTERFACING THE AD574A TO MICROPROCESSORS

The control logic of the AD574A makes direct connection to most microprocessor system buses possible. While it is impossible to describe the details of the interface connections for every microprocessor type, several representative examples will be described here.

GENERAL A/D CONVERTER INTERFACE CONSIDERATIONS

Analog-to-digital converters, like any I/O device, may be interfaced to microprocessors by several methods. These methods include (but are not limited to) direct memory access, isolated or accumulator I/O, and memory-mapped I/O. Direct memory access (DMA) is the fastest, since conversions occur automatically and data updates into memory are transparent to the processor. DMA logic is very processor-dependent and makes use of dedicated specialized hardware.

Memory-mapped and accumulator I/O are more often used and somewhat easier to understand. Memory-mapped I/O assigns the I/O device to one or more locations in the memory space of the microprocessor. This technique has the advantage that the full range of memory reference instructions may be used to operate on the data. The potential disadvantages include limiting the memory space available for program and data memory, somewhat more complex address decoding and more difficult isolation of device select pulses for system debugging. Many processors offer only memory-mapped I/O.

Accumulator I/O uses a set of control signals which are distinct and different from the memory control signals. These control signals, combined with the address bus, serve to define a totally

separate I/O address space. This architecture is simpler from a hardware standpoint, since address decoding requirements are less severe and distinct I/O read and write pulses are more easily located for system debugging purposes. However, processors using accumulator I/O generally can only send data to an output device from the accumulator. This can make the software more cumbersome, since processor-controlled transfers of I/O device data to a memory location cannot be accomplished in a single instruction.

A typical A/D converter interface routine involves several operations. First, a write to the ADC address initiates a conversion. The processor must then wait for the conversion cycle to complete, since most integrated circuit ADCs take longer than one instruction cycle to complete a conversion. Valid data can, of course, only be read after the conversion is complete. The AD574A provides an output signal (STS) which indicates when a conversion is in progress. This signal can be polled by the processor by reading it through an external three-state buffer (or other input port). The STS signal can also be used to generate an interrupt upon completion of conversion, if the system timing requirements are critical (bear in mind that the maximum conversion time of the AD574A is only 35 microseconds) and the processor has other tasks to perform during the ADC conversion cycle. Another possible time-out method is to assume that the ADC will take 35 microseconds to convert, and insert a sufficient number of "do-nothing" instructions to ensure that 35 microseconds of processor time is consumed.

Once it is established that the converter is done with its cycle, the data can be read. In the case of an ADC of 8-bit resolution (or less), a single data read operation is sufficient. In the case of converters with more data bits than are available on the bus, a choice of data formats is required, and multiple read operations are needed. The AD574A includes internal logic to permit direct interface to 8-bit or 16-bit data buses, selected by connection of the 12/$\overline{8}$ input. In 16-bit bus applications (12/$\overline{8}$ high) the data lines (DB11 through DB0) may be connected to either the 12 most significant or 12 least significant bits of the data bus. The remaining four bits should be masked in software. The interface to an 8-bit data bus (12/$\overline{8}$ low) is done in a left-justified format. The even address (A0 low) contains the 8MSBs (DB11 through DB4). The odd address (A0 high) contains the 4LSBs (DB3 through DB0) in the upper half of the byte, followed by four trailing zeroes, thus eliminating bit masking instructions.

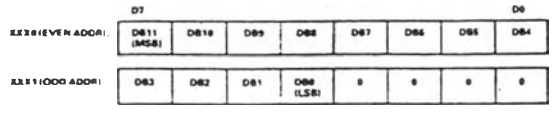


Figure 12. AD574A Data Format for 8-Bit Bus

It is not possible to rearrange the AD574A data lines for right-justified 8-bit bus interface.

The AD574A three-state buffers feature access times and data latency times comparable to presently-available memory devices. Therefore, the AD574A can interface directly to many processor buses without the need for wait states or external data buffers.

SPECIFIC PROCESSOR INTERFACE EXAMPLES

6800/6502-Type Systems

The control signals and bus architecture of the 6800 series and 6502 series microprocessors are very similar. In each, the state of the R/$\overline{W}$ signal at the rising edge of the Ø2 (or equivalent) clock establishes whether a memory read or write is in progress. The memory address being exercised is signaled by decoding the address bits to (usually) an active low signal.

This control structure is directly compatible with the AD574A. The R/$\overline{W}$ line can be used for R/$\overline{C}$, the active-low decoded base address (the AD574A occupies two memory locations) is applied to $\overline{CS}$, and Ø2 is used for CE. The least-significant address line ties to the AD574A A0 input.

In this interface, the processor can write to one address (A0 low) to start a full 12-bit conversion or another address (A0 high) to start a short 8-bit conversion. The contents of the data bus are meaningless during these writes. After sufficient time has passed for the conversion to complete, the processor can read the data in the two memory locations occupied by the AD574A. The even location (A0 low) contains the eight MSBs and the odd location contains the four LSBs and four trailing zeroes.

The AD574A may be used directly with 6800 series processors running at clock speeds up to 1.5MHz.

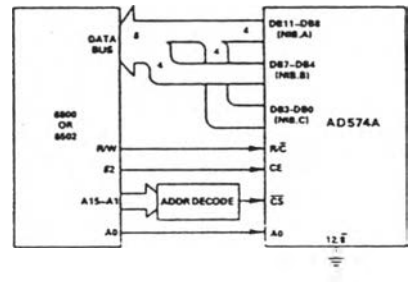


Figure 13. AD574A–6800/6502 Interface Connections

8085A Interface

The 8085A microprocessor uses a multiplexed address/data bus. At the beginning of a machine cycle, this bus contains the low byte of the address being exercised. The ALE output signal is available to strobe a latch to hold the low address byte. For the rest of the machine cycle, this bus carries data to or from the CPU.

The 8085A can use either accumulator I/O or memory-mapping for I/O devices. The system $\overline{RD}$ and $\overline{WR}$ are gated with IO/$\overline{M}$ to provide distinct I/O read and write signals and memory read and write signals. The control signals required for the AD574A are easily derived from the 8085A control bus. $\overline{CS}$ is taken from an address decoder on the high-order address bits. R/$\overline{C}$ can be taken from $\overline{WR}$ (either I/O write or memory write), A0 is tied to the LSB of the address bus, and CE is taken from the output of a NAND gate driven from $\overline{RD}$ and $\overline{WR}$. All bus access and float delay requirements are met for direct bus interface for 8085A clock rates up to 3MHz.

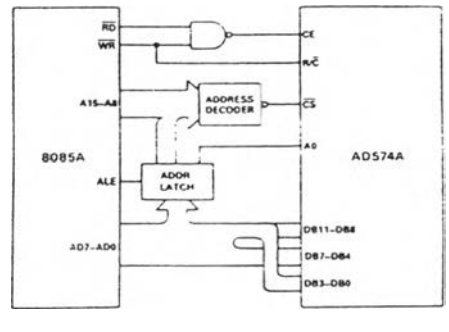


Figure 14. AD574A–8085A Direct Bus Interface

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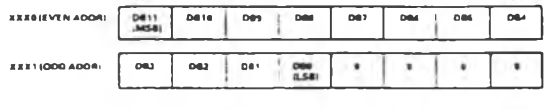

Figure 12. AD574A Data Format for 8-Bit Bus

It is not possible to rearrange the AD574A data lines for right-justified 8-bit bus interface.

The AD574A three-state buffers feature access times and data latency times comparable to presently-available memory devices. Therefore, the AD574A can interface directly to many processor buses without the need for wait states or external data buffers.

SPECIFIC PROCESSOR INTERFACE EXAMPLES

6800/6502-Type Systems

The control signals and bus architecture of the 6800 series and 6502 series microprocessors are very similar. In each, the state of the R/$\overline{W}$ signal at the rising edge of the ϕ2 (or equivalent) clock establishes whether a memory read or write is in progress. The memory address being exercised is signaled by decoding the address bits to (usually) an active low signal.

This control structure is directly compatible with the AD574A. The R/$\overline{W}$ line can be used for R/$\overline{C}$, the active-low decoded base address (the AD574A occupies two memory locations) is applied to $\overline{CS}$, and ϕ2 is used for CE. The least-significant address line ties to the AD574A A0 input.

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The AD574A may be used directly with 6800 series processors running at clock speeds up to 1.5MHz.

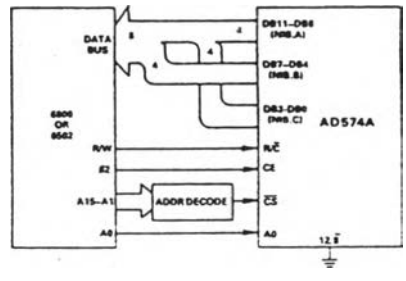

Figure 13. AD574A–6800 6502 Interface Connections

8085A Interface

The 8085A microprocessor uses a multiplexed address/data bus. At the beginning of a machine cycle, this bus contains the low byte of the address being exercised. The ALE output signal is available to strobe a latch to hold the low address byte. For the rest of the machine cycle, this bus carries data to or from the CPU.

The 8085A can use either accumulator I/O or memory-mapping for I/O devices. The system $\overline{RD}$ and $\overline{WR}$ are gated with IO/$\overline{M}$ to provide distinct I/O read and write signals and memory read and write signals. The control signals required for the AD574A are easily derived from the 8085A control bus. $\overline{CS}$ is taken from an address decoder on the high-order address bits. R/$\overline{C}$ can be taken from $\overline{WR}$ (either I/O write or memory write), A0 is tied to the LSB of the address bus, and CE is taken from the output of a NAND gate driven from $\overline{RD}$ and $\overline{WR}$. All bus access and float delay requirements are met for direct bus interface for 8085A clock rates up to 3MHz.

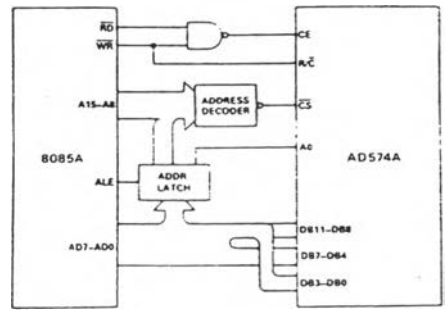

Figure 14. AD574A–8085A Direct Bus Interface

In 8085A systems running at high clock frequencies some external circuitry is required. First, the AD574A delay from CE going low to the data lines going into three-state will cause a bus conflict when the 8085A sends out the low byte of the next instruction address. This conflict will occur if the AD574A data outputs are tied directly to the 8085A bus. In systems where bus transceivers (e.g., 74LS245, 8286, etc.) are used to separate the address and data lines, the conflict is eliminated. The transceivers are disabled at the end of the read cycle and thus isolate the AD574A from the 8085A bus. Since most systems incorporate such buffers, this does not add to system complexity.

A second consideration when interfacing to higher speed 8085A systems is the width of the convert start pulse. The $\overline{WR}$ pulse from a 5MHz 8085A is only guaranteed to be 230 nanoseconds wide and is thus not long enough to initiate a conversion. There are two solutions to this problem. One possibility is to use a dual D-type flip-flop connected as shown in Figure 15 to insert a single wait state in read and write operations directed towards the AD574A. Another solution is to substitute the earlier-occurring S1 and S0 outputs from 8085A for $\overline{RD}$ and $\overline{WR}$ in the circuit of Figure 14 to generate the required control signals. It is important that bus transceivers be employed if S1 and S0 are used for control signals since these signals remain active longer than $\overline{RD}$ and $\overline{WR}$, enabling the AD574A output buffers in read operations for too long, causing potential bus conflicts.

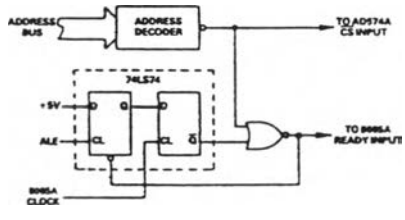

Figure 15. Wait State Generator for 5MHz 8085A Interface

Z-80 System Interface

The Z-80 series of 8-bit microprocessors, like the 8085A, offers both memory-mapped and accumulator I/O capability. While the 8085A only includes two instructions for accumulator I/O (IN and OUT), the Z-80 I/O instruction set is considerably more extensive.

The control signals available on the Z-80 include $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, and $\overline{WR}$. The $\overline{RD}$ and $\overline{WR}$ signals indicate direction of data flow while $\overline{MREQ}$ and $\overline{IORQ}$ determine whether the read or write cycle in progress is a memory or I/O cycle. During I/O reads and writes, only 8 address lines are active (as in the 8085A). An interesting feature of the Z-80 is that I/O read and write cycles are automatically extended by one clock cycle (one wait state is inserted) and are thus slower. The Z-80 control signal connections to the AD574A are identical to the 8085A connections.

The AD574A can be interfaced to Z-80 series processors with clock speeds up to 2.5MHz in the memory address space using the $\overline{MWR}$ and $\overline{MRD}$ signals. At higher clock rates (4 and 6MHz), the memory write pulse is not wide enough to properly start a conversion. The extra wait state added during I/O write operations will extend this pulse to a suitable width at clock rates up to 6MHz so that accumulator I/O is possible.

INTERFACING THE AD574A TO THE APPLE II COMPUTER

The AD574A can be used to provide a low-cost precision analog input port for the Apple II microcomputer without the need for additional power supplies or extensive digital interface logic. The AD574A can be mounted on a hobby card designed to plug into an Apple II I/O slot.

Hardware

All required supply voltages and control signals are available on the Apple's peripheral connectors. Each connector contains, on pin 41, a $\overline{DEVICE\ SELECT}$ output which is active when the address bus holds a hexadecimal address between C0n0 and C0nF, where n is equal to the slot number plus 8. This signal can be connected to pin 3 ($\overline{CS}$) of the AD574A. The Φ0 clock on pin 40 of the peripheral connector can be used for the AD574A CE input (pin 6). The AD574A R/$\overline{C}$ input (pin 5) can be driven directly by the R/$\overline{W}$ output available on peripheral connector pin 18. Pin 2 of the peripheral connector, A0, connects directly to the AD574A pin 4. The connections between the peripheral connector and the AD574A are shown in Figure 16.

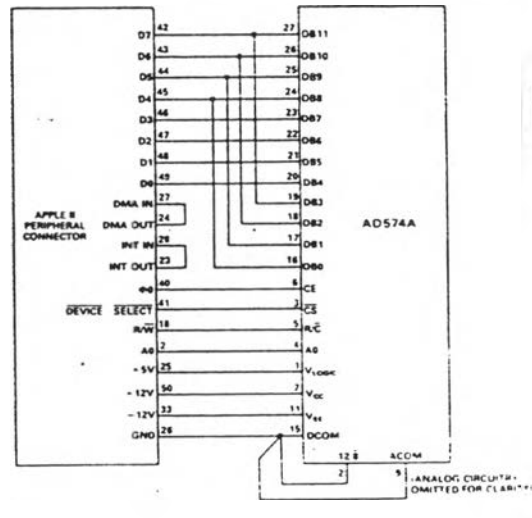

Figure 16. AD574A Connections to Apple II Peripheral Connector

The Apple II represents a relatively hostile electrical environment to the AD574A. The high frequency clocks radiate a large amount of noise which can be inadvertently coupled into analog signal lines. Furthermore, the switching power supply in the Apple is noisy, and this noise will often pollute the analog signals. It is possible, however, by judicious bypassing, decoupling, and ground management, to achieve a data acquisition system with only occasional flicker. A suggested grounding and decoupling scheme is shown in Figure 17.

It is recommended that any signal preamplification used in such a system be physically located outside the Apple cabinet. A full-scale signal range is less susceptible to electromagnetically coupled interference than a smaller signal range would be. Thus the preferred method is to deliver a buffered, high-level signal to the AD574A through a shielded cable. The ±5V or ±10V

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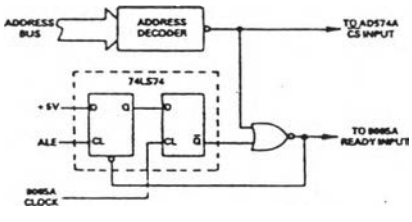

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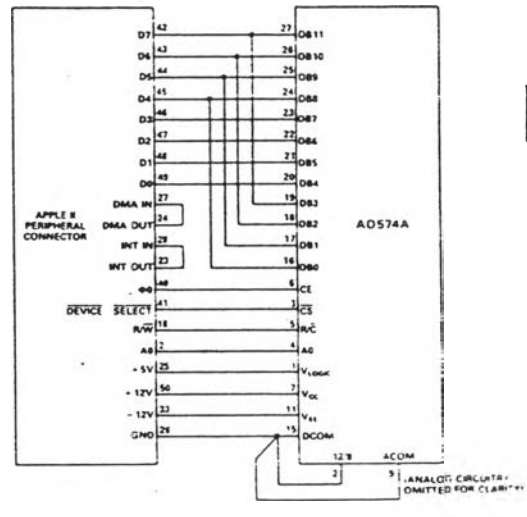

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EXAR

XR-2206

Monolithic Function Generator

GENERAL DESCRIPTION

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high-stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01 Hz to more than 1 MHz.

The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation. It has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 2000:1 frequency range, with an external control voltage, having a very small affect on distortion.

FEATURES

Low-Sine Wave Distortion	0.5%, Typical
Excellent Temperature Stability	20 ppm/°C, Typical
Wide Sweep Range	2000:1, Typical
Low-Supply Sensitivity	0.01%/V, Typical
Linear Amplitude Modulation	
TTL Compatible FSK Controls	
Wide Supply Range	10V to 26V
Adjustable Duty Cycle	1% to 99%

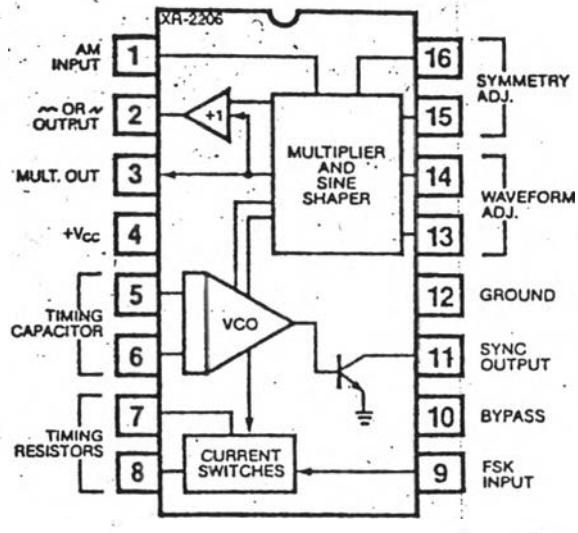
APPLICATIONS

Waveform Generation
Sweep Generation
AM/FM Generation
V/F Conversion
FSK Generation
Phase-Locked Loops (VCO)

ABSOLUTE MAXIMUM RATINGS

Power Supply	26V
Power Dissipation	750 mW
Derate Above 25°C	5 mW/°C
Total Timing Current	6 mA
Storage Temperature	−65°C to +150°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2206M	Ceramic	−55°C to +125°C
XR-2206N	Ceramic	0°C to +70°C
XR-2206P	Plastic	0°C to +70°C
XR-2206CN	Ceramic	0°C to +70°C
XR-2206CP	Plastic	0°C to +70°C

SYSTEM DESCRIPTION

The XR-2206 is comprised of four functional blocks; a voltage-controlled oscillator (VCO), an analog multiplier and sine-shaper; a unity gain buffer amplifier; and a set of current switches.

The VCO actually produces an output frequency proportional to an input current, which is produced by a resistor from the timing terminals to ground. The current switches route one of the timing pins current to the VCO controlled by an FSK input pin, to produce an output frequency. With two timing pins, two discrete output frequencies can be independently produced for FSK Generation Applications.

XR-2206

ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of Figure 1, $V^+ = 12V$, $T_A = 25°$, $C = 0.01\ \mu F$, $R_1 = 100\ k\Omega$, $R_2 = 10\ k\Omega$, $R_3 = 25\ k\Omega$ unless otherwise specified. S_1 open for triangle, closed for sine wave.

PARAMETERS	XR-2206M			XR-2206C			UNITS	CONDITIONS
	MIN	TYP	MAX	MIN	TYP	MAX		
GENERAL CHARACTERISTICS								
Single Supply Voltage	10		26	10		26	V	
Split-Supply Voltage	±5		±13	±5		±13	V	
Supply Current		12	17		14	20	mA	$R_1 \geq 10\ k\Omega$
OSCILLATOR SECTION								
Max. Operating Frequency	0.5	1		0.5	1		MHz	$C = 1000\ pF$, $R_1 = 1\ k\Omega$
Lowest Practical Frequency		0.01			0.01		Hz	$C = 50\ \mu F$, $R_1 = 2\ M\Omega$
Frequency Accuracy		±1	±4		±2		% of f_o	$f_o = 1/R_1C$
Temperature Stability		±10	±50		±20		ppm/°C	$0°C \leq T_A \leq 70°C$, $R_1 = R_2 = 20\ k\Omega$
Supply Sensitivity		0.01	0.1		0.01		%/V	$V_{LOW} = 10V$, $V_{HIGH} = 20V$, $R_1 = R_2 = 20\ k\Omega$
Sweep Range	1000:1	2000:1			2000:1		$f_H = f_L$	f_H @ $R_1 = 1\ k\Omega$, f_L @ $R_1 = 2\ M\Omega$
Sweep Linearity								
10:1 Sweep		2			2		%	$f_L = 1$ kHz, $f_H = 10$ kHz
1000:1 Sweep		8			8		%	$f_L = 100$ kHz, $f_H = 100$ kHz
FM Distortion		0.1			0.1		%	±10% Deviation
Recommended Timing Components								
Timing Capacitor: C	0.001		100	0.001		100	µF	See Figure 4.
Timing Resistors: R_1 & R_2	1		2000	1		2000	k Ω	
Triangle Sine Wave Output								See Note 1, Figure 2.
Triangle Amplitude		160			160		mV/k Ω	Figure 1, S_1 Open
Sine Wave Amplitude	40	60	80		60		mV/k Ω	Figure 1, S_1 Closed
Max. Output Swing		6			6		V p-p	
Output Impedance		600			600		Ω	
Triangle Linearity		1			1		%	
Amplitude Stability		0.5			0.5		dB	For 1000:1 Sweep
Sine Wave Amplitude Stability		4800			4800		ppm/°C	See Note 2.
Sine Wave Distortion								
Without Adjustment		2.5			2.5		%	$R_1 = 30\ k\Omega$
With Adjustment		0.4	1.0		0.5	1.5	%	See Figures 6 and 7.
Amplitude Modulation								
Input Impedance	50	100		50	100		k Ω	
Modulation Range		100			100		%	
Carrier Suppression		55			55		dB	
Linearity		2			2		%	For 95% modulation
Square-Wave Output								
Amplitude		12			12		V p-p	Measured at Pin 11.
Rise Time		250			250		nsec	$C_L = 10$ pF
Fall Time		50			50		nsec	$C_L = 10$ pF
Saturation Voltage		0.2	0.4		0.2	0.6	V	$I_L = 2$ mA
Leakage Current		0.1	20		0.1	100	µA	$V_{11} = 26V$
FSK Keying Level (Pin 9)	0.8	1.4	2.4	0.8	1.4	2.4	V	See section on circuit controls
Reference Bypass Voltage	2.9	3.1	3.3	2.5	3	3.5	V	Measured at Pin 10.

Note 1: Output amplitude is directly proportional to the resistance, R_3, on Pin 3. See Figure 2.
Note 2: For maximum amplitude stability, R_3 should be a positive temperature coefficient resistor.

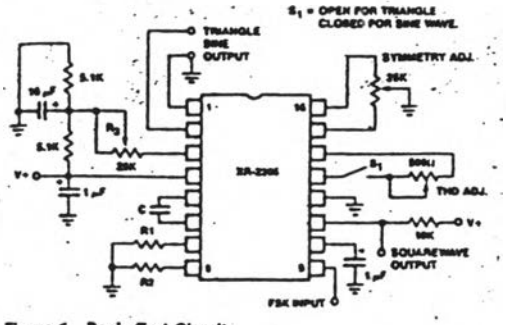


Figure 1. Basic Test Circuit.

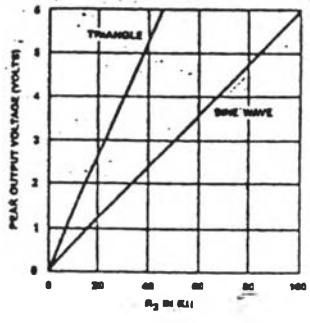


Figure 2. Output Amplitude as a Function of the Resistor, R_3, at Pin 3.

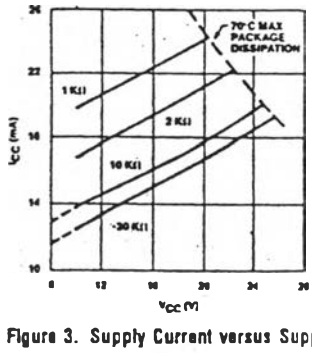


Figure 3. Supply Current versus Supply Voltage, Timing, R.

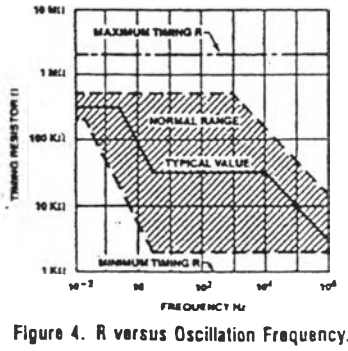


Figure 4. R versus Oscillation Frequency.

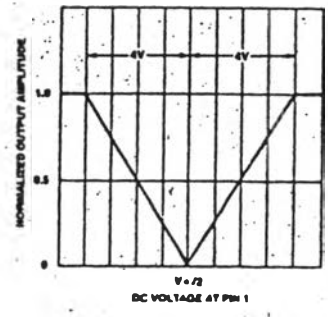


Figure 5. Normalized Output Amplitude versus DC Bias at AM Input (Pin 1).

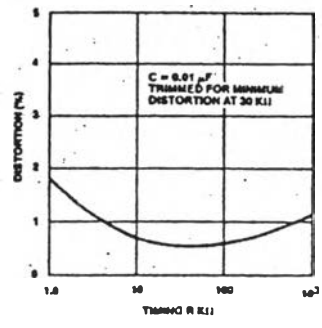


Figure 6. Trimmed Distortion versus Timing Resistor.

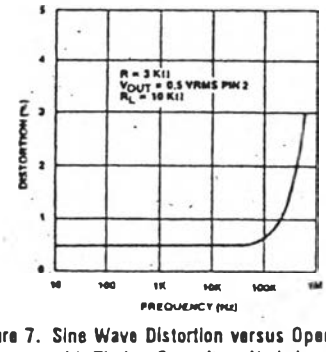


Figure 7. Sine Wave Distortion versus Operating Frequency with Timing Capacitors Varied.

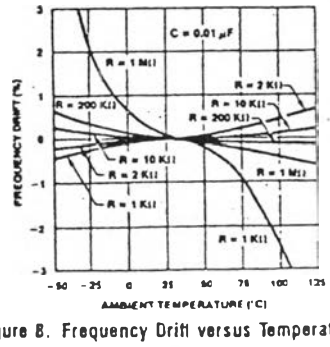


Figure 8. Frequency Drift versus Temperature.

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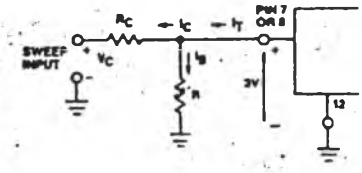


Figure 9. Circuit Connection for Frequency Sweep.

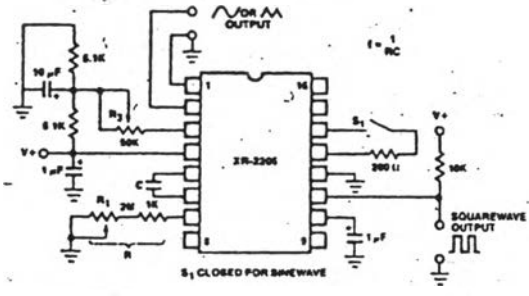


Figure 10. Circuit for Sine Wave Generation without External Adjustment. (See Figure 2 for Choice of R_3).

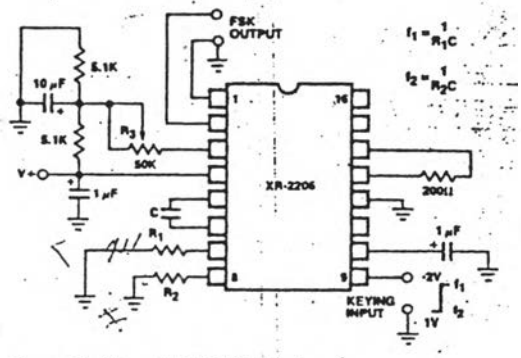


Figure 12. Sinusoidal FSK Generator.

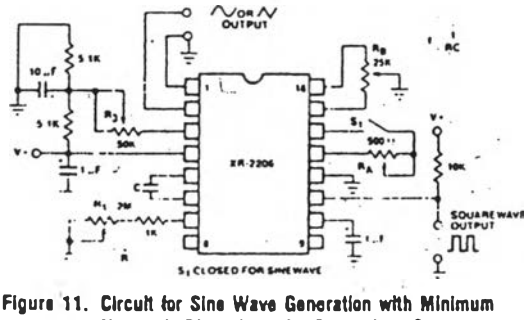


Figure 11. Circuit for Sine Wave Generation with Minimum Harmonic Distortion. (R_3 Determines Output Swing—See Figure 2.)

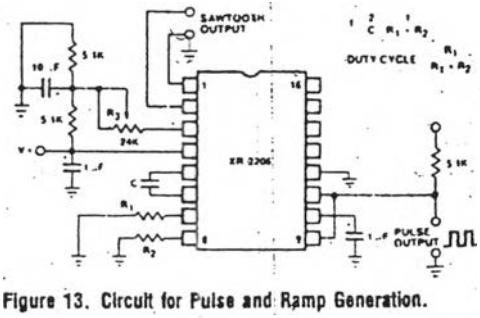


Figure 13. Circuit for Pulse and Ramp Generation.

Frequency-Shift Keying:

The XR-2206 can be operated with two separate timing resistors, R_1 and R_2, connected to the timing Pin 7 and 8, respectively, as shown in Figure 12. Depending on the polarity of the logic signal at Pin 9, either one or the other of these timing resistors is activated. If Pin 9 is open-circuited or connected to a bias voltage ≥ 2V, only R_1 is activated. Similarly, if the voltage level at Pin 9 is ≤1V, only R_2 is activated. Thus, the output frequency can be keyed between two levels, f_1 and f_2, as:

$$f_1 = 1/R_1C \text{ and } f_2 = 1/R_2C$$

For split-supply operation, the keying voltage at Pin 9 is referenced to V^-.

Output DC Level Control:

The dc level at the output (Pin 2) is approximately the same as the dc bias at Pin 3. In Figures 10, 11 and 12, Pin 3 is biased midway between V^+ and ground, to give an output dc level of $= V^+/2$.

APPLICATIONS INFORMATION

Sine Wave Generation

Without External Adjustment:

Figure 10 shows the circuit connection for generating a sinusoidal output from the XR-2206. The potentiometer, R_1 at Pin 7, provides the desired frequency tuning. The maximum output swing is greater than $V^+/2$, and the typical distortion (THD) is <2.5%. If lower sine wave distortion is desired, additional adjustments can be provided as described in the following section.

The circuit of Figure 10 can be converted to split-supply operation, simply by replacing all ground connections with V^-. For split-supply operation, R_3 can be directly connected to ground.

With External Adjustment:

The harmonic content of sinusoidal output can be reduced to ≈0.5% by additional adjustments as shown in Figure 11. The potentiometer, R_A, adjusts the sine-shaping resistor, and R_B provides the fine adjustment for the waveform symmetry. The adjustment procedure is as follows:

1. Set R_B at midpoint, and adjust R_A for minimum distortion.
2. With R_A set as above, adjust R_B to further reduce distortion.

Triangle Wave Generation

The circuits of Figures 10 and 11 can be converted to triangle wave generation, by simply open-circuiting Pin 13 and 14 (i.e., S_1 open). Amplitude of the triangle is approximately twice the sine wave output.

FSK Generation

Figure 12 shows the circuit connection for sinusoidal FSK signal operation. Mark and space frequencies can be independently adjusted, by the choice of timing resistors, R_1 and R_2; the output is phase-continuous during transitions. The keying signal is applied to Pin 9. The circuit can be converted to split-supply operation by simply replacing ground with V^-.

Pulse and Ramp Generation

Figure 13 shows the circuit for pulse and ramp waveform generation. In this mode of operation, the FSK keying terminal (Pin 9) is shorted to the square-wave output (Pin 11), and the circuit automatically frequency-shift keys itself between two separate frequencies during the positive-going and negative-going output waveforms. The pulse width and duty cycle can be adjusted from 1% to 99%, by the choice of R_1 and R_2. The values of R_1 and R_2 should be in the range of 1 kΩ to 2 MΩ.

PRINCIPLES OF OPERATION

Description of Controls

Frequency of Operation:

The frequency of oscillation, f_o, is determined by the external timing capacitor, C, across Pin 5 and 6, and by the timing resistor, R, connected to either Pin 7 or 8. The frequency is given as:

$$f_o = \frac{1}{RC} \text{ Hz}$$

and can be adjusted by varying either R or C. The recommended values of R, for a given frequency range, as shown in Figure 4. Temperature stability is optimum for 4 kΩ < R < 200 kΩ. Recommended values of C are from 1000 pF to 100 μF.

Frequency Sweep and Modulation:

Frequency of oscillation is proportional to the total timing current, I_T, drawn from Pin 7 or 8:

$$f = \frac{320\ I_T\ (\text{mA})}{C\ (\mu\text{F})} \text{ Hz}$$

Timing terminals (Pin 7 or 8) are low-impedance points, and are internally biased at +3V, with respect to Pin 12. Frequency varies linearly with I_T, over a wide range of current values, from 1 μA to 3 mA. The frequency can be controlled by applying a control voltage, V_C, to the activated timing pin as shown in Figure 9. The frequency of oscillation is related to V_C as:

$$f = \frac{1}{RC} 1 + \frac{R}{R_C}\left(1 - \frac{V_C}{3}\right) \text{ Hz}$$

XR-2206

where V_C is in volts. The voltage-to-frequency conversion gain, K, is given as:

$$K = \partial f/\partial VC = -\frac{0.32}{R_C C} \text{ Hz/V}$$

CAUTION: For safety operation of the circuit, I_T should be limited to ≤3 mA.

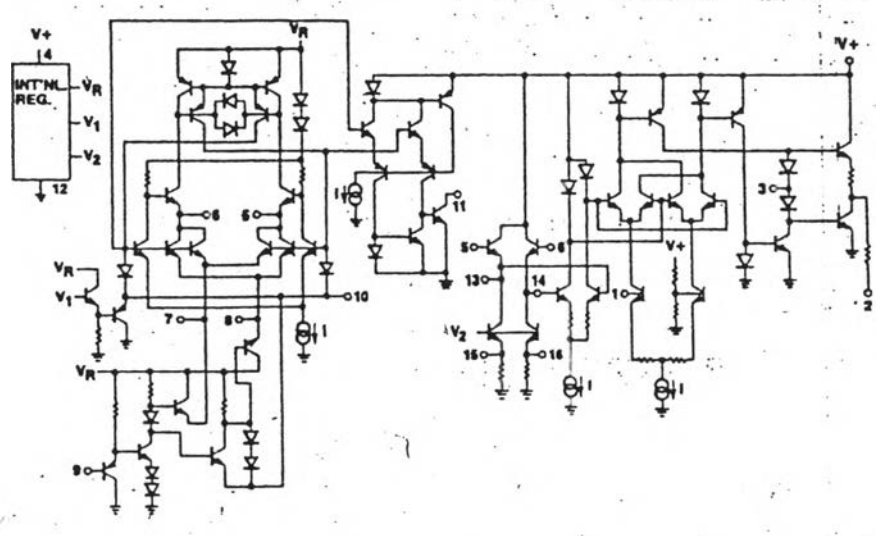
Output Amplitude:

Maximum output amplitude is inversely proportional to the external resistor, R_3, connected to Pin 3 (see Figure 2). For sine wave output, amplitude is approximately 60 mV peak per kΩ of R_3; for triangle, the peak amplitude is approximately 160 mV peak per kΩ of R_3. Thus, for example, R_3 = 50 kΩ would produce approximately ±3V sinusoidal output amplitude.

Amplitude Modulation:

Output amplitude can be modulated by applying a dc bias and a modulating signal to Pin 1. The internal impedance at Pin 1 is approximately 100 kΩ. Output amplitude varies linearly with the applied voltage at Pin 1 for values of dc bias at this pin, within ±4 volts of $V^+/2$ as shown in Figure 5. As this bias level approaches $V^+/2$, the phase of the output signal is reversed, and the amplitude goes through zero. This property is suitable for phase-shift keying and suppressed-carrier AM generation. Total dynamic range of amplitude modulation is approximately 55 dB.

CAUTION: AM control must be used in conjunction with a well-regulated supply, since the output amplitude now becomes a function of V^+.



EQUIVALENT SCHEMATIC DIAGRAM

EXAR

XR-2211

FSK Demodulator/Tone Decoder

GENERAL DESCRIPTION

The XR-2211 is a monolithic phase-locked loop (PLL) system especially designed for data communications. It is particularly well suited for FSK modem applications. It operates over a wide supply voltage range of 4.5 to 20V and a wide frequency range of 0.01 Hz to 300 kHz. It can accommodate analog signals between 2 mV and 3V, and can interface with conventional DTL, TTL, and ECL logic families. The circuit consists of a basic PLL for tracking an input signal within the pass band, a quadrature phase detector which provides carrier detection, and an FSK voltage comparator which provides FSK demodulation. External components are used to independently set center frequency, bandwidth, and output delay. An internal voltage reference proportional to the power supply provides ratio metric operation for low system performance variations with power supply changes.

The XR-2211 is available in 14 pin DTL ceramic or plastic packages specified for commercial or military temperature ranges.

FEATURES

Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20 V
DTL/TTL/ECL Logic Compatibility	
FSK Demodulation, with Carrier Detection	
Wide Dynamic Range	2 mV to 3 V rms
Adjustable Tracking Range (±1% to ±80%)	
Excellent Temp. Stability	20 ppm/°C, typ.

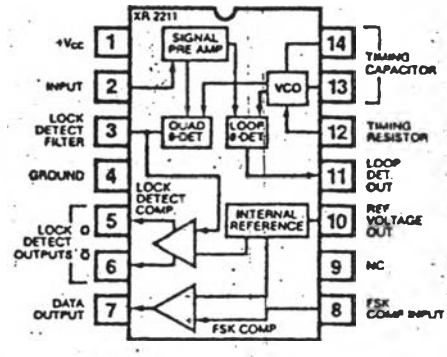
APPLICATIONS

FSK Demodulation
Data Synchronization
Tone Decoding
FM Detection
Carrier Detection

ABSOLUTE MAXIMUM RATINGS

Power Supply	20V
Input Signal Level	3V rms
Power Dissipation	
Ceramic Package	750 mW
Derate Above T_A = +25°C	6 mV/°C
Plastic Package	
Derate Above T_A = +25°C	5.0 mW/°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-2211M	Ceramic	−55°C to +125°C
XR-2211CN	Ceramic	0°C to +70°C
XR-2211CP	Plastic	0°C to +70°C
XR-2211N	Ceramic	−40°C to +85°C
XR-2211P	Plastic	−40°C to +85°C

SYSTEM DESCRIPTION

The main PLL within the XR-2211 is constructed from an input preamplifier, analog multiplier used as a phase detector, and a precision voltage controlled oscillator (VCO). The preamplifier is used as a limiter such that input signals above typically 2MV RMS are amplified to a constant high level signal. The multiplying-type phase detector acts as a digital exclusive or gate. Its output (unfiltered) produces sum and difference frequencies of the input and the VCO output, f input + f input (2f input) and f input - f input (0 Hz) when the phase detector output to remove the "sum" frequency component while passing the difference (DC) component to drive the VCO. The VCO is actually a current controlled oscillator with its nominal input current (f_0) set by a resistor (R_0) to ground and its driving current with a resistor (R_1) from the phase detector.

The other sections of the XR-2211 act to: determine if the VCO is driven above or below the center frequency (FSK comparator); produced both active high and active low outputs to indicate when the main PLL is in lock (quadrature phase detector and lock detector comparator)

XR-2211

ELECTRICAL CHARACTERISTICS

Test Conditions: Test Circuit of Figure 1, $V^+ = V^- = 6V$, $T_A = +25°C$, $C = 5000$ pF, $R_1 = R_2 = R_3 = R_4 = 20$ kΩ, $R_L = 4.7$ kΩ. Binary inputs grounded, S_1 and S_2 closed, unless otherwise specified.

PARAMETER	XR-2211/2211M MIN	XR-2211/2211M TYP	XR-2211/2211M MAX	XR-2211C MIN	XR-2211C TYP	XR-2211C MAX	UNITS	CONDITIONS
GENERAL								
Supply Voltage	4.5		20	4.5		20	V	
Supply Current		4	7		5	9	mA	$R_0 \geq 10$ kΩ. See Fig. 4
OSCILLATOR SECTION								
Frequency Accuracy		±1	±3		±1		%	Deviation from $f_0 = 1/R_0C_0$
Frequency Stability								$R_1 = 1/2$
Temperature		±20	±50		±20		ppm/°C	See Fig. 8.
Power Supply		0.05	0.5		0.05		%/V	$V^+ = 12 \pm 1$V. See Fig. 7.
		0.2			0.2		%/V	$V^+ 5 \pm 0.5$V. See Fig. 7.
Upper Frequency Limit	100	300			300		kHz	$R_0 = 8.2$ kΩ, $C_0 = 400$ pF
Lowest Practical								
Operating Frequency			0.01		0.01		Hz	$R_0 = 2$ MΩ, $C_0 = 50$ µF
Timing Resistor, R_0								See Fig. 5.
Operating Range	5		2000	5		2000	kΩ	
Recommended Range	15		100	15		100	kΩ	See Figs. 7 and 8.
LOOP PHASE DETECTOR SECTION								
Peak Output Current	±150	±200	±300	±100	±200	±300	µA	Measured at Pin 11.
Output Offset Current		±1			±2		µA	
Output Impedance		1			1		MΩ	
Maximum Swing	±4	±5		±4	±5		V	Referenced to Pin 10.
QUADRATURE PHASE DETECTOR								Measured at Pin 3.
Peak Output Current	100	150			150		µA	
Output Impedance		1			1		MΩ	
Maximum Swing		11			11		V pp	
INPUT PREAMP SECTION								Measured at Pin 2.
Input Impedance		20			20		kΩ	
Input Signal								
Voltage Required to								
Cause Limiting		2	10		2		mV rms	
VOLTAGE COMPARATOR SECTIONS								
Input Impedance		2			2		MΩ	Measured at Pins 3 and 8.
Input Bias Current		100			100		nA	
Voltage Gain	55	70		55	70		dB	$R_L = 5.1$ kΩ
Output Voltage Low		300			300		mV	$I_C = 3$ mA
Output Leakage Current		0.01			0.01		µA	$V_O = 12$V
INTERNAL REFERENCE								
Voltage Level	4.9	5.3	5.7	4.75	5.3	5.85	V	Measured at Pin 10.
Output Impedance		100			100		Ω	

XR-2211

9. Total Loop Gain, K_T:

$K_T = 2\pi K\phi K_O = 4/C_O R_1$ rad/sec/volt

10. Peak Phase Detector Current I_A:

$I_A = V_R$ (volts)/25 mA

APPLICATIONS INFORMATION

FSK DECODING:

Figure 9 shows the basic circuit connection for FSK decoding. With reference to Figures 2 and 9, the functions of external components are defined as follows: R_O and C_O set the PLL center frequency, R_1 sets the system bandwidth, and C1 sets the loop filter time constant and the loop damping factor. C_F and R_F form a one-pole post-detection filter for the FSK data output. The resistor R_B (= 510 KΩ) from Pin 7 to Pin 8 introduces positive feedback across the FSK comparator to facilitate rapid transition between output logic states.

Recommended component values for some of the most commonly used FSK bands are given in Table 1.

Design Instructions:

The circuit of Figure 9 can be tailored for any FSK decoding application by the choice of five key circuit components: R_O, R_1, C_O, C_1 and C_F. For a given set of FSK mark and space frequencies, f_1 and f_2, these parameters can be calculated as follows:

a) Calculate PLL center frequency, f_O:

$$f_O = \frac{f_1 + f_2}{2}$$

b) Choose value of timing resistor R_O, to be in the range of 10 KΩ to 100 KΩ. This choice is arbitrary. The recommended value is R_O = 20 KΩ. The final value of R_O is normally fine-tuned with the series potentiometer, R_X.

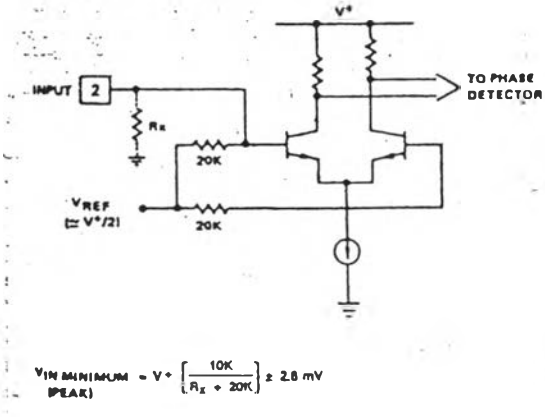


Figure 3. Desensitizing Input Stage

c) Calculate value of C_O from design equation (1) or from Figure 6:

$C_O = 1/R_O f_O$

d) Calculate R_1 to give a Δf equal to the mark space deviation:

$R_1 = R_O[f_O/(f_1 - f_2)]$

e) Calculate C_1 to set loop damping. (See design equation No. 4.):

Normally, ζ = 1/2 is recommenced.

Then: $C_1 = C_O/4$ for ζ = 1/2

f) Calculate Data Filter Capacitance, C_F:

For R_F = 100 KΩ, R_B = 510 KΩ, the recommended value of C_F is:

C_F = 3/(Baud Rate) μF

Note: All calculated component values except R_O can be rounded to the nearest standard value, and R_O can be varied to fine-tune center frequency, through a series potentiometer, R_X. (See Figure 9.)

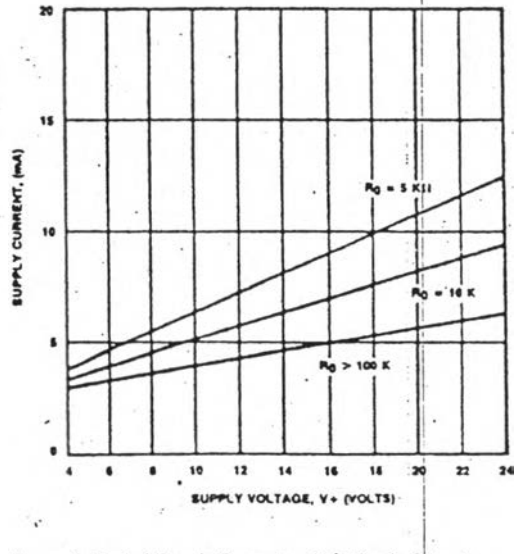


Figure 4. Typical Supply Current vs V+ (Logic Outputs Open Circuited)

Reference Voltage, V_R (Pin 10): This pin is internally biased at the reference voltage level, V_R: $V_R = V+/2 - 650$ mV. The dc voltage level at this pin forms an internal reference for the voltage levels at Pins 5, 8, 11 and 12. Pin 10 *must* be bypassed to ground with a 0.1 μF capacitor for proper operation of the circuit.

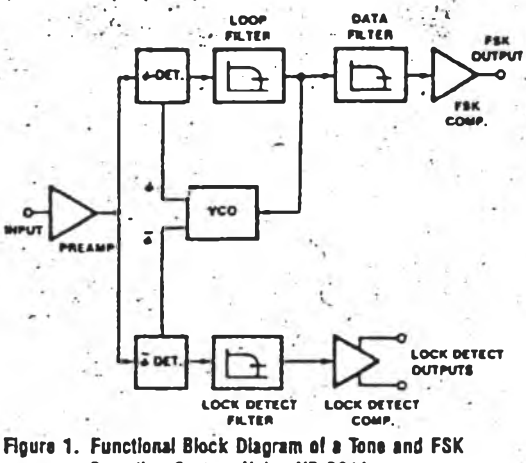


Figure 1. Functional Block Diagram of a Tone and FSK Decoding System Using XR-2211

Loop Phase Detector Output (Pin 11): This terminal provides a high impedance output for the loop phase detector. The PLL loop filter is formed by R_1 and C_1 connected to Pin 11 (see Figure 2). With no input signal, or with no phase error within the PLL, the dc level at Pin 11 is very nearly equal to V_R. The peak voltage swing available at the phase detector output is equal to $\pm V_R$.

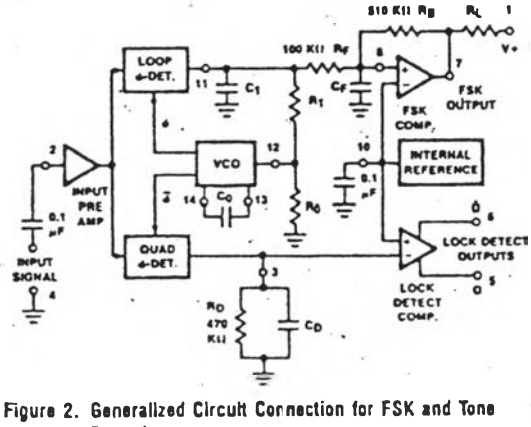


Figure 2. Generalized Circuit Connection for FSK and Tone Detection

VCO Control Input (Pin 12): VCO free-running frequency is determined by external timing resistor, R_0, connected from this terminal to ground. The VCO free-running frequency, f_0, is:

$$f_0 = \frac{1}{R_0 C_0} \text{ Hz}$$

where C_0 is the timing capacitor across Pins 13 and 14. For optimum temperature stability, R_0 must be in the range of 10 KΩ to 100 KΩ see Figure 8).

This terminal is a low impedance point, and is internally biased at a dc level equal to V_R. The maximum timing current drawn from Pin 12 must be limited to ≤ 3 mA for proper operation of the circuit.

VCO Timing Capacitor (Pins 13 and 14): VCO frequency is inversely proportional to the external timing capacitor, C_0, connected across these terminals (see Figure 5). C_0 must be nonpolar, and in the range of 200 pF to 10 μF.

VCO Frequency Adjustment: VCO can be fine-tuned by connecting a potentiometer, R_X, in series with R_0 at Pin 12 (see Figure 9).

VCO Free-Running Frequency, f_0: XR-2211 does not have a separate VCO output terminal. Instead, the VCO outputs are internally connected to the phase detector sections of the circuit. However, for set-up or adjustment purposes, VCO free-running frequency can be measured at Pin 3 (with C_D disconnected), with no input and with Pin 2 shorted to Pin 10.

DESIGN EQUATIONS

(See Figure 2 for definition of components.)

1. VCO Center Frequency, f_0

   $f_0 = 1/R_0C_0$ Hz

2. Internal Reference Voltage, V_R (measured at Pin 10):

   $V_R = V+/2 - 650$ mV

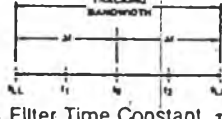
3. Loop Low-Pass Filter Time Constant, τ:

   $\tau = R_1C_1$

4. Loop Damping, ζ:

   $$\zeta = 1/4\sqrt{\frac{C_0}{C_1}}$$

5. Loop Tracking Bandwidth, $\pm \Delta f/f_0$:
   $\Delta f/f_0 = R_0/R_1$



6. FSK Data Filter Time Constant, τF:
   $\tau F = R_FC_F$

7. Loop Phase Detector Conversion Gain, $K\phi$: ($K\phi$ is the differential dc voltage across Pins 10 and 11, per unit of phase error at phase detector input):

   $K\phi = 02V_R/\pi$ volts/radian

8. VCO Conversion gain, K_0: (K_0 is the amount of change in VCO frequency, per unit of dc voltage change at Pin 11):

   $K_0 = -1/V_RC_0R_1$ Hz/volt

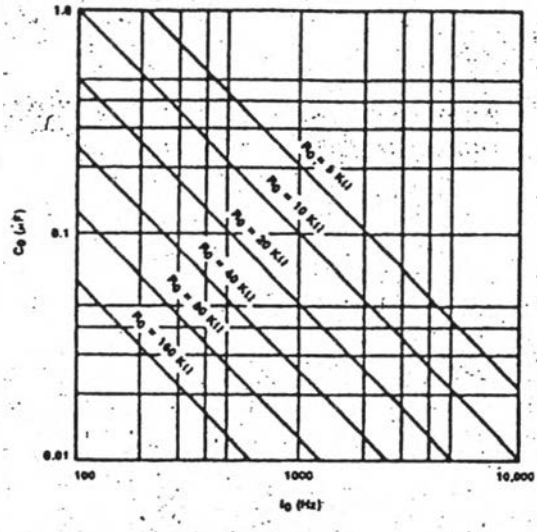


Figure 5. VCO Frequency vs Timing Resistor

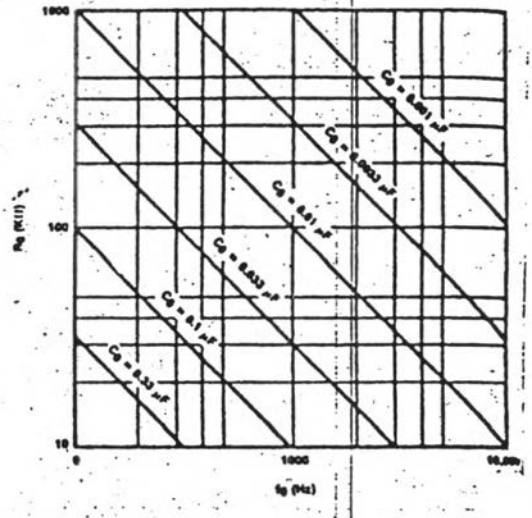


Figure 6. VCO Frequency vs Timing Capacitor

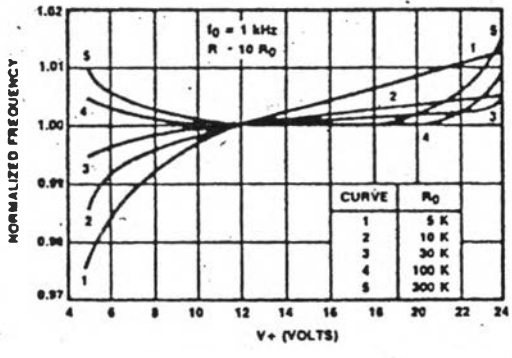


Figure 7. Typical f_0 vs Power Supply Characteristics

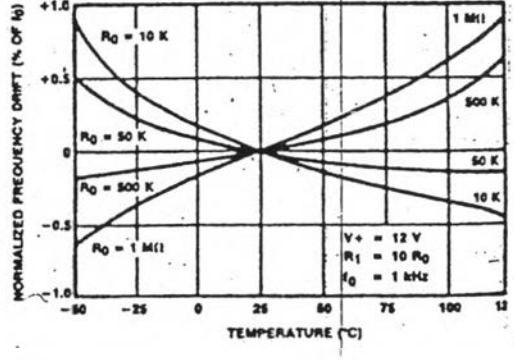


Figure 8. Typical Center Frequency Drift vs Temperature

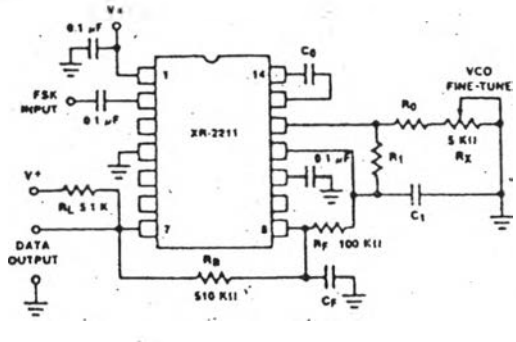


Figure 9. Circuit Connection for FSK Decoding

XR-2211

Design Example:

75 Baud FSK demodulator with mark space frequencies of 1110/1170 Hz:

Step 1: Calculate f_0: f_0 (1110 + 1170) (1/2) = 1140 Hz

Step 2: Choose R_0 - 20 KΩ (18 KΩ fixed resistor in series with 5 KΩ potentiometer)

Step 3: Calculate C_0 from Figure 6: C_0 = 0.044 μF

Step 4: Calculate R_1: R_1 = R_0 (2240/60) = 380 KΩ

Step 5: Calculate C_1: C_1 = C_0/4 = 0.011 μF

Note: All values except R_0 can be rounded to *nearest* standard value.

Table 1. Recommended Component Values for Commonly Used FSK Bands. (See Circuit of Figure 9.)

FSK BAND	COMPONENT VALUES
300 Baud f_1 = 1070 Hz F_2 = 1270 Hz	C_0 = 0.039 μF C_F = 0.005 μF C_1 = 0.01 μF R_0 = 18 KΩ R_1 = 100 KΩ
300 Baud f_1 = 2025 Hz f_2 = 2225 Hz	C_0 = 0.022 μF C_F = 0.005 μF C_1 = 0.0047 μF R_0 = 18 KΩ R_1 = 200 KΩ
1200 Baud f_1 = 1200 Hz f_2 = 2200 Hz	C_0 = 0.027 μF C_F = 0.0022 μF C_1 = 0.01 μF R_0 = 18 KΩ R_1 = 30 KΩ

FSK DECODING WITH CARRIER DETECT:

The lock detect section of XR-2211 can be used as a carrier detect option, for FSK decoding. The recommended circuit connection for this application is shown in Figure 10. The open collector lock detect output, Pin 6, is shorted to data output (Pin 7). Thus, data output

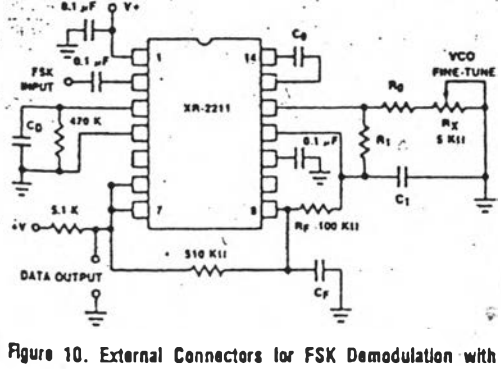


Figure 10. External Connectors for FSK Demodulation with Carrier Detect Capability

Note: Data Output is "Low" When No Carrier is Present.

will be disabled at "low" state, until there is a carrier within the detection band of the PPL, and the Pin 6 output goes "high," to enable the data output.

The minimum value of the lock detect filter capacitance C_D is inversely proportional to the capture range, ± Δf_C. This is the range of incoming frequencies over which the loop can acquire lock and is always less than the tracking range. It is further limited by C_1. For most applications, $\Delta f_C > \Delta f/2$. For R_D = 470 KΩ, the approximate minimum value of C_D can be determined by:

C_D (μF) ≥ 16/capture range in Hz.

With values of C_D that are too small, chatter can be observed on the lock detect output as an incoming signal frequency approaches the capture bandwidth. Excessively large values of C_D will slow the response time of the lock detect output.

TONE DETECTION:

Figure 11 shows the generalized circuit connection for tone detection. The logic outputs, Q and $\overline{Q}$ at Pins 5 and 6 are normally at "high" and "low" logic states, respectively. When a tone is present within the detection band of the PLL, the logic state at these outputs become reversed for the duration of the input tone. Each logic output can sink 5 mA of load current.

Both logic outputs at Pins 5 and 6 are open collector type stages, and require external pull-up resistors R_{L1} and R_{L2}, as shown in Figure 11.

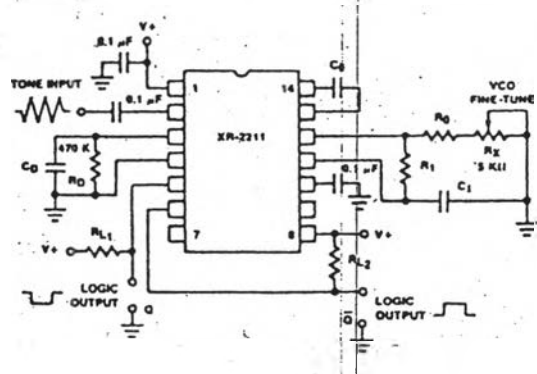


Figure 11. Circuit Connection for Tone Detection

With reference to Figures 2 and 11, the functions of the external circuit components can be explained as follows: R_0 and C_0 set VCO center frequency; R_1 sets the detection bandwidth; C_1 sets the low pass-loop filter time constant and the loop damping factor. R_{L1} and R_{L2} are the respective pull-up resistors for the Q and $\overline{Q}$ logic outputs.

Design Instructions:

The circuit of Figure 11 can be optimized for any tone detection application by the choice of the 5 key circuit components: R_0, R_1, C_0, C_1 and C_D. For a given input,

the tone frequency, f_S, these parameters are calculated as follows:

a) Choose R_0 to be in the range of 15 KΩ to 100 KΩ. This choice is arbitrary.

b) Calculate C_0 to set center frequency, f_0 equal to f_s (see Figure 6): $C_0 = 1/R_0 f_S$

c) Calculate R_1 to set bandwidth $\pm\Delta f$ (see design equation No. 5):

$$R_1 = R_0(f_0/\Delta f)$$

Note: The total detection bandwidth covers the frequency range of $f_0 \pm \Delta f$.

d) Calculate value of C_1 for a given loop damping factor;

$$C_1 = C_0/16\zeta^2$$

Normally $\zeta = 1/2$ is optimum for most tone detector applications, giving $C_1 = 0.25\ C_0$.

Increasing C_1 improves the out-of-band signal rejection, but increases the PLL capture time.

e) Calculate value of filter capacitor C_D. To avoid chatter at the logic output, with $R_D = 470$ KΩ, C_D must be:

$$C_D(\mu F) \geq (16/\text{capture range in Hz})$$

Increasing C_D slows down the logic output response time.

Design Examples:

Tone detector with a detection band of 1 kHz ± 20 Hz:

a) Choose $R_0 = 20$ KΩ (18 KΩ in series with 5 KΩ potentiometer).

b) Choose C_0 for $f_0 = 1$ kHz (from Figure 6): $C_0 = 0.05\ \mu F$.

c) Calculate R_1: $R_1 = (R_0)\ (1000/20) = 1$ MΩ.

d) Calculate C_1: for $\zeta = 1/2$, $C_1 = 0.25$, $C_0 = 0.013\ \mu F$.

e) Calculate C_D: $C_D = 16/38 = 0.42\ \mu F$.

f) Fine-tune center frequency with 5 KΩ potentiometer, R_X.

LINEAR FM DETECTION:

XR-2211 can be used as a linear FM detector for a wide range of analog communications and telemetry applications. The recommended circuit connection for this application is shown in Figure 12. The demodulated output is taken from the loop phase detector output (Pin 11), through a post-detection filter made up of R_F and C_F, and an external buffer amplifier. This buffer amplifier is necessary because of the high impedance output at Pin 11. Normally, a non-inverting unity gain op amp can be used as a buffer amplifier, as shown in Figure 12.

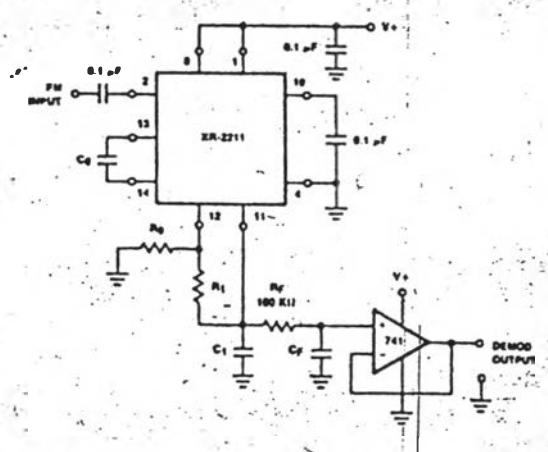


Figure 12. Linear FM Detector Using XR-2211 and an External Op Amp. (See Section on Design Equation for Component Values.)

The FM detector gain, i.e., the output voltage change per unit of FM deviation can be given as:

$$V_{out} = R_1\ V_R/100\ R_0 \text{ Volts/\% deviation}$$

where V_R is the internal reference voltage ($V_R = V+/2 - 650$ mV). For the choice of external components R_1, R_0, C_D, C_1 and C_F, see section on design equations.

PRINCIPLES OF OPERATION

Signal Input (Pin 2): Signal is ac coupled to this terminal. The internal impedance at Pin 2 is 20 KΩ. Recommended input signal level is in the range of 10 mV rms to 3V rms.

Quadrature Phase Detector Output (Pin 3): This is the high impedance output of quadrature phase detector and is internally connected to the input of lock detect voltage comparator. In tone detection applications, Pin 3 is connected to ground through a parallel combination of R_D and C_D (see Figure 2) to eliminate the chatter at lock detect outputs. If the tone detect section is not used, Pin 3 can be left open circuited.

Lock Detect Output, Q (Pin 5): The output at Pin 5 is at "high" state when the PLL is out of lock and goes to "low" or conducting state when the PLL is locked. It is an open collector type output and requires a pull-up resistor, R_L, to V+ for proper operation. At "low" state, it can sink up to 5 mA of load current.

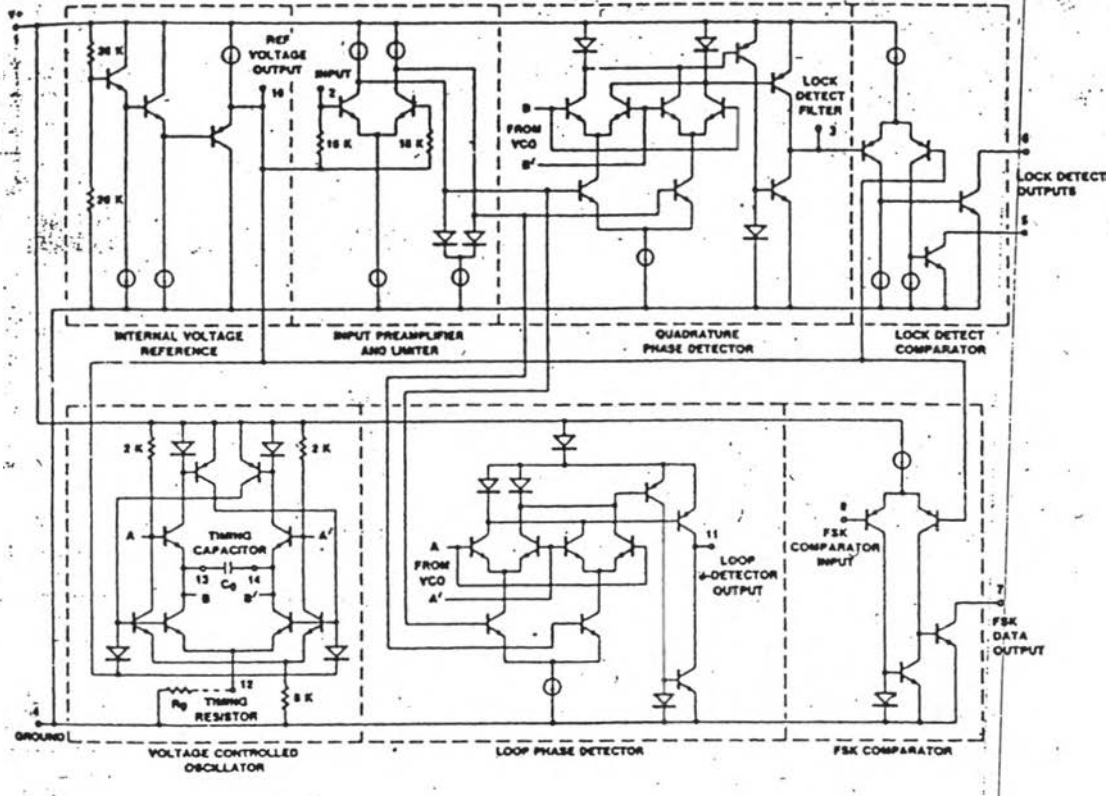
Lock Detect Complement, $\overline{Q}$ (Pin 6): The output at Pin 6 is the logic complement of the lock detect output at Pin 5. This output is also an open collector type stage which can sink 5 mA of load current at low or "on" state.

XR-2211

FSK Data Output (Pin 7): This output is an open collector logic stage which requires a pull-up resistor, R_L, to V+ for proper operation. It can sink 5 mA of load current. When decoding FSK signals, FSK data output is at "high" or "off" state for low input frequency, and at "low" or "on" state for high input frequency. If no input signal is present, the logic state at Pin 7 is indeterminate.

FSK Comparator Input (Pin 8): This is the high impedance input to the FSK voltage comparator. Normally, an FSK post-detection or data filter is connected between this terminal and the PLL phase detector output (Pin 11). This data filter is formed by R_F and C_F of Figure 2. The threshold voltage of the comparator is set by the internal reference voltage, V_R, available at Pin 10.

EQUIVALENT SCHEMATIC DIAGRAM



ภาคผนวก ค.

โปรแกรมควบคุมการทำงาน

Channel Colour สีประจำช่องความถี่	Transmitter ความถี่แร่คริสตอลภาคส่ง	Receiver ความถี่แร่คริสตอลภาครับ	
	MHz	I.F.455KHz	I.F.465KHz
น้ำตาล	26.995	26.540	26.530
แดง	27.045	26.590	26.580
ส้ม	27.095	26.640	26.630
เหลือง	27.145	26.690	26.680
เขียว	27.195	26.740	26.730
น้ำเงิน	27.245	26.790	26.780

```
;*************************************************************************
;*****  PROGRAM FOR PRECESS SIGNAL AND SEND IT BY WIRELESS METHOD  *****
;*****                      CHULALONGKORN UNIVERSITY                *****
;*****    BY MR. AMNUAY SOODSAKORN   C2-17065 NUCLEAR TECHNOLOGY   *****
;*************************************************************************
;
;***************************
;This program thesis CHULA.
;***************************
org 2200H
;Init 8255 and control word
;*** for EXP-2..PA=IN ,PB=IN ,PCH=IN ,PCL=IN.
EXP2PA          EQU      0E080H
EXP2PB          EQU      0E081H
EXP2PC          EQU      0E082H
EXP2PCC         EQU      0E083H
;*** for EXP-3..PA=OUT,PB=OUT,PCH=OUT,PCL=OUT.
EXP3PA          EQU      0E0A0H
EXP3PB          EQU      0E0A1H
EXP3PC          EQU      0E0A2H
EXP3PCC         EQU      0E0A3H
;*** for EXP-4..PA=   ,PB=   ,PCH=   ,PCL=
EXP4PA          EQU      0E0C0H
EXP4PB          EQU      0E0C1H
EXP4PC          EQU      0E0C2H
EXP4PCC         EQU      0E0C3H
;***************************
CTRLW1          EQU      09BH    ;control word for EXP-2
CTRLW2          EQU      080H    ;control word for EXP-3
CTRLW3          EQU      080H    ;control word for EXP-4
;***************************
LOCAT1          EQU      02500H  ;first addr. for save address
;*********************************
```

```
;**********************************
;*** LOAD CONTROL WORD TO 8255 ***
;**********************************
;
BEGIN:   MOV   A,#CTRLW1        ;control word = 09Bh
         MOV   DPTR,#EXP2PCC    ;IN IN IN
         MOVX  @DPTR,A          ;conrtol word for EXP-2
         MOV   A,#CTRLW2        ;control word = 080h
         MOV   DPTR,#EXP3PCC    ;OUT OUT OUT
         MOVX  @DPTR,A          ;control word for EXP-3
         MOV   A,#CTRLW3
         MOV   DPTR,#EXP4PCC
         MOVX  @DPTR,A          ;control word for EXP-4
;**************************
;INITIAL SERIAL PORT
;**************************
;
INIT:    MOV  SCON,#50H          ;page 30 MCS-51
         MOV  TMOD,#20H          ;page 38  mode 2
         MOV  TH1,#0E8H          ;set baud rate to 1200 bps.
         SETB  TR1
         CLR  ET1
         CLR  ES

;**************************
;RESET OUTPUT PORT 8255
;
RESP:    MOV  A,#00H
         MOV  DPTR,#EXP3PA
         MOVX @DPTR,A
         MOV  DPTR,#EXP3PB
         MOVX @DPTR,A
         MOV  DPTR,#EXP3PC
         MOVX @DPTR,A
;
```

```
;**************************
;TRIG FOR PEAK
;**************************
;
TRIG:    MOV  A,#00H          ;trig all bit to '0'
         MOV  DPTR,#EXP3PA
         MOVX @DPTR,A
         MOV  A,#00H          ;
;
;**************************
CHKP:    MOV  DPTR,#EXP2PC
         MOVX A,@DPTR
         ANL  A,#00000100B    ;
         JZ   CHKP
;
DELA:    MOV  A,#20H          ;delay 16 uS
DELAY:   DEC  A
         JNZ  DELAY
CEOC:    MOV  DPTR,#EXP2PC
         MOVX A,@DPTR
         ANL  A,#00001000B    ;check end of conversion
         JZ   CEOC
;
SAVE:    MOV  DPTR,#EXP2PA
         MOVX A,@DPTR
         MOV  DPTR,#2500H
         MOVX @DPTR,A
         MOV  DPTR,#EXP2PB
         MOVX A,@DPTR
         MOV  DPTR,#2501H
         MOVX @DPTR,A
CLRP:    MOV  A,#00100000B
         MOV  DPTR,#EXP3PA
         MOVX @DPTR,A
```

```
;*********************************
;SEND TO SERIAL PORT AND OUT
;
START:   CLR  ES
         CLR  RI
         CLR  TI
         MOV  DPTR,#2500H
         MOVX A,@DPTR
         MOV  SBUF,A
         JNB  TI,$
         CLR  TI
         INC  DPTR
         MOVX A,@DPTR
         MOV  SBUF,A
         JNB  TI,$
         CLR  TI
;*********************************
         LJMP TRIG
;*********************************
         END
```

```
read_com()
 {
  int data;
  unsigned char ch_l,ch_h;
   ch_l=read();
   ch_h=read();
  data=ch_l+(ch_h*0x100);
  return(data);
 }
read_head()
 {
   int count;
   unsigned char ch;
   /* get header befor recive data */
   for(count=0;count<2;count++)
    {
     do{
       ch=read();
       }while(ch!=0xFF);
    }
 }
read()
  {
     unsigned char ch,t1;
     do{
t1=inportb(0x3FD);
t1=t1&0x01;
}while(t1!=1);
ch=inportb(0x3F8);
      outportb(0x3FA,0x86); /* reset recive buffer */
      return(ch);
   }
set_com()
  {
   unsigned char data;
```

```
    _AH = 0x00;
    _AL = 0x83;
    _DX = 0x00;
    geninterrupt(0x14);
    data=inportb(0x3FB);  /* set to data mode */
    data=data&0x7F;
    outportb(0x3FB,data);
    outport(0x3F9,0x0F);
    outportb(0x3FC,0x0F);
   }
hit_key()
 {
    unsigned int key;
      if((key=bioskey(1))!=0)
       {
key=bioskey(0);
return(key);
        }
    return(0);
   }
```

```
gen_graph()
 {
  int GD=DETECT,GM;
  int count,x,y;
   initgraph(&GD,&GM,NULL);
   x=getmaxx();
   y=getmaxy();
   setcolor(BLUE);
   setbkcolor(WHITE);
   setfillstyle(SOLID_FILL,DARKGRAY);
   bar(1,1,getmaxx(),getmaxy());
   setcolor(LIGHTGREEN);
   line(50,10,50,410);
   line(50,410,610,410);
   x=50;
   y=410;
    for(count=0;count<103;count++)
      {
       x=x+5;
       line(x,y,x,y+5);
      }
   setcolor(YELLOW);
   outtextxy(40,420,"0");
   outtextxy(x,420,"1023");
   outtextxy(5,(410-(1*30)-3)," 1000");
   outtextxy(5,(410-(2*30)-3)," 2000");
   outtextxy(5,(410-(3*30)-3)," 3000");
   outtextxy(5,(410-(4*30)-3)," 4000");
   outtextxy(5,(410-(5*30)-3)," 5000");
   outtextxy(5,(410-(6*30)-3)," 6000");
   outtextxy(5,(410-(7*30)-3)," 7000");
   outtextxy(5,(410-(8*30)-3)," 8000");
   outtextxy(5,(410-(9*30)-3)," 9000");
   outtextxy(5,(410-(10*30)-3),"10000");
   setcolor(GREEN);
```

```
    x=50;
    y=410;
      for(count=1;count<=100;count++)
       {
y=y-3;
        if((count%10)==0)
  {
    line(x-6,y,x,y);
  }
else
  {
    line(x-3,y,x,y);
  }
      }
    settextstyle(SMALL_FONT,HORIZ_DIR,1);
    setcolor(LIGHTBLUE);
    settextstyle(DEFAULT_FONT,HORIZ_DIR,2);
    outtextxy(180,445,"NUCLEAR SPECTRUM");
    setfillstyle(SOLID_FILL,BLACK);
    bar(525,440,630,460);
    settextstyle(SMALL_FONT,HORIZ_DIR,1);
    setcolor(WHITE);
    outtextxy(530,450,"Scale = 1:10");
    }
re_graph()
  {
    setbkcolor(BLACK);
    setfillstyle(EMPTY_FILL,WHITE);
    bar(51,11,610,409);
    setcolor(LIGHTRED);
    outtextxy(15,95,"Over");
    line(47,105,620,105);
  }
set_time()
  {
```

```
    settextstyle(SMALL_FONT,HORIZ_DIR,1);
    setcolor(WHITE);
    outtextxy(12,11,"TIME");
    outtextxy(17,50,"min");
    setfillstyle(SOLID_FILL,BLACK);
    bar(10,25,40,45);
    }
/*out_time()
  {
    char ch[3]={NULL,NULL,NULL};
    int count=0;
    settextstyle(SMALL_FONT,HORIZ_DIR,1);
    setcolor(WHITE);
    outtextxy(12,11,"TIME");
    outtextxy(17,50,"min");
    setbkcolor(BLACK);
    setfillstyle(EMPTY_FILL,BLACK);
    do{
       ch[count]=getch();
       count++;
       bar(10,25,40,45);
       outtextxy(

       }while(ch[count]!=ENTER||key==ESx);
  }*/
off_graph()
  {
    int x,y;
    setcolor(BLACK);
    x=getmaxx();
    y=getmaxy();
    setfillstyle(SOLID_FILL,BLACK);
    bar(1,1,x,y);
    closegraph();
    }
```

```
#include<stdio.h>
#include<conio.h>
#include<dos.h>
#include<graphics.h>
#include<bios.h>
#include"gph.c"
#include"recive.c"
#define   SET_T   0x1400
#define    ESC    0x011B
#define   DEF_T     50
#define   ENTER   0x1C0D
#define   Enter   0x0D1C
#define    HB     0xFFFF
#define    TB     0xF0F0

unsigned int cc[1024];
unsigned int key,tm;
struct time tt_old,tt_new;

main()
 {
  unsigned int  data;
 tm=DEF_T;
 reset_val();
 set_com();
 gen_graph();
BEGIN:
 re_graph();
 set_time();
 out_time(tm);
 gettime(&tt_old);
 setfillstyle(SOLID_FILL,WHITE);
 do{
/*     read_head();*/
/*      if(key==ESC)
```

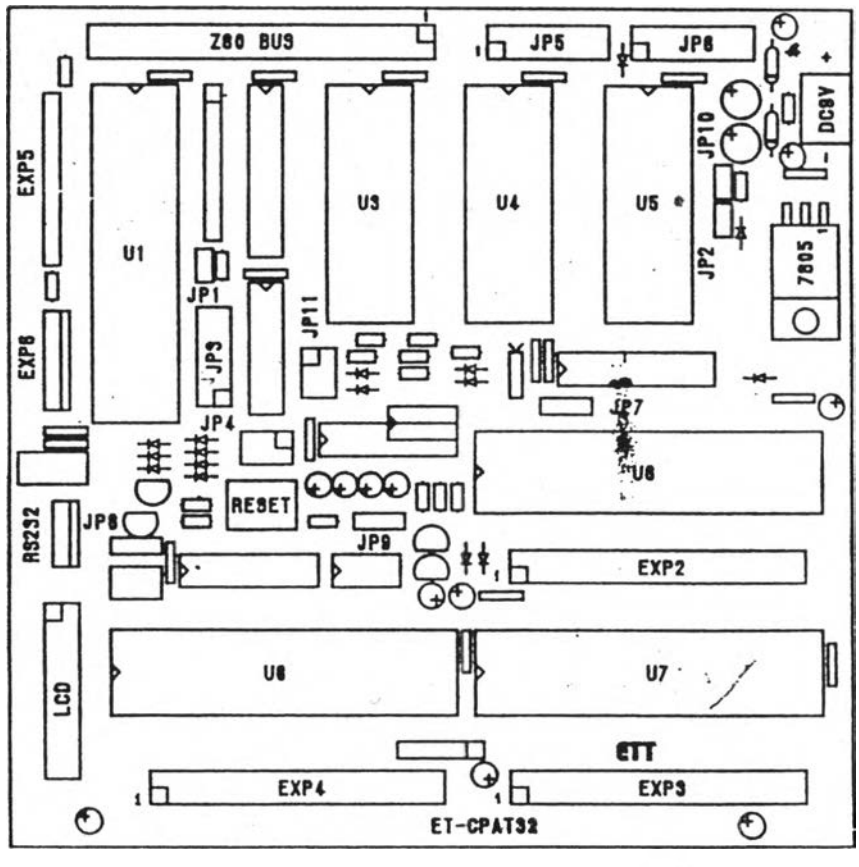
```
{
  goto==ESC;
 } */
      do{
  data=read_com();
/*  if(key==ESC)
    {
     goto C_KEY;
    } */
  if((data!=HB)&&(data!=TB))
    {
      data=data&0x3FF;
      cc[data]++;
      if(cc[data]>100)cc[data]=100;
      set_bar(data,cc[data]);
    }
 key=0x0000;
 key=hit_key();
 gettime(&tt_new);
/* }while(data!=TB&&key!=ESC&&((((tt_new.ti_hour-tt_old.ti_hour)*60)+(tt_new.ti_
 }while(key!=ESC&&((((tt_new.ti_hour-tt_old.ti_hour)*60)+(tt_new.ti_min-tt_old.t
    }while(key!=ESC&&((((tt_new.ti_hour-tt_old.ti_hour)*60)+(tt_new.ti_min-tt_ol
C_KEY:do{
    key=0x0000;
    key=hit_key();
    if(key==ENTER||key==Enter)
       goto BEGIN;
    if(key==SET_T)
      {
       tm=get_time(tm);
       goto BEGIN;
      }
  }while(key==0x0000||key!=ESC);
 }
```

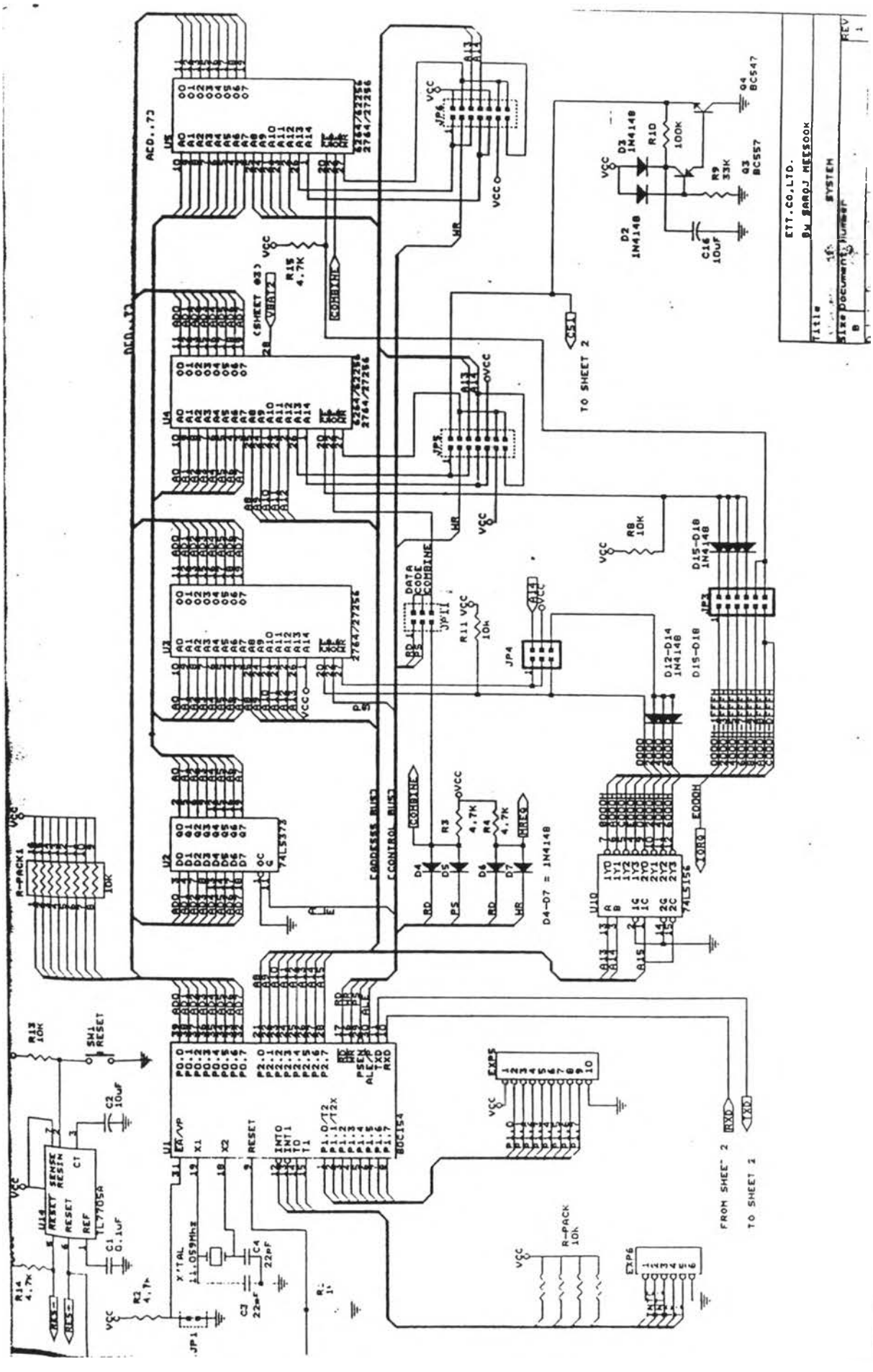
```
get_time(int ttm)
 {
  int  t1,t2,count;
  char ch[3]={'0','0',NULL};
  char cha;
  out_time(ttm);
   count=1;
   do{
       cha=getch();
       if(cha<='9'||cha>='0')
 {
  ch[0]=ch[1];
  ch[1]=cha;
 }
       else sound(800);
      ttm=(ch[0]-'0'*10)+(ch[1]-'0');
      out_time(ttm);
     }while(cha!=0x0D||cha!=0x1D);
    return(ttm);
 }
out_time(int tm)
 {
  char ch[3]={NULL,NULL,NULL};
  int  tmp1,tmp2;
       tmp1=tm/10;
       tmp2=tm%10;
       ch[0]='0'+tmp1;
       ch[1]='0'+tmp2;
       setfillstyle(SOLID_FILL,BLACK);
       bar(10,25,40,45);
       outtextxy(15,28,ch);
 }

set_bar(int chan,int data)
 {
```

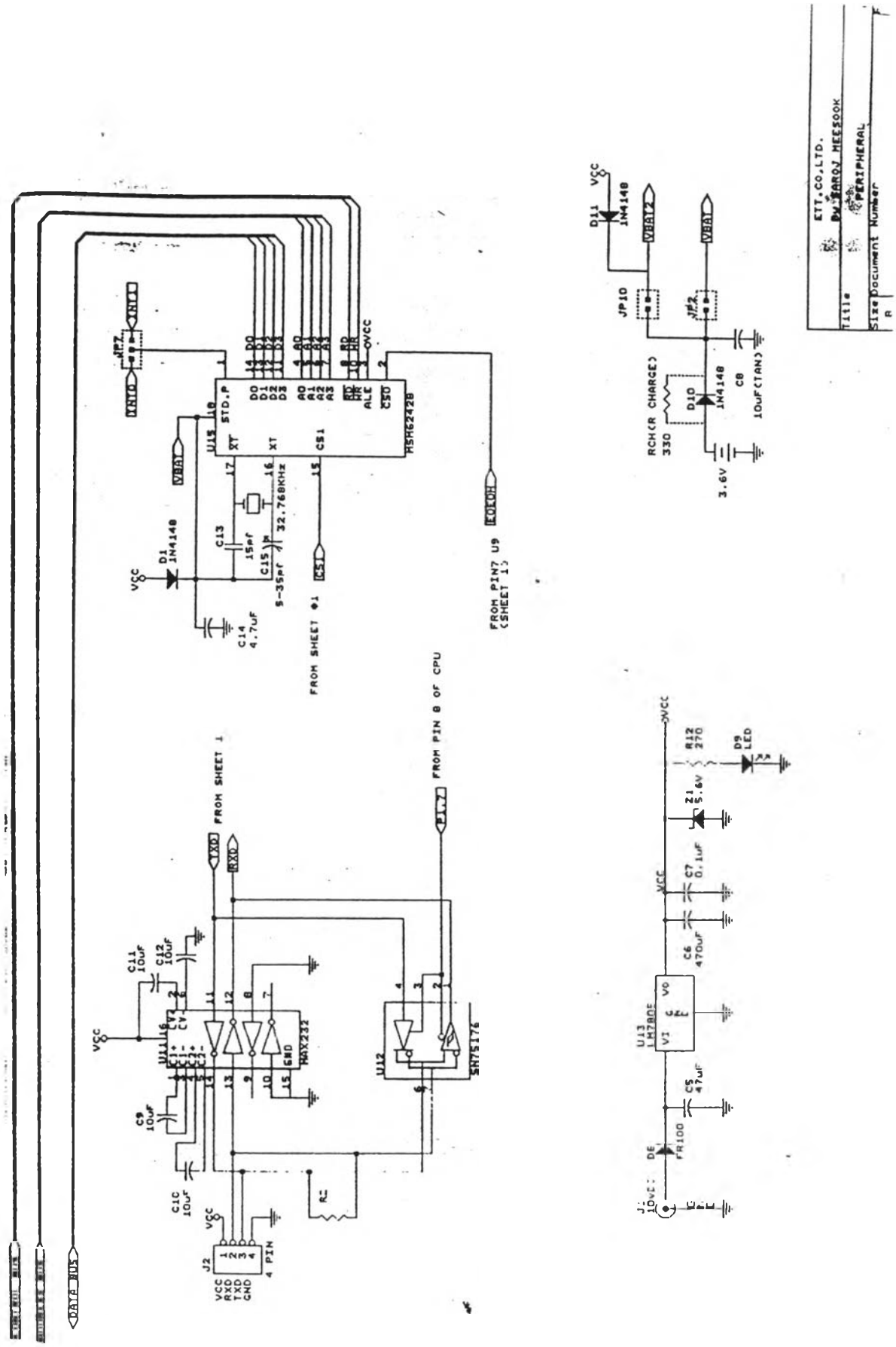
```
  int x1,y1,x2,y2,cc1,cc2,high;
      y2=409;
      if((chan%10)>0)
{
  cc1=1;
}
      else
       {
 cc1=0;
       }
       if((data%10)>0)
{
  cc2=1;
}
      else
       {
 cc2=0;
       }
       y1=y2-(((data/1)*3)+(cc2*3))+1;   /* +1 for simu to y=410 */
       x1=51+(((chan/10)*5)+(1-cc1));
       x2=x1+3;
       bar(x1,y1,x2,y2);
 }

 reset_val()
    {
      unsigned int count;
 for(count=0;count<1024;count++);
  {
    cc[count]=0;
  }
     }
```

ภาคผนวก ง.

วงจรเครื่องรับ/ส่ง
ไมโครคอนโทรลเลอร์


Z80 BUS
JP5
JP6
DC9V
JP10
JP2
7805
EXP5
U1
U3
U4
U5
JP1
JP3
JP11
EXP6
JP4
JP7
U8
RESET
RS232
JP8
JP9
EXP2
LCD
U6
U7
ETT
EXP4
EXP3
ET-CPAT32


ETT.CO,LTD.
By BARQ MEESOOK
SYSTEM
TO SHEET 2
FROM SHEET 2
TO SHEET 1
D4-D7 = 1N4148
D15-D18
D12-D14
D15-D18
74LS373
74LS154
80C154
TL7705A
X'TAL
11.059MHz
R-PACK1
10K
R-PACK
10K
EXP5
EXP6
JP1
JP2
JP3
JP4
SW1
RESET
COMBINE
DATA
CODE
ADDRESS BUS
CONTROL BUS
VCC
RXD
TXD


ADDR BUS
DATA BUS
CONTROL BUS
VCC
VBAT
D1 IN4148
C14 4.7uF
C13 15pf
C15 5-35pf
32.768KHz
XT
STD.P
MSM62428
CS1
CS2
FROM SHEET #1
FROM PIN7 U9 (SHEET 1)
FROM PIN 8 OF CPU
TXD
RXD
MAX232
SN75176
C11 10uF
C12 10uF
C9 10uF
C10 10uF
J2 4 PIN
VCC RXD TXD GND
D11 IN4148
JP10
JP12
RCH(R CHARGE) 330
D10 IN4148
3.6V
C8 10uF(TAN)
U13 LM78M05
C5 47uF
C6 470uF
C7 0.1uF
Z1 5.6V
R12 270
D9 LED
FR100
ETT.CO.LTD.
By SAROJ MEESOOK
Title PERIPHERAL
Size Document Number
A

PRELIMINARY

AUGUST 1988

DATA SHEET

83C154

CMOS SINGLE - CHIP 8 BIT MICROCONTROLLER

- **83C154 – CMOS SINGLE-CHIP 8-BIT MICROCONTROLLER with factory mask-programmable ROM**
- **83C154F – The internal ROM code cannot be read or dumped after activation of a special protection**
- **80C154 – ROMLESS version**
- **83C154-1 – 16 MHz version**
- **80C154-1 – 16 MHz ROMless version**

FEATURES

- 16K x 8 BIT INTERNAL ROM
- 256 x BIT RAM
- 32 PROGRAMMABLE I/O LINES (PROGRAMMABLE IMPEDANCE)
- THREE 16-BIT TIMER/COUNTERS (INCLUDING WATCH DOG AND 32 BIT TIMER)
- 64K PROGRAM MEMORY SPACE
- FULLY STATIC DESIGN
- POWER CONTROL MODES
- INTERRUPT PRIORITY CONTROL
- 0 TO 16 MHz
- BOOLEAN PROCESSOR
- 6 INTERRUPT SOURCES
- PROGRAMMABLE SERIAL PORT
- 64K DATA MEMORY SPACE
- TEMPERATURE RANGE:
  - COMMERCIAL
  - INDUSTRIAL

DESCRIPTION

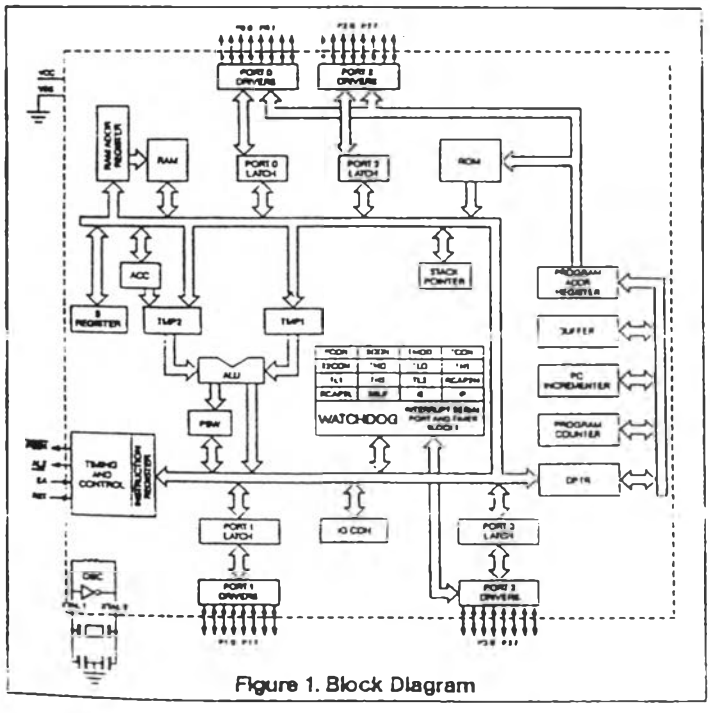


Figure 1. Block Diagram

The 83C154 retains all the features of the MHS 80C52 with extended ROM capacity (16K bytes), 256 bytes of RAM, 32 I/O lines, a 6-source 2-level interrupts, a full duplex serial port, an on-chip oscillator and clock circuits, three 16 bit timers with extra features: 32 bit timer and watch dog functions. Timer 0 and 1 can be configured by program to implement a 32 bit timer. The watch dog function can be activated either with timer 0, or timer 1 or both together (32 bit timer).

In addition, the 83C154 has two software selectable modes of reduced activity for further reduction of power consumption. In the Idle Mode, the CPU is frozen while the RAM is saved, and the timers, the serial port, and the interrupt system continue to function. In the Power Down Mode, the RAM is saved and the timers, serial port and interrupts continue to function when driven by external clocks. In addition as for the MHS 80C51/C52, the stop clock mode is also available.

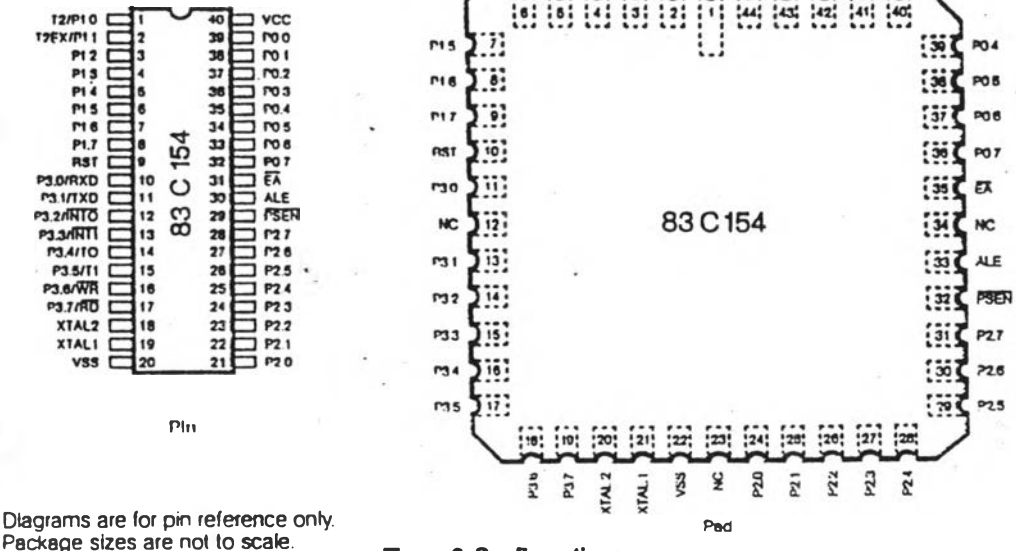


Figure 2. Configurations

3 IDLE AND POWER DOWN OPERATION

Figure 3 shows the internal Idle and Power Down clock configuration. As illustrated, Power Down operation stops the oscillator. The interrupt, serial port, and timer blocks continue to function only with external clock (INT0, INT1, T0, T1).

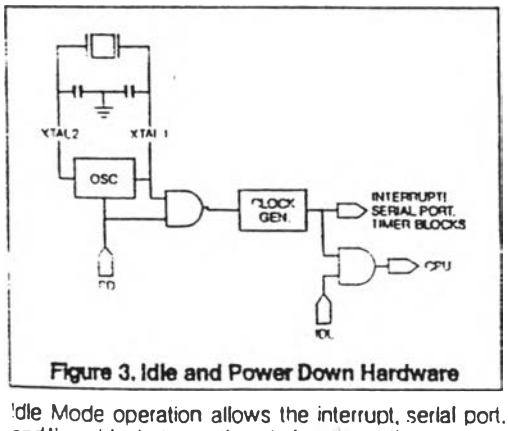


Figure 3. Idle and Power Down Hardware

Idle Mode operation allows the interrupt, serial port, and timer blocks to continue to function with internal or external clocks, while the clock to CPU is gated off. The special modes are activated by software via the Special Function Register, PCON. Its hardware address is 87H. PCON is not bit addressable.

PCON: Power Control Register

(MSB) (LSB)

SMOD	HPD	RPD	-	GF1	GF0	PD	IDL

Symbol	Position	Name and Function
SMOD	PCON.7	Double Baud rate bit. When s to a 1, the baud rate is doub when the serial port is be used in either modes 1, 2 or
HPD	PCON.6	Hard Power Down bit. Setti this bit allows CPU to enter Power Down state on a external event (1 to 0 transitic on bit T1 (p. 3-5) the CPU qu the Hard Power Down mod when bit T1 (p. 3-5) go high when reset is activated.
RPD	PCON.5	Recover from Idle or Pow Down bit. When 0 RPD has n effect. When 1, RPD permits exit from idle or Power Dow with any non enabled interru source (except timex 2). In th case the program start at th next address. When interru is enabled, the appropria interrupt routine is serviced.
-	PCON.4	(Reserved)
GF1	PCON.3	General-purpose flag bit.
GF0	PCON.2	General-purpose flag bit.
PD	PCON.1	Power Down bit. Setting this b activates power down oper tion.
IDL	PCON.0	Idle mode bit. Setting this b activates Idle mode operatio

PRELIMINARY AUGUST 1988

DATA SHEET 80C51-L / 80C31-L

CMOS SINGLE-CHIP 8 BIT 3V-MICROCONTROLLER

- **80C51-L – CMOS SINGLE-SHIP 8-BIT MICROCONTROLLER with factory mask-programmable ROM**
- **80C31-L - CMOS SINGLE-CHIP 8-BIT CONTROL-ORIENTED CPU with RAM and I/O**
- **80C51-L/C31-L: 0 TO 6 MHz, VCC = 2.7V TO 6V**

FEATURES

- **POWER CONTROL MODES**
- **128 x 8 BIT RAM**
- **32 PROGRAMMABLE I/O LINES**
- **TWO 16-BIT TIMER/COUNTERS**
- **64K PROGRAM MEMORY SPACE**
- **FULLY STATIC DESIGN**
- **HIGH PERFORMANCE SAJI VI CMOS PROCESS**
- **BOOLEAN PROCESSOR**
- **5 INTERRUPT SOURCES**
- **PROGRAMMABLE SERIAL PORT**
- **64K DATA MEMORY SPACE**
- **TEMPERATURE RANGE: 0 TO 70°C**

DESCRIPTION

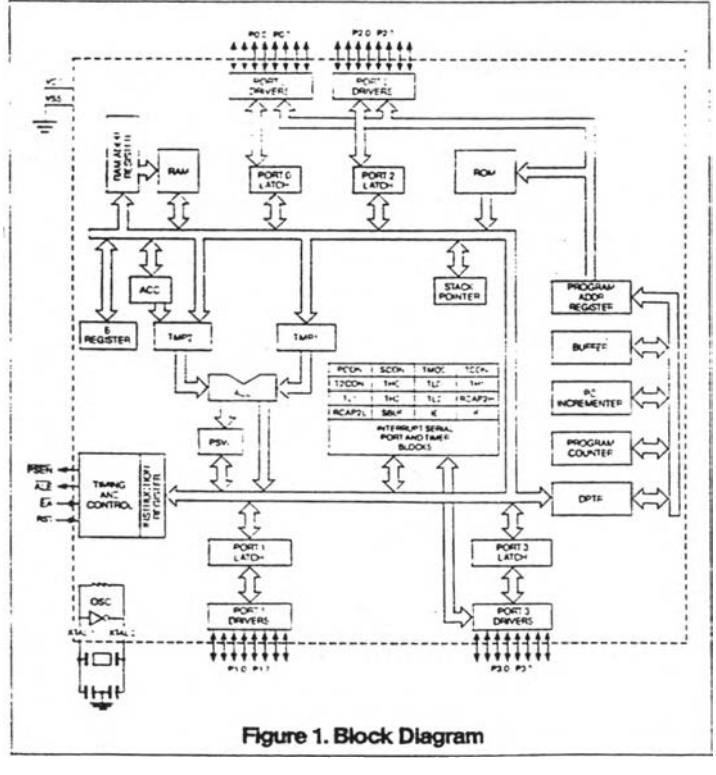


Figure 1. Block Diagram

MHS's 80C51 and 80C31 are high performance CMOS versions of the 8051/8031 NMOS single chip 8 bit µC and is manufactured using a self-aligned silicon gate CMOS process (SAJI VI).

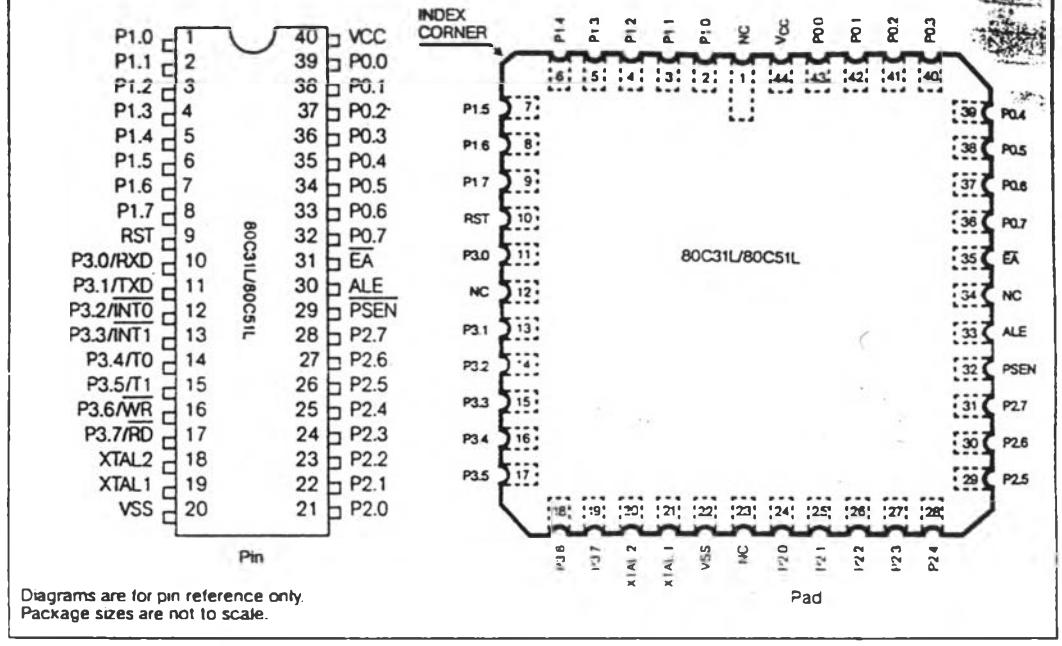
The fully static design of the MHS 80C51/80C31 allows to reduce system power consumption by bringing the clock frequency down to any value, even DC, without loss of data.

The 80C51 retains all the features of the 8051: 4K bytes of ROM; 128 bytes of RAM; 32 I/O lines; two 16 bit timers; a 5-source 2-level interrupt structure; a full duplex serial port; and on-chip oscillator and clock circuits.

In addition, the 80C51 has two software-selectable modes of reduced activity for further reduction in power consumption. In the Idle Mode the CPU is frozen while the RAM, the timers, the serial port, and the interrupt system continue to function. In the Power Down Mode the RAM is saved and all other functions are inoperative.

The 80C31 is identical to the 80C51 except that it has no on-chip ROM.

Figure 2. Configurations



Diagrams are for pin reference only.
Package sizes are not to scale.

IDLE AND POWER DOWN OPERATION

Figure 3 shows the internal Idle and Power Down clock configuration. As illustrated, Power Down operation stops the oscillator. Idle mode operation allows the interrupt, serial port, and timer blocks to continue to function while the clock to the CPU is gated off.
These special modes are activated by software via the Special Function Register. Its hardware address is 87H. PCON is not bit addressable.

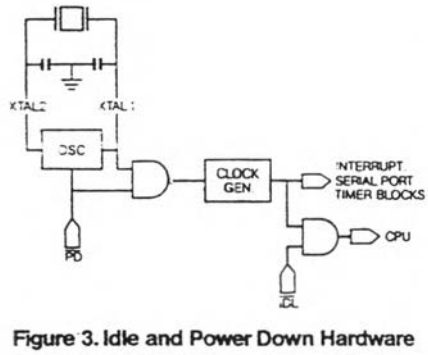


Figure 3. Idle and Power Down Hardware

PCON: Power Control Register

(MSB) (LSB)

SMOD	–	–	–	GF1	GF0	PD	IDL

Symbol	Position	Name and Function
SMOD	PCON.7	Double Baud rate bit. When set to a 1, the baud rate is doubled when the serial port is being used in either modes 1, 2 or 3.
–	PCON.6	(Reserved)
–	PCON.5	(Reserved)
–	PCON.4	(Reserved)
GF1	PCON.3	General-purpose flag bit.
GF0	PCON.2	General-purpose flag bit.
PD	PCON.1	Power Down bit. Setting this bit activates power down operation.
IDL	PCON.0	Idle mode bit. Setting this bit activates idle mode operation.

If 1's are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is (0XXXC000).

Table 1. Status of the external pins during Idle and Power Down modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

IDLE MODE

The instruction that sets PCON.0 is the last instruction executed before the Idle mode is activated. Once in the Idle mode the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM, and all other registers maintain their data during Idle. *Table 1* describes the status of the external pins during Idle mode.

There are two ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating Idle mode. The interrupt is serviced, and following RETI, the next instruction to be executed will be the one following theinstruction that wrote a 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the Idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an enabled interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle mode is with a hardware reset. Since the oscillator is still running, the hardware reset needs to be active for only 2 machine cycles (24 oscillator periods) to complete the reset operation.

POWER DOWN MODE

The instruction that sets PCON.1 is the last executed prior to entering power down. Once in power down, the oscillator is stopped. The contents of the onchip RAM and the Special Function Register is saved during power down mode. A hardware reset is the only way of exiting the power down mode. The hardware reset initiates the Special Function Register *(see Table 1)*.

In the Power Down mode, V_{CC} may be lowered to minimize circuit power consumption. Care must be taken to ensure the voltage is not reduced until the power down mode is entered, and that the voltage is restored before the hardware reset is applied which frees the oscillator. Reset should not be released until the oscillator has restarted and stabilized.

Table 1 describes the status of the external pins while in the power down-mode. It should be noted that if the power down mode is activated while in external program memory, the port data that is held in the Special Function Register P2 is restored to Port 2. If the data is a 1, the port pin is held high during the power down mode by the strong pullup, T1, shown in *Figure 4*.

STOP CLOCK MODE

Due to static design, the MHS 80C31/C51 clock speed can be reduced until 0 MHz without any data loss in memory or registers. This mode allows step by step utilization, and permits to reduce system power consumption by bringing the clock frequency down to any value. At 0 MHz, the power consumption is the same as in the Power Down Mode.

80C51 I/O PORTS

The I/O port drive of the 80C51 is similar to the 8051. The I/O buffers for Ports 1, 2, and 3 are implemented as shown in *figure 4*.

When the port latch contains a 0, all pFETS in *figure 4* are off while the nFET is turned on. When the port latch makes a 0-to-1 transition, the nFET turns off. The strong pullup pFET, T1, turns on for two oscillator periods, pulling the output high very rapidly. As the output line is drawn high, pFET T3 turns on through the inverter to supply the I_{OH} source current. This inverter and T3 form a latch which holds the 1 and is supported by T2. When Port 2 is used as an address port, for access to external program of data memory, any address bit that contains a 1 will have his strong pullup turned on for the entire duration of the external memory access.

When an I/O pin on Ports 1, 2, or 3 is used as an input, the user should be aware that the external circuit must sink current during the logical 1-to-0 transition. The maximum sink current is specified as ITL under the D.C. Specifications. When the input goes below approximately 2V, T3 turns off to save ICC current. Note, when returning to a logical 1, T2 is the only internal pullup that is on. This will result in a slow rise time if the user's circuit does not force the input line high.

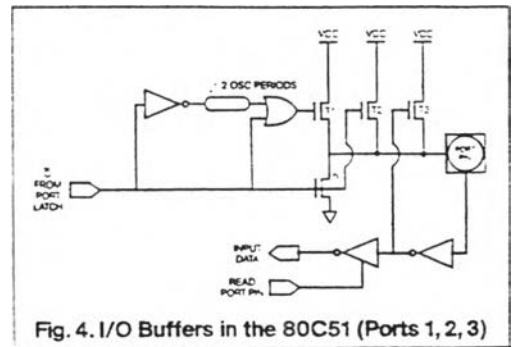


Fig. 4. I/O Buffers in the 80C51 (Ports 1, 2, 3)

80C51 PIN DESCRIPTIONS

V_{SS}
Circuit ground potential

V_{CC}
Supply voltage during normal, Idle, and Power Down operation.

Port 0
Port 0 is an 8-bit open drain bi-directional I/O port. Port 0 pins that have 1's written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1's. Port 0 also outputs the code bytes during program verification in the 80C51. External pullups are required during program verification. Port 0 can sink eight LS TTL inputs.

Port 1
Port 1 is an 8-bit bi-directional I/O port with internal pullups. Port 1 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the internal pullups.

Port 1 also receives the low-order address bytes during program verification. In the 80C51, Port 1 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

Port 2
Port 2 is an 8-bit bi-directional I/O port with internal pullups. Port 2 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the internal pullups. Port 2 emits the high-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pullups when emitting 1's. During accesses to external Data Memory that uses 8-bit addresses (MOVX @ Ri), Port 2 emits the contents of the P2 Special Function Register.

It also receives the high-order address bits and control signals during progam verification in the 80C51. Port 2 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

Port 3
Port 3 is an 8-bit bi-directional I/O port with internal pullups. Port 3 pins that have 1's written to them are pulled high by the internal pullups, and in that state can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (IIL, on the data sheet) because of the pullups. It also serves the functions of various special features of the MCS-51 Family, as listed below:

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	INT0 (external interrupt 0)
P3.3	INT1 (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{WR}$ (external Data Memory write strobe)
P3.7	$\overline{RD}$ (external Data Memory read strobe)

Port 3 can sink/source three LS TTL inputs. It can drive CMOS inputs without external pullups.

RST
A high level on this for two machine cycles while the oscillator is running resets the device. An internal pull-down resistor permits Power-On reset using only a capacitor connected to V_{CC}.

ALE
Address Latch Enable output for latching the low byte of the address during accesses to external memory. ALE is activated as though for this purpose at a constant rate of 1/6 the oscillator frequency except during an external data memory access at which time one ALE pulse is skipped. ALE can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

$\overline{PSEN}$
Program Store Enable output is the read strobe to external Program Memory. PSEN is activated twice each machine cycle during fetches from external Program Memory. (However, when executing out of external Program Memory, two activations of PSEN are skipped during each access to external Data Memory). PSEN is not activated during fetches from internal Program Memory. PSEN can sink/source 8 LS TTL inputs. It can drive CMOS inputs without an external pullup.

$\overline{EA}$
When EA is held high, the CPU executes out of internal Program Memory (unless the Program Counter exceeds OFFFH). When EA is held low, the CPU executes only out of external Program Memory. EA must not be floated.

XTAL1
Input to the inverting amplifier that forms the oscillator. Receives the external oscillator signal when an external oscillator is used.

XTAL2
Output of the inverting amplifier that forms the oscillator, and input to the internal clock generator. This pin should be floated when an external oscillator is used.

OSCILLATOR CHARACTERISTICS

XTAL1 and XTAL2 are the input and output respectively, of an inverting amplifier which is configured for use as an on-chip oscillator, as shown in figure 5. Either a quartz crystal or ceramic resonator may be used.
To drive the device from an external clock source, XTAL1 should be driven while XTAL2 is left unconnected as shown in *figure 6*. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum high and low times specified on the Data Sheet must be observed.

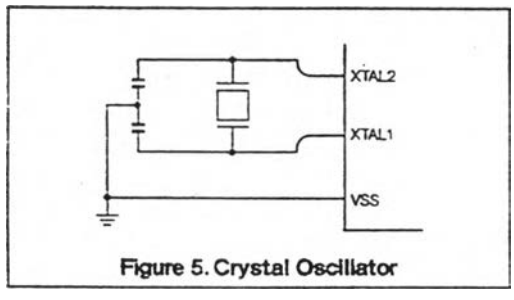


Figure 5. Crystal Oscillator

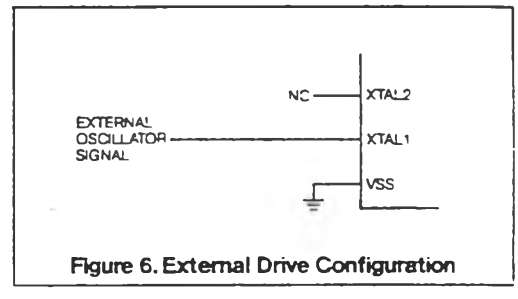


Figure 6. External Drive Configuration

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias:
Commercial ..... 0°C to 70°C
Industrial ..... −40°C to 85°C
Storage Temperature ..... −65°C to +150°C
Voltage on V_{CC} to V_{SS} ..... −0.5V to +7V
Voltage on Any Pin to V_{SS} ..... −0.5V to V_{CC} +0.5V
Power Dissipation 1W*

* This value is based on the maximum allowable die temperature and the thermal resistance of the package.

***NOTICE:**

Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

DC CHARACTERISTICS

T_A = −40°C to 85°C; V_{CC} = 2.7V to 6V; V_{SS} = 0V; F = 0 to 6 MHz

Symbol	Parameter	Min	Max	Unit	Test Conditions
VIL	Input Low Voltage	−0.5	0.2 V_{CC} −0.1	V	
VIH	Input High Voltage (Except XTALs and RST)	0.2 V_{CC} −0.9	V_{CC} −0.5	V	
VIH1	Input High Voltage to RST for Reset	0.7 V_{CC}	V_{CC} −0.5	V	
VIH2	Input High Voltage To XTAL 1	0.7 V_{CC}	V_{CC} −0.5	V	
VPD	Power Down voltage To V_{CC} in PD Mode	2.0	6.0	V	
VOL	Output Low Voltage (Ports 1, 2, 3)		0.45	V	IOL = 1.6mA (note 1)
VOL1	Output Low Voltage Port 0, ALE, $\overline{PSEN}$		0.45	V	IOL = 3.2mA (note 1)
VOH	Output High Voltage Ports 1, 2, 3	0.9 V_{CC}		V	IOH = −10μa
		2.4		V	IOH = −60μA V_{CC} = 5V ± 10%
VOH1	Output High Voltage (Port 0 in External in External Bus Mode), ALE, $\overline{PSEN}$	0.9 V_{CC}		V	IOH = −40μA
		2.4		V	IOH = −400μA V_{CC} = 5V ± 10%
IIL	Logical 0 Input Current Ports 1,2,3		−50	μA	Vin = 0.45V
ILI	Input Leakage Current		± 10	μA	0.45 < Vin < V_{CC}
ITL	Logical 1 to 0 Transition Current (Ports 1, 2, 3)		−500	μA	Vin = 2.0V
ICCPD	Power Supply Current (Power Down Mode)	50	10	μA	V_{CC} = 2.0V to 5.5V (note 2)
RRST	RST Pulldown Resistor	50	150	kΩ	
CIO	Capacitance of I/O Buffer		10	pF	f_C = 1MHz, T_A = 25°C

Note 1:

Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading 100 pF), the noise pulse on the ALE line may exceed 0.45V with maxi V_{OL} peak 0.6V. A Schmitt Trigger use is not necessary.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias:
Commercial ..... 0 °C to 70 °C
Industrial ..... −40 °C to 85 °C
Storage Temperature ..... −65 °C to +150 °C
Voltage on V_{CC} to V_{SS} ..... −0.5V to +7V
Voltage on Any Pin to V SS..... −0.5V to V_{CC} +0.5V
Power Dissipation 1W*

* This value is based on the maximum allowable die temperature and the thermal resistance of the package.

***NOTICE:**

Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

DC CHARACTERISTICS

TA = −40 °C to 85 °C; VCc = 2.7V to 6V; VSS = 0V; F = 0 to 6 MHz

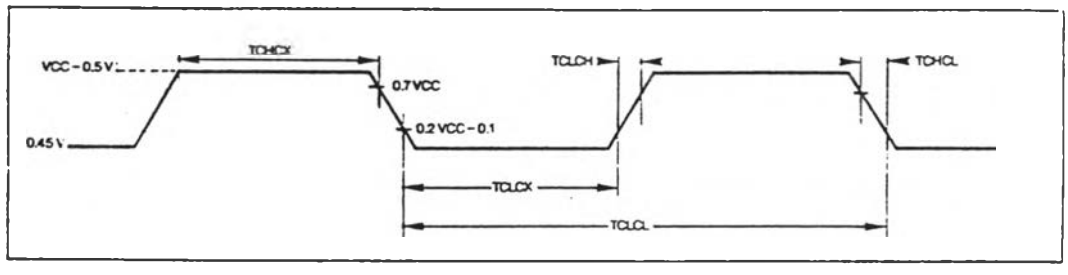
Symbol	Parameter	Min	Max	Unit	Test Conditions
VIL	Input Low Voltage	−0.5	0.2 V_{CC} −0.1	V	
VIH	Input High Voltage (Except XTALs and RST)	0.2 V_{CC} −0.9	V_{CC} +0.5	V	
VIH1	Input High Voltage to RST for Reset	0.7 V_{CC}	V_{CC} +0.5	V	
VIH2	Input High Voltage To XTAL 1	0.7 V_{CC}	V_{CC} +0.5	V	
VPD	Power Down Voltage To V_{CC} in PD Mode	2.0	5.0	V	
VOL	Output Low Voltage (Ports 1, 2, 3)		0.45	V	IOL = 1.6mA (note 1)
VOL1	Output Low Voltage Port 0, ALE, $\overline{PSEN}$		0.45	V	IOL = 3.2mA (note 1)
VOH	Output High Voltage Ports 1, 2, 3	0.9 V_{CC}		V	IOH = −10µa
		2.4		V	IOH = −60µA V_{CC} = 5V ± 10%
VOH1	Output High Voltage (Port 0 in External in External Bus Mode), ALE, $\overline{PSEN}$	0.9 V_{CC}		V	IOH = −40µA
		2.4		V	IOH = −400µA V_{CC} = 5V ± 10%
IIL	Logical 0 Input Current Ports 1,2,3		−50	µA	Vin = 0.45V
ILI	Input Leakage Current		± 10	µA	0.45 < Vin < V_{CC}
ITL	Logical 1 to 0 Transition Current (Ports 1, 2, 3)		−500	µA	Vin = 2.0V
ICCPD	Power Supply Current (Power Down Mode)	50	10	µA	V_{CC} = 2.0V to 5.5V (note 2)
RRST	RST Pulldown Resistor	50	150	kΩ	
CIO	Capacitance of I/O Buffer		10	pF	f_C = 1MHz, T_A = 25 °C

Note 1:

Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading 100 pF), the noise pulse on the ALE line may exceed 0.45V with maxi V_{OL} peak 0.6V. A Schmitt Trigger use is not necessary.

EXTERNAL CLOCK DRIVE CHARACTERISTICS (XTAL 1)

Symbol	Parameter	Variable Clock freq = 0 to 6 MHz		Unit
		Min	Max	
TCLCL	Oscillator Period	166		ns
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns



AC CHARACTERISTICS

(T_A = −40°C to 85°C, V_{CC} = 2.7 V to 6V, V_{SS} = 0V)
(Load Capacitance for Port 0, ALE, and PSEN = 100pf; Load Capacitance for All Other Outputs = 80pf)

EXTERNAL PROGRAM MEMORY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
TLHLL	ALE Pulse Width	2TCLCL − 40		ns
TAVLL	Address Valid to ALE	TCLCL − 55		ns
TLLAX	Address Hold After ALE	TCLCL − 35		ns
TLLIV	ALE to Valid instr In		4TCLCL − 170	ns
TLLPL	ALE to $\overline{PSEN}$	TCLCL − 25		ns
TPLPH	$\overline{PSEN}$ Pulse Width	3TCLCL − 35		ns
TPLIV	$\overline{PSEN}$ to Valid Instr In		3TCLCL − 220	ns
TPXIX	Input Instr Hold After $\overline{PSEN}$	0		ns
TPXIZ	Input Instr Float After $\overline{PSEN}$		TCLCL − 20	ns
TPXAV	$\overline{PSEN}$ to Address Valid	TCLCL − 8		ns
TAVIV	Address to Valid Instr In		5TCLCL − 220	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		0	ns

See next page for External Data Memory Characteristics.

EXTERNAL DATA MEMORY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units
TRLRH	RD Pulse Width	6TCLCL – 100		ns
TWLWH	WR Pulse Width	6TCLCL – 100		ns
TLLAX	Data Address Hold After ALE	TCLCL – 35		ns
TRLDV	RD to Valid Data In		5TCLCL – 165	ns
TRHDX	Data Hold After RD	0		ns
TRHDZ	Data Float After RD		2TCLCL – 70	ns
TLLDV	ALE to Valid Data In		8TCLCL – 150	ns
TAVDV	Address to Valid Data In		9TCLCL – 165	ns
TLLWL	ALE to WR or RD	3TCLCL – 50	3TCLCL + 50	ns
TAVWL	Address to WR or RD	4TCLCL – 130		ns
TQVWX	Data Valid to WR Transition	TCLCL – 60		ns
TQVWH	Data Setup to WR High	7TCLCL – 150		ns
TWHQX	Data Hold After WR	TCLCL – 50		ns
TRLAZ	RD Low to Address Float		0	ns
TWHLH	RD or WR High to ALE High	TCLCL – 40	TCLCL – 40	ns

MAXIMUM I_{CC} (mA)

	Operating (Note 3)			Idle (Note 4)		
Freq. V_{CC}	2.7V	5V	6V	2.7V	5V	6V
1 MHz	0.8 mA	1.5 mA	1.8 mA	400 µA	800 µA	1 mA
6 MHz	4 mA	8 mA	10 mA	1.2 mA	3.5 mA	3.8 mA

Note 2:

Power Down I_{CC} is measured with all output pins disconnected; EA = Port 0 = V_{CC}; XTAL2 N.C.; RST = V_{SS}

Note 3:

I_{CC} is measured with all output pins disconnected; XTAL1 driven with TCLCH, TCHCL = 5 ns, $V_{IL} = V_{SS} - 0.5V$; $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C.; EA = RST = Port 0 = V_{CC}. I_{CC} would be slightly higher if a crystal oscillator used.

Note 4:

Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven TCLCH, TCHCL = 5 ns, $V_{IL} = V_{SS} - 0.5V$; $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C.; Port 0 = V_{CC}; EA = RST = V_{SS}.

EXPLANATION OF THE AC SYMBOLS

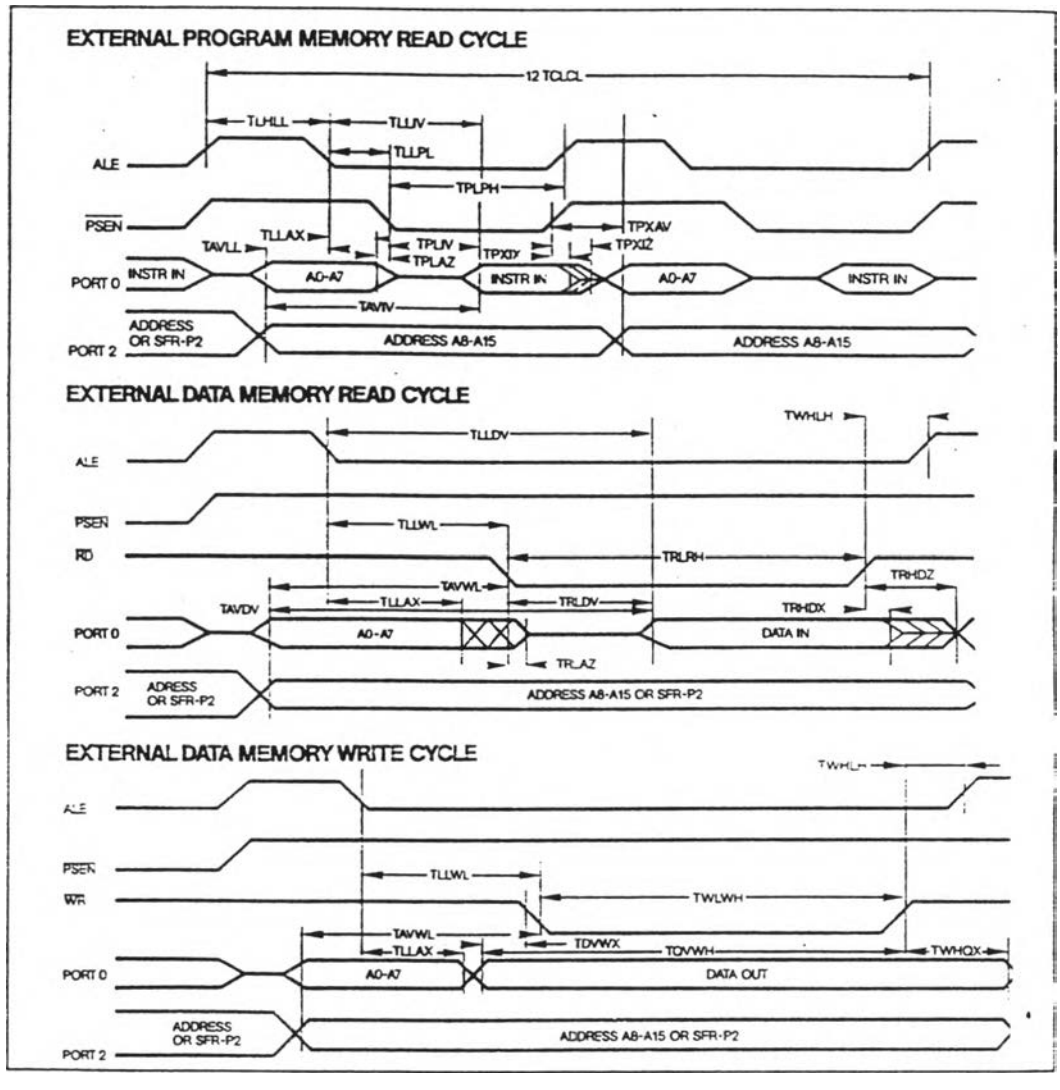
Each timing symbol has 5 characters. The first character is always a 'T' (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list all the characters and what they stand for.

A: Address.
C: Clock.
D: Input data.
H: Logic level HIGH.
I: Instruction (program memory contents).
L: Logic level LOW, or ALE.
P: PSEN
Q: Output data.
R: READ signal.
T: Time.
V: Valid.
W: WRITE signal.
X: No longer a valid logic level.
Z: Float.

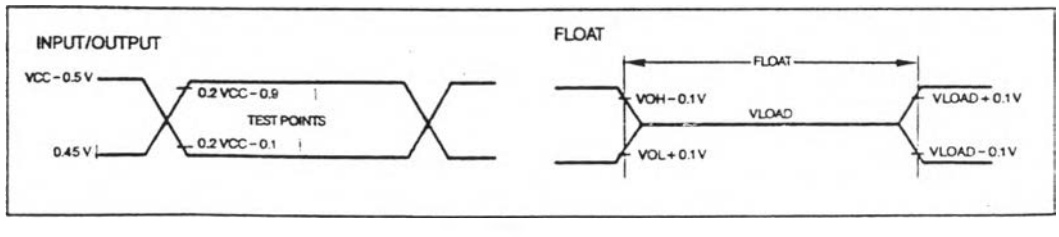
EXAMPLE:

TAVLL = Time for Address Valid to ALE low.
TLLPL = Time for ALE low to PSEN low

AC TIMING DIAGRAMS



AC TESTING INPUT/OUTPUT, FLOAT WAVEFORMS



AC inputs during testing are driven at V_{CC} – 0.5 for a logic "1" and 0.45V for a logic "0". Timing measurements are made at VIH min for a logic "1" and VIL max for a logic "0". For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded VOH/VOL level occurs. Iol/IoH ≥ ± 20 Ma.

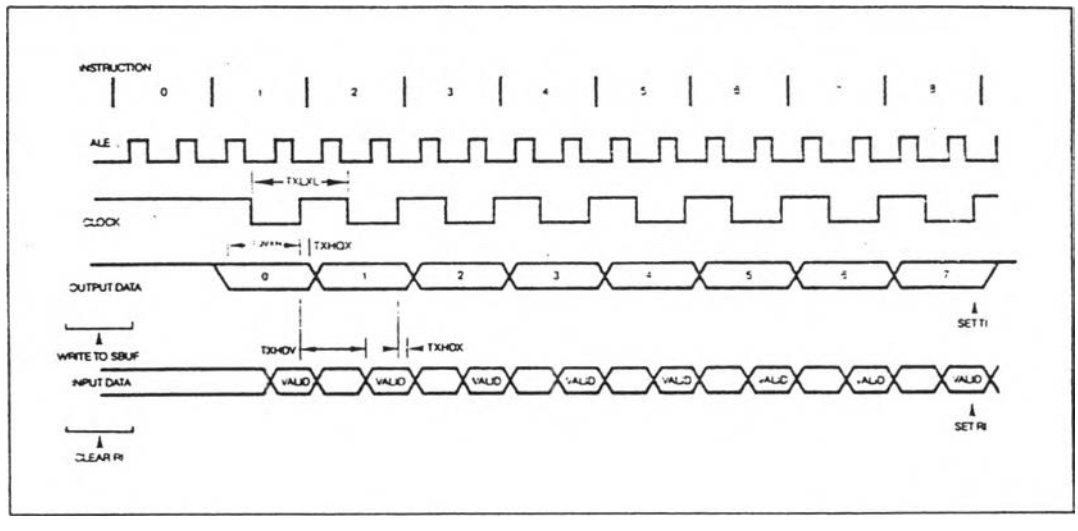
SERIAL PORT TIMING - SHIFT REGISTER MODE

A.C. CHARACTERISTICS:

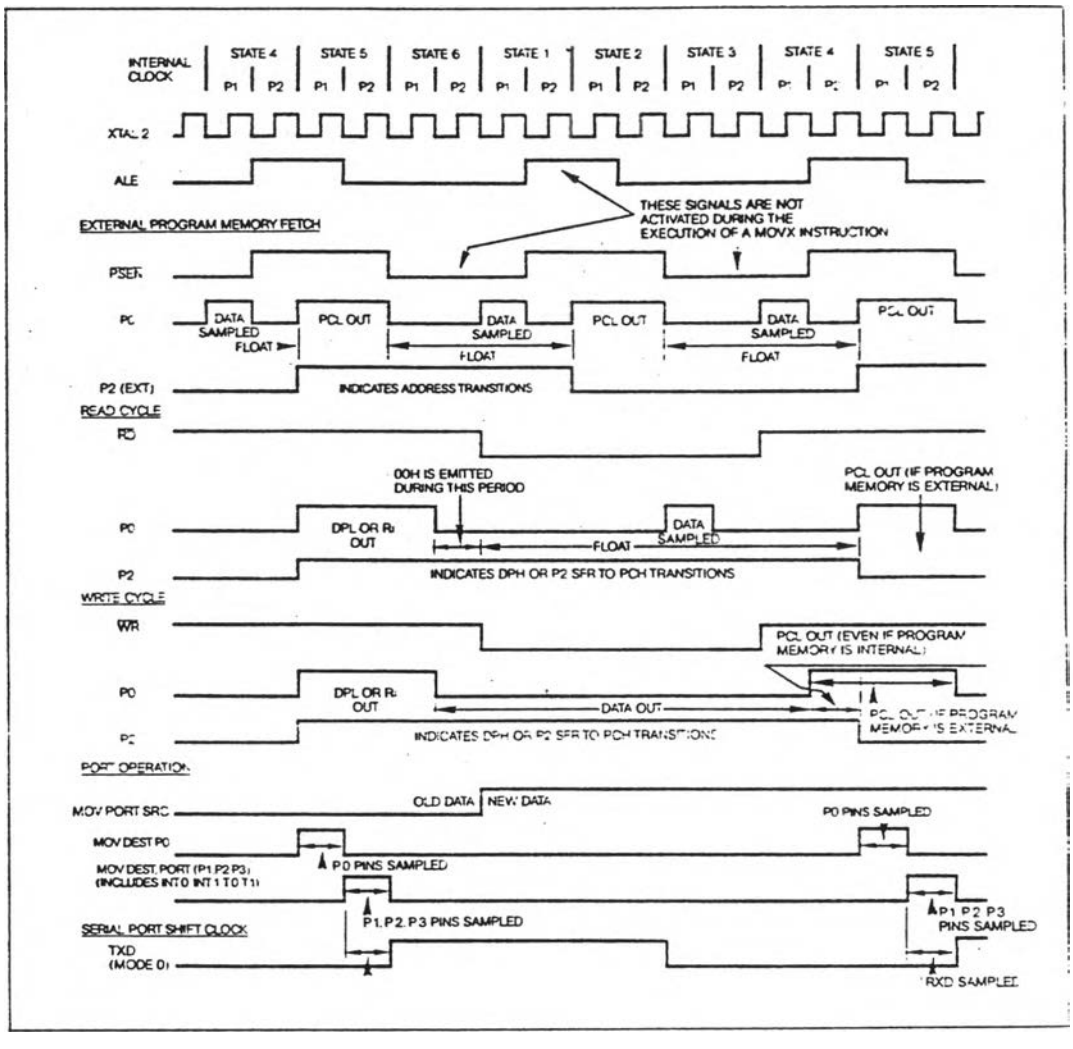
(T_A = 0°C to 70°C; V_{SS} = 0V; V_{CC} = 2.7V to 6V; Load Capacitance = 80 pF)

Symbol	Parameter	Min	Max	Units
TXLXL	Serial Port Clock Cycle Time	12TCLCL		µs
TQVXH	Output Data Setup to Clock Rising Edge	10TCLCL-133		ns
TXHQX	Output Data Hold After Clock Rising Edge	2TCLCL-117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		ns
TXHDV	Clock Rising Edge to Input Data Valid		10TLCL-133	ns

SHIFT REGISTER TIMING WAVEFORMS



CLOCK WAVEFORMS



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though ($T_A = 25°C$ fully loaded) RD and WR propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

Table 1. MCS®-51 Instruction Set Description

ARITHMETIC OPERATIONS

Mnemonic		Description	Byte	Cyc
ADD	A,Rn	Add register to Accumulator	1	1
ADD	A,direct	Add direct byte to Accumulator	2	1
ADD	A,@Ri	Add indirect RAM to Accumulator	1	1
ADD	A,#data	Add immediate data to Accumulator	2	1
ADDC	A,Rn	Add register to Accumulator with Carry	1	1
ADDC	A,direct	Add direct byte to A with Carry flag	2	1
ADDC	A,@Ri	Add indirect RAM to A with Carry flag	1	1
ADDC	A,#data	Add immediate data to A with Carry flag	2	1
SUBB	A,Rn	Subtract register from A with Borrow	1	1
SUBB	A,direct	Subtract direct byte from A with Borrow	2	1
SUBB	A,@Ri	Subtract indirect RAM from A with Borrow	1	1
SUBB	A,#data	Subtract immed. data from A with Borrow	2	1
INC	A	Increment Accumulator	1	1
INC	Rn	Increment register	1	1
INC	direct	Increment direct byte	2	1
INC	@Ri	Incriment indirect RAM	1	1
INC	DPTR	Incriment Data Pointer	1	2
DEC	A	Decrement Accumulator	1	1
DEC	Rn	Decrement register	1	1
DEC	direct	Decrement direct byte	2	1
DEC	@Ri	Decrement indirect RAM	1	1
MUL	AB	Multiply A & B	1	4
DIV	AB	Divide A by B	1	4
DA	A	Decimal Adjust Accumulator	1	1

LOGICAL OPERATIONS

Mnemonic		Destination	Byte	Cyc
ANL	A,Rn	AND register to Accumulator	1	1
ANL	A,direct	AND direct byte to Accumulator	2	1
ANL	A,@Ri	AND indirect RAM to Accumulator	1	1
ANL	A,#data	AND immediate data to Accumulator	2	1
ANL	direct,A	AND Accumulator to direct byte	2	1
ANL	direct,#data	AND immediate data to direct byte	3	2
ORL	A,Rn	OR register to Accumulator	1	1
ORL	A,direct	OR direct byte to Accumulator	2	1
ORL	A,@Ri	OR indirect RAM to Accumulator	1	1
ORL	A,#data	OR immediate data to Accumulator	2	1
ORL	direct,A	OR Accumulator to direct byte	2	1
ORL	direct,#data	OR immediate data to direct byte	3	2
XRL	A,Rn	Exclusive-OR register to Accumulator	1	1
XRL	A,direct	Exclusive-OR direct byte to Accumulator	2	1
XRL	A,@Ri	Exclusive-OR indirect RAM to A	1	1
XRL	A,#data	Exclusive-OR immediate data to A	2	1
XRL	direct,A	Exclusive-OR Accumulator to direct byte	2	1
XRL	direct,#data	Exclusive-OR immediate data to direct	3	2
CLR	A	Clear Accumulator	1	1
CPL	A	Complement Accumulator	1	1
RL	A	Rotate Accumulator Left	1	1
RLC	A	Rotate A Left through the Carry flag	1	1
RR	A	Rotate Accumulator Right	1	1
RRC	A	Rotate A Right through Carry flag	1	1
SWAP	A	Swap nibbles within the Accumulator	1	1

Table 1. (Cont.)

DATA TRANSFER

Mnemonic		Description	Byte	Cyc
MOV	A,Rn	Move register to Accumulator	1	1
MOV	A,direct	Move direct byte to Accumulator	2	1
MOV	A,@Ri	Move indirect RAM to Accumulator	1	1
MOV	A,#data	Move immediate data to Accumulator	2	1
MOV	Rn,A	Move Accumulator to register	1	1
MOV	Rn,direct	Move direct byte to register	2	2
MOV	Rn,#data	Move immediate data to register	2	1
MOV	direct,A	Move Accumulator to direct byte	2	1
MOV	direct,Rn	Move register to direct byte	2	2
MOV	direct,direct	Move direct byte to direct	3	2
MOV	direct,@Ri	Move indirect RAM to direct byte	2	2
MOV	direct,#data	Move immediate data to direct byte	3	2
MOV	@Ri,A	Move Accumulator to indirect RAM	1	1
MOV	@Ri,direct	Move direct byte to indirect RAM	2	2
MOV	@Ri,#data	Move immediate data to indirect RAM	2	1
MOV	DPTR,#data 16	Load Data Pointer with a 16-bit constant	3	2
MOVC	A,@A+DPTR	Move Code byte relative to DPTR to A	1	2
MOVC	A,@A+PC	Move Code byte relative to PC to A	1	2
MOVX	A,@Ri	Move External RAM (8-bit addr) to A	1	2
MOVX	A,@DPTR	Move External RAM (16-bit addr) to A	1	2
MOVX	@Ri,A	Move A to External RAM (8-bit addr)	1	2
MOVX	@DPTR,A	Move A to External RAM (16-bit addr)	1	2
PUSH	direct	Push direct byte onto stack	2	2
POP	direct	Pop direct byte form stack	2	2
XCH	A,Rn	Exchange register with Accumulator	1	1
XCH	A,direct	Exchange direct byte with Accumulator	2	1
XCH	A,@Ri	Exchange indirect RAM with A	1	1
XCHD	A,@Ri	Exchange low-order nibble ind RAM with A	1	1

BOOLEAN VARIABLE MANIPULATION

Mnemonic		Description	Byte	Cyc
CLR	C	Clear Carry flag	1	1
CLR	bit	Clear direct bit	2	1
SETB	C	Set Carry flag	1	1
SETB	bit	Set direct Bit	2	1
CPL	C	Complement Carry flag	1	1
CPL	bit	Complement direct bit	2	1
ANL	C,bit	AND direct bit to Carry flag	2	2
ANL	C,/ bit	AND complement of direct bit to Carry	2	2
ORL	C,bit	OR direct bit to Carry flag	2	2
ORL	C,/ bit	OR complement of direct bit to Carry	2	2
MOV	C,bit	Move direct bit to Carry flag	2	1
MOV	bit,C	Move Carry flag to direct bit	2	2

PROGRAM AND MACHINE CONTROL

Mnemonic		Description	Byte	Cyc
ACALL	addr 11	Absolute Subroutine Call	2	2
LCALL	addr 16	Long Subroutine Call	3	2
RET		Return from subroutine	1	2
RETI		Return from interrupt	1	2
AJMP	addr 11	Absolute Jump	2	2
LJMP	addr 16	Long Jump	3	2
SJMP	rel	Short Jump (relative addr)	2	2
JMP	@A+DPTR	Jump indirect relative to the DPTR	1	2
JZ	rel	Jump if Accumulator is Zero	2	2
JNZ	rel	Jump if Accumulator is Not Zero	2	2
JC	rel	Jump if Carry flag is set	2	2
JNC	rel	Jump if No Carry flag	2	2

Table 1. (Cont.)

PROGRAM AND MACHINE CONTROL (cont.)

Mnemonic		Description	Byte	Cyc
JB	bit,rel	Jump if direct Bit set	3	2
JNB	bit,rel	Jump if direct Bit Not set	3	2
JBC	bit,rel	Jump if direct Bit is set & Clear bit	3	2
CJNE	A,direct,rel	Compare direct to A & Jump if Not Equal	3	2
CJNE	A,#data,rel	Comp. immed. to A & Jump if Not Equal	3	2
CJNE	Rn,#data,rel	Comp. immed. to reg & Jump if Not Equal	3	2
CJNE	@Ri,#data. rel	Comp. immed. to ind. & Jump if Not Equal	3	2
DJNZ	Rn,rel	Decrement register & Jump if Not Zero	2	2
DJNZ	direct. rel	Decrement direct & Jump if Not Zero	3	2
NOP		No operation	1	1

Notes on data addressing modes:

Rn	– Working register R0-R7
direct	– 128 internal RAM locations, any I/O port, control or status register
@Ri	– Indirect internal RAM location addressed by register R0 or R1
#data	– 8-bit constant included in instruction
#data 16	– 16-bit constant included as bytes 2 & 3 of instruction
bit	– 128 software flags, any I/O pin, control or status bit

Notes on program addressing modes:

addr 16	– Destination address for LCALL & LJMP may be anywhere within the 64-k program memory address space
addr 11	– Destination address for ACALL & AJMP will be within the same 2-k page of program memory as the first byte of the following instruction
rel	– SJMP and all conditional jumps include an 8-bit offset byte. Range is +127–128 bytes relative to first byte of the following instruction.

Table 2. Instruction Opcodes In Hexadecimal Order

Hex Code	Number of Bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	code addr
02	3	LJMP	code addr
03	1	RR	A
04	1	INC	A
05	2	INC	data addr
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	bit addr,code addr
11	2	ACALL	code addr
12	3	LCALL	code addr
13	1	RRC	A
14	1	DEC	A
15	2	DEC	data addr
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	bit addr,code addr
21	2	AJMP	code addr
22	1	RET	
23	1	RL	A
24	2	ADD	A,data
25	2	ADD	A,data addr
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	bit addr,code addr
31	2	ACALL	code addr
32	1	RETI	

Hex Code	Number of Bytes	Mnemonic	Operands
33	1	RLC	A
34	2	ADDC	A,#data
35	2	ADDC	A,data addr
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R6
3F	1	ADDC	A,R7
40	2	JC	code addr
41	2	AJMP	code addr
42	2	ORL	data addr,A
43	3	ORL	data addr,#data
44	2	ORL	A,#data
45	2	ORL	A,data addr
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	code addr
51	2	ACALL	code addr
52	2	ANL	data addr,A
53	3	ANL	data addr,#data
54	2	ANL	A,#data
55	2	ANL	A,data addr
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	code addr
61	2	AJMP	code addr
62	2	XRL	data addr,A
63	3	XRL	data addr,#data
64	2	XRL	A,#data
65	2	XRL	A,data addr

Table 2. (Cont.)

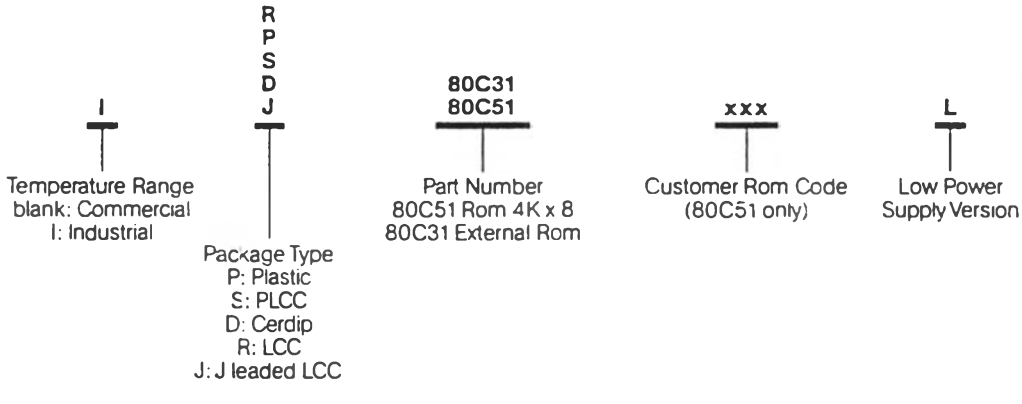
Hex Code	Number of Bytes	Mnemonic	Operands
66	1	XRL	A,@R0
67	1	XRL	A,@R1
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	code addr
71	2	ACALL	code addr
72	2	ORL	C,bit addr
73	1	JMP	@A+DPTR
74	2	MOV	A,#data
75	3	MOV	data addr,#data
76	2	MOV	@R0,#data
77	2	MOV	@R1,#data
78	2	MOV	R0,#data
79	2	MOV	R1,#data
7A	2	MOV	R2,#data
7B	2	MOV	R3,#data
7C	2	MOV	R4,#data
7D	2	MOV	R5,#data
7E	2	MOV	R6,#data
7F	2	MOV	R7,#data
80	2	SJMP	code addr
81	2	AJMP	code addr
82	2	ANL	C,bit addr
83	1	MOVC	A,@A+PC
84	1	DIV	AB
85	3	MOV	data addr,data addr
86	2	MOV	data addr,@R0
87	2	MOV	data addr,@R1
88	2	MOV	data addr,R0
89	2	MOV	data addr,R1
8A	2	MOV	data addr,R2
8B	2	MOV	data addr,R3
8C	2	MOV	data addr,R4
8D	2	MOV	data addr,R5
8E	2	MOV	data addr,R6
8F	2	MOV	data addr,R7
90	3	MOV	DPTR,#data
91	2	ACALL	code addr
92	2	MOV	bit addr,C
93	1	MOVC	A,@A+DPTR
94	2	SUBB	A,#data
95	2	SUBB	A,data addr
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0

Hex Code	Number of Bytes	Mnemonic	Operands
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,bit addr
A1	2	AJMP	code addr
A2	2	MOV	C,bit addr
A3	1	INC	DPTR
A4	1	MUL	AB
A5		reserved	
A6	2	MOV	@R0,data addr
A7	2	MOV	@R1,data addr
A8	2	MOV	R0,data addr
A9	2	MOV	R1,data addr
AA	2	MOV	R2,data addr
AB	2	MOV	R3,data addr
AC	2	MOV	R4,data addr
AD	2	MOV	R5,data addr
AE	2	MOV	R6,data addr
AF	2	MOV	R7,data addr
B0	2	ANL	C,bit addr
B1	2	ACALL	code addr
B2	2	CPL	bit addr
B3	1	CPL	C
B4	3	CJNE	A,#data,code addr
B5	3	CJNE	A,data addr,code addr
B6	3	CJNE	@R0,#data,code addr
B7	3	CJNE	@R1,#data,code addr
B8	3	CJNE	R0,#data,code addr
B9	3	CJNE	R1,#data,code addr
BA	3	CJNE	R2,#data,code addr
BB	3	CJNE	R3,#data,code addr
BC	3	CJNE	R4,#data,code addr
BD	3	CJNE	R5,#data,code addr
BE	3	CJNE	R6,#data,code addr
BF	3	CJNE	R7,#data,code addr
C0	2	PUSH	data addr
C1	2	AJMP	code addr
C2	2	CLR	bit addr
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,data addr
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3

Table 2. (Cont.)

Hex Code	Number of Bytes	Mnemonic	Operands
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7
D0	2	POP	data addr
D1	2	ACALL	code addr
D2	2	SETB	bit addr
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	data addr,code addr
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,code addr
D9	2	DJNZ	R1,code addr
DA	2	DJNZ	R2,code addr
DB	2	DJNZ	R3,code addr
DC	2	DJNZ	R4,code addr
DD	2	DJNZ	R5,code addr
DE	2	DJNZ	R6,code addr
DF	2	DJNZ	R7,code addr
E0	1	MOVX	A,@DPTR
E1	2	AJMP	code addr
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,data addr

Hex Code	Number of Bytes	Mnemonic	Operands
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	code addr
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	data addr,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A



ประวัติผู้เขียน

นายอำนวย สุดสาคร เกิดวันที่ 26 มีนาคม 2506 ที่จังหวัดชลบุรี สำเร็จการศึกษาปริญญาวิศวกรรมศาสตรบัณฑิต สาขาเทคโนโลยี ไฟฟ้าอุตสาหกรรม ปีการศึกษา 2531 จากสถาบันเทคโนโยีพระจอมเกล้า พระนครเหนือ เข้าศึกษาต่อที่ภาควิชานิวเคลียร์เทคโนโลยี คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย ในปี พ.ศ.2532

ประวัติการทำงาน

สถาบันบริการคอมพิวเตอร์ จุฬาลงกรณ์มหาวิทยาลัย ระหว่างปี พ.ศ.2526 ถึงปี พ.ศ.2530

องค์การโทรศัพท์แห่งประเทศไทย ตำแหน่งวิศวกร 5 ระหว่างปี พ.ศ.2530 ถึงปัจจุบัน