CHAPTER 5

Device Fabrication

The descriptions of the RW laser-diode fabrication process reported in this literature are the aim of this chapter. The process can be introduced by Fig. 5.1 which consists of 6 major steps. First, the epitaxy are grown on a GaAs substrate to create the transverse structure and the p-n junction. After that, the photolithography and chemically-etching process are performed to establish the ridges at the upper cladding layer. Next, the SiO_2 insulator is deposited on the entirely top surface. Then the stripes of insulator are removed for metal contact. Next, the mechanical lapping is used to decrease the substrate thickness for heat accumulation reduction. Finally, the metal contact is carried out by metallization and annealing process. The details of all steps are described in the following sections.

5.1 Epitaxy growth

The horizontal *liquid phase epitaxy* (LPE) growth technique is used in the work to provide the transverse DH structure. The LPE process is carried out by supercooling method [57] with the saturated temperature of 800°C, the precise cooling rate of 0.2°C per minute and the starting growth temperature of 797°C (ΔT = 3°C). Before epitaxy-growth starts, substrate etching is achieved by rising up the temperature of the contacting solution, starting from the saturated temperature to the etching temperature of 804°C. This etching process is used to remove the contamination on the substrate surface and also be used to prepare the nucleation site for epitaxy growth.

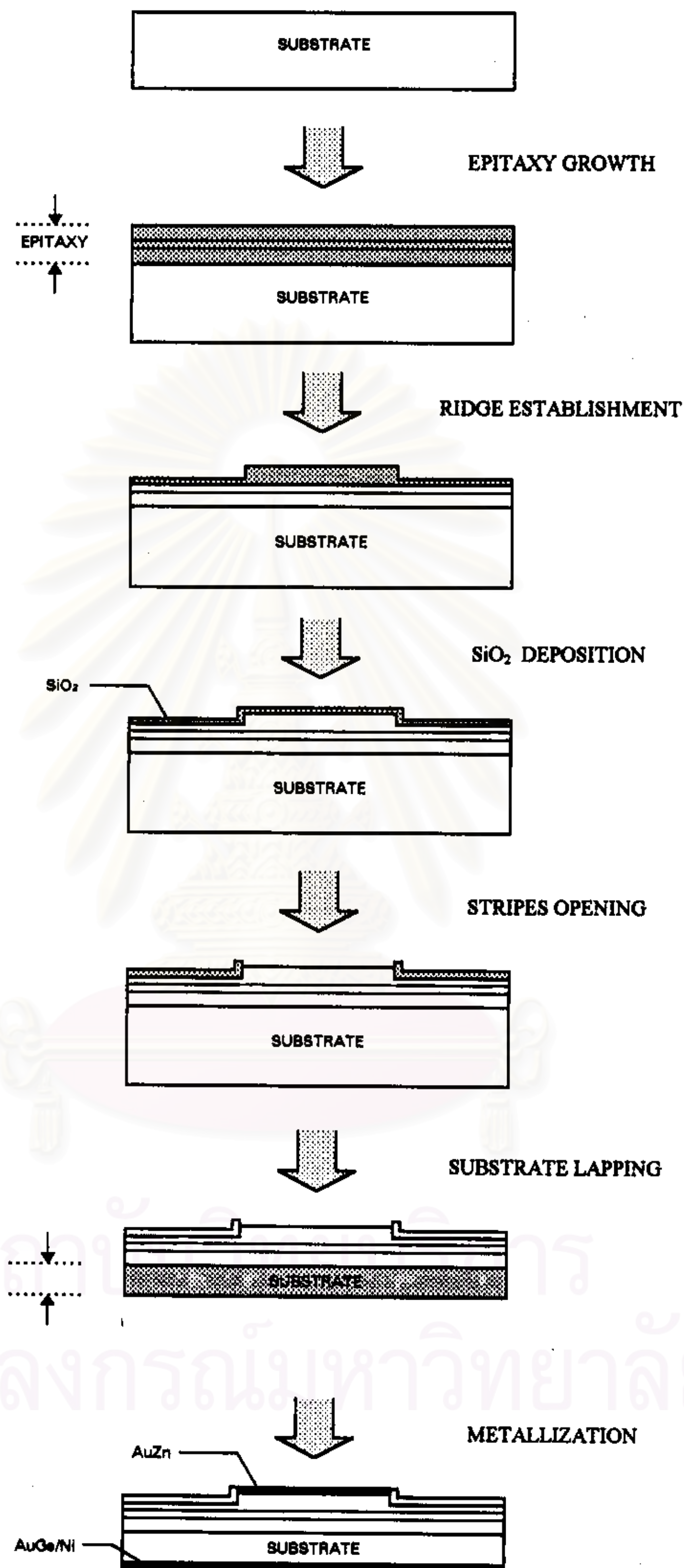

Fig. 5.1 Major steps of device fabrication. Shaded area designates the region applied by each step.

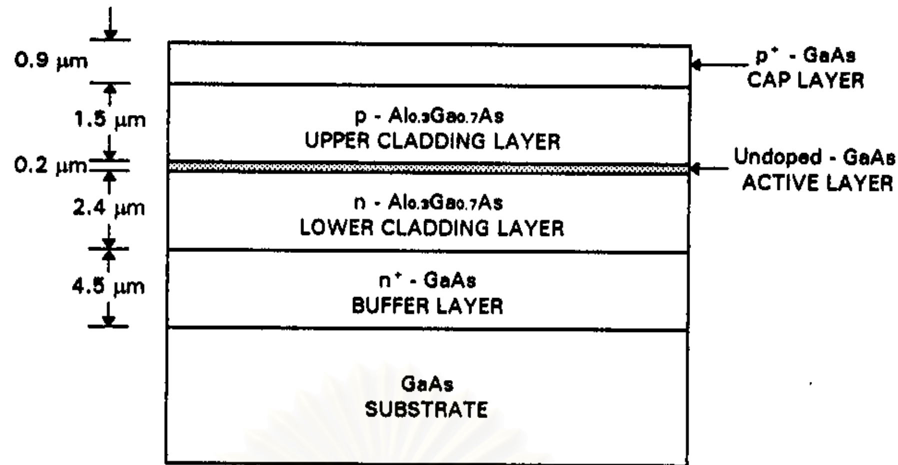

Fig. 5.2 Schematic of LPE epitaxy grown for the transverse DH laser diodes.

Fig. 5.2 illustrates typical schematic of epitaxy structure grown on the (100)-oriented n^+ GaAs substrate. The layer structure is composed by a n^+ GaAs buffer layer, a 2.4 μm thick n-$Al_{0.30}Ga_{0.70}As$ lower cladding layer, a 0.2 μm thick undoped GaAs active layer, a 1.5 μm thick p-$Al_{0.30}Ga_{0.70}As$ upper cladding layer and a 0.9 μm thick p^+-GaAs cap layer. The Al-content (x) of 0.30 used in both cladding layers provide the material refractive index of 3.40 calculated from the equation in [2] and [3] while the Al-free GaAs active layer provides the index of 3.62 .

The details and conditions of the solutions used for LPE epitaxy growth are shown as following.

Layer	Al (mg)	Dopant (mg)	Time (min)	Temperature start-stop	Al content	Carrier density	Thickness (μm)
Etching				800 - 804			
Buffer		Sn = 400		804 - 797		$n = 1\times10^{18}$	4.5
Cladding	2.0	Sn = 200	6		30%	$n = 1\times10^{17}$	2.4
Active			3 sec			undoped	0.2
Cladding	2.0	Ge = 40	4		30%	$p = 1\times10^{17}$	1.5
Cap		Ge = 80	20 sec			$p = 5\times10^{18}$	0.9

Note : The Ga solvent quantity of each solution is 2 g.

Fig. 5.3 shows the photograph from optical microscope of a grown sample fabricated by the above conditions. The figure reveals that the grown epitaxy corresponds to the desired thickness except the active layer of 0.2 μm thick which larger than the proposed thickness due to the LPE process.

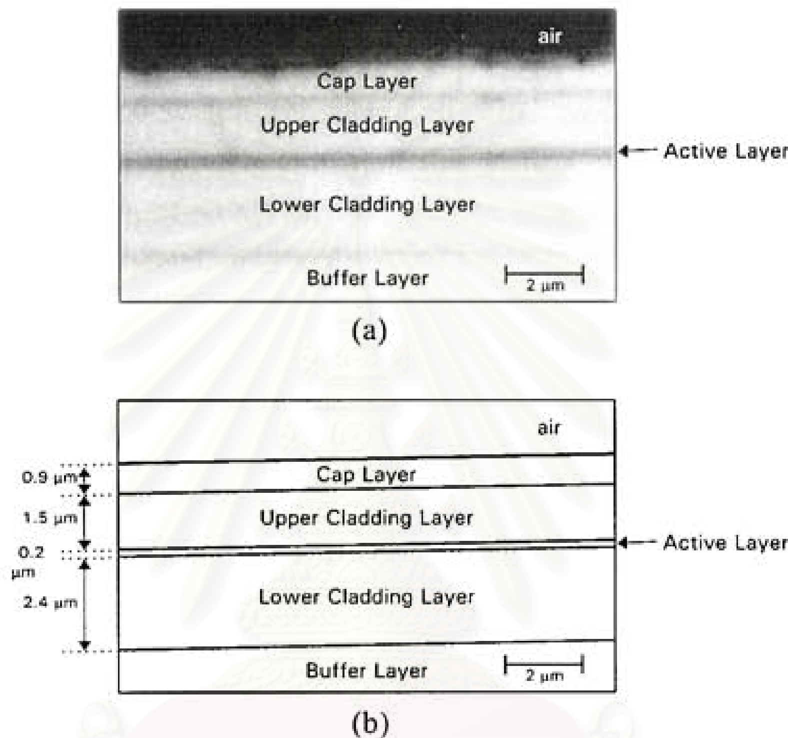

Fig. 5.3 (a) Cross-section photograph of an epitaxy-grown sample taken by the optical microscope and (b) schematic detail of the photograph to describe the thickness of each layer.

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5.2 Ridge establishment

The photolithography process is applied on the LPE samples to create the photoresist-mask stripes. A positive photoresist and developer named commercially *Shipley AZ-1350* and *Shipley MF-312* are used in the process while the rinse solution is the de-ionized (DI) water. The process is performed by the consequent conditions.

Spinning	500 rpm	for 5 second	(first stage)
	4,000 rpm	for 25 second	(second stage)
Prebake	90°C	for 5 minute	

Exposed time	30 second	at lamp power density of 1.1 mW/cm^2
Develop time	10 second	(1:1 diluted to DI water)
Rinse time	30 second	
Post bake	120°C for 5 minute	

After mask stripe has been created, wet-chemical etching is performed. The etchant of $H_2SO_4 : H_2O_2 : H_2O = 1 : 4 : 44$ was choosen from various etchants [31] which are shown in appendix. This solution is a non-selective etchant and its etch rate in <100> direction is 0.59 μm per minute at 27°C room temperature. Fig. 5.4 schematically illustrates the etch profile of this etchant which all dimensions are presented in the fraction of <100> etch depth. The etching time is 3 minute and 30 second under ultrasonic vibration to achieve 2.05 μm etch depth corresponding to 0.35 μm residual thickness.

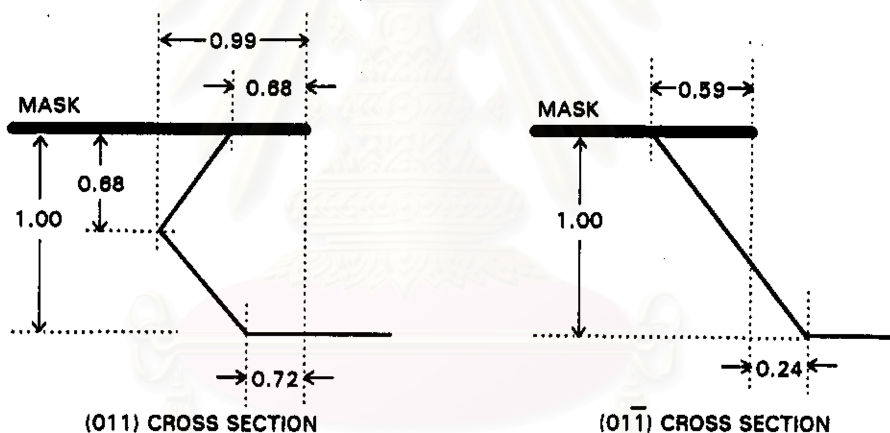

Fig. 5.4 Schematic of GaAs profile etched by $H_2SO_4 : H_2O_2 : H_2O = 1 : 4 : 44$. All dimensions are normalized by the etch depth in <100> direction.

A Chromium-on-glass mask is carefully selected to match the designed ridge dimensions. The stripe width of the mask must be 2.4 μm larger than the width of the required ridge because 59% of undercut occurs in each edge of the mask by the chemically-etching process (Fig. 5.4). And we also align the stripe direction corresponding to $\langle 01\bar{1} \rangle$ for conventional-mesa shape of the ridge in $(01\bar{1})$ cross section. An etched sample taken by the optical microscope is shown in Fig. 5.5 which shows the 4 μm ridge width as requiring.

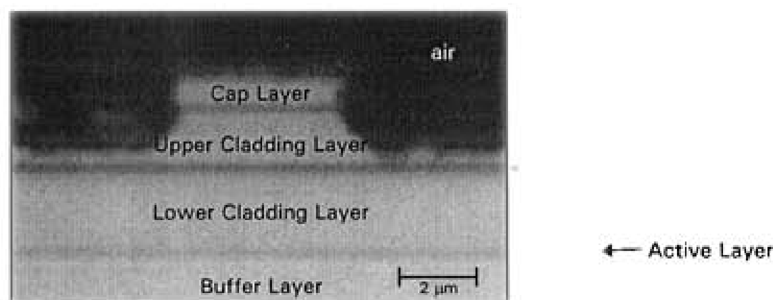

Fig. 5.5 Cross-section photograph of an etched sample taken by optical microscope.

Finally, the photoresist covered on the samples is removed by Acetone and the samples must be cleaned up for the consequent step.

5.3 SiO_2 deposition

The deposition of SiO_2 insulator is performed by the *electron-beam (EB) evaporator* which heats the SiO_2 source by electron bombardment and controls the beam by varied magnetic field. The machine working in SDRL has been installed the thickness monitoring module for real-time measurement of the film thickness. The SiO_2 film is deposited on the entirely top surface included both the ridges and the grooves. The evaporated conditions and thickness-monitoring parameters are in following.

Evaporated conditions :

Substrate temperature	200°C
Back pressure	5×10^{-6} torr
Deposition rate	3 - 5 Å/s
Thickness from the evaporator	3,000 Å

Thickness monitoring parameters :

SiO_2 density	2.20 g/cm^3
Z-ratio	1.070

The thickness and refractive index of the SiO_2 film are confirmed by the *laser ellipsometer* which expresses 2,000 Å of thickness and 1.46 of refractive index. While the film is depositing, the temperature within the evaporating chamber is at 200°C,

then the crystal-oscillating which depends on the temperature is far-away from the low-temperature calibrated values. Then the thickness measured from the ellipsometer is more reliable than the crystal-oscillation used in the thickness monitoring module.

5.4 Stripes opening

After SiO_2 insulator is deposited on the entirely sample surface, the stripes of SiO_2 must be removed over the top of the ridges by the photolithography process. The negative photoresist named commercially *OMR-83* is used, which is different from the section 5.2 because it is favorable for the second-time mask alignment. In this negative process, the developer and the rinse solution are *Xylene* and *OMR-Buthyl* used by the consequent conditions.

Spinning	1,000 rpm for 5 second	(first stage)
	7,000 rpm for 60 second	(second stage)
Prebake	90°C for 5 minute	
Exposed time	60 second at lamp power density of 1.1 mW/cm^2	
Develop time	30 second	
Rinse time	30 second	
Post bake	120°C for 5 minute	

The opening stripes of SiO_2 is achieved by chemically selective etching. A HF buffer which contains HF : NH_4F : H_2O = 1 : 6 : 65 is the etchant for SiO_2 in this case and the 12 second of etch time is performed for 2000 Å of SiO_2 film removal. After that, the photoresist covered on the samples is removed by *OMR-502* and the samples must be cleaned up for the consequent step.

5.5 Substrate lapping

During laser diode operation, the high current density is injected into the chips, that brings to the accumulation of heat within them. It is obvious that the reduction of substrate thickness can decrease the heat gathering and also increase the laser efficiency. Mechanical lapping is performed by mounting the samples onto the holder

and lapping the substrate-side with SiC powder to decrease the substrate thickness. It is a fact that less substrate thickness produces less heat gathering within the chips, but it is not practical to process the very thin samples because they are easy to crack while holding. Then the lapping process is terminated when 150 μm thickness of the samples is reached.

In the commercial industry, the laser diode chips are mounted to the heat sinks to help the power dissipation which can decrease the accumulated heat. In SDRL, the lack of mounting equipment is a major cause to skip this process.

Consequently, the sample must be de-mounted from the holder and be cleaned up for the next process.

5.6 Metallization

The metal contact for GaAs sample is performed by the *filament evaporator* which heats the metal sources by a hot tungsten filament injected by the very high current. AuZn (Zn=10%) alloy is used as p-contact evaporated on the ridge while AuGe (Ge=5%) / Ni alloy is used as n-contact evaporated on the substrate side. Before the metals evaporating, the native gallium oxide on the both sides of samples is removed by a HCl : H_2O = 1 : 1 solution for 1 minute. The evaporated conditions are in following.

	Back pressure of chamber	10^{-6} torr
p-contact		
	AuZn thickness	3,000 Å
	AuZn annealing	500°C for 2 minute
n-contact		
	AuGe thickness	2,000 Å
	Ni thickness	500 Å
	AuGe/Ni annealing	480°C for 2 minute

It should be noted that all of the thickness displayed above are measured by the crystal-oscillation technique which is calibrated by the Aluminium (Al) mass, then the

It should be noted that all of the thickness displayed above are measured by the crystal-oscillation technique which is calibrated by the Aluminium (Al) mass, then the exact thickness of these alloys are less than the measured values. And the totally annealing time for AuZn contact is 4 minute including annealing time of AuGe/Ni contact.

After complete the device fabrication, the sample is cleaved to form 500~600 μm long laser chips for the measurement of laser characteristics.

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