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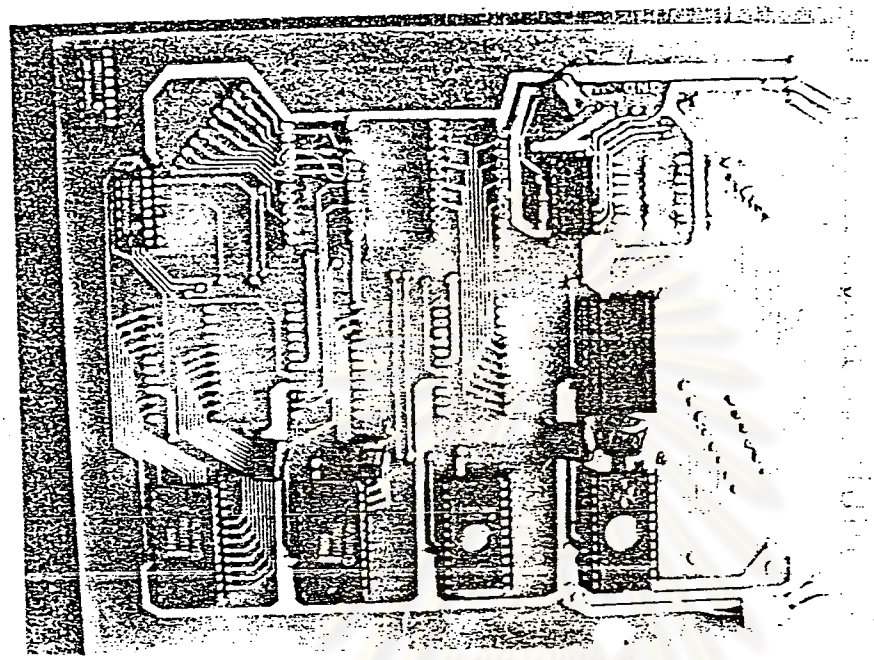
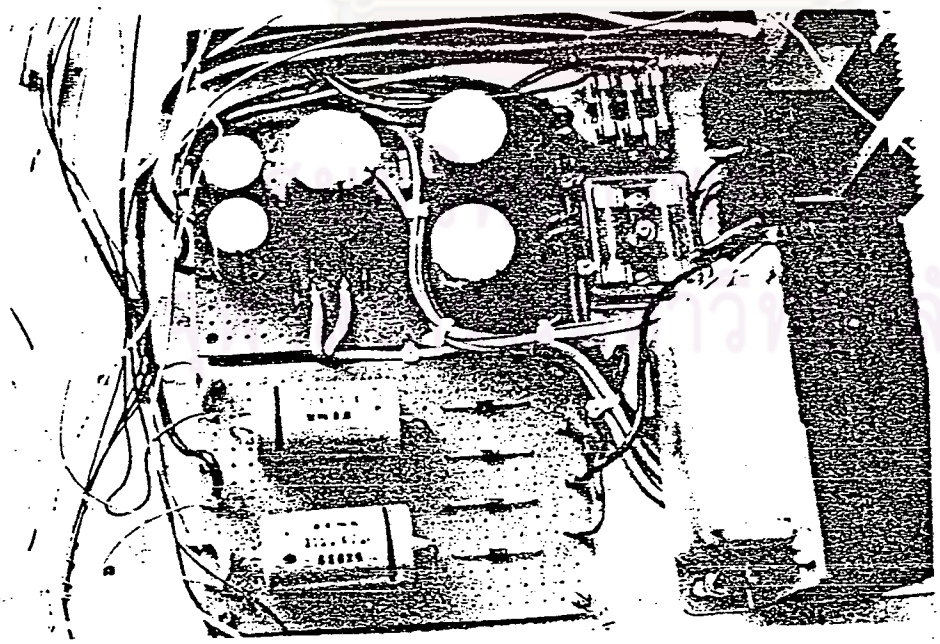
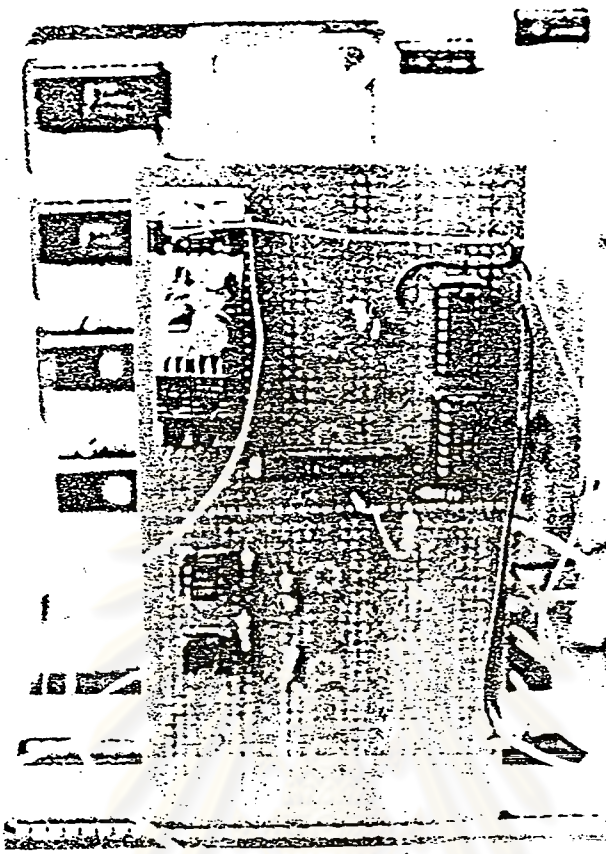
ภาคผนวก ก



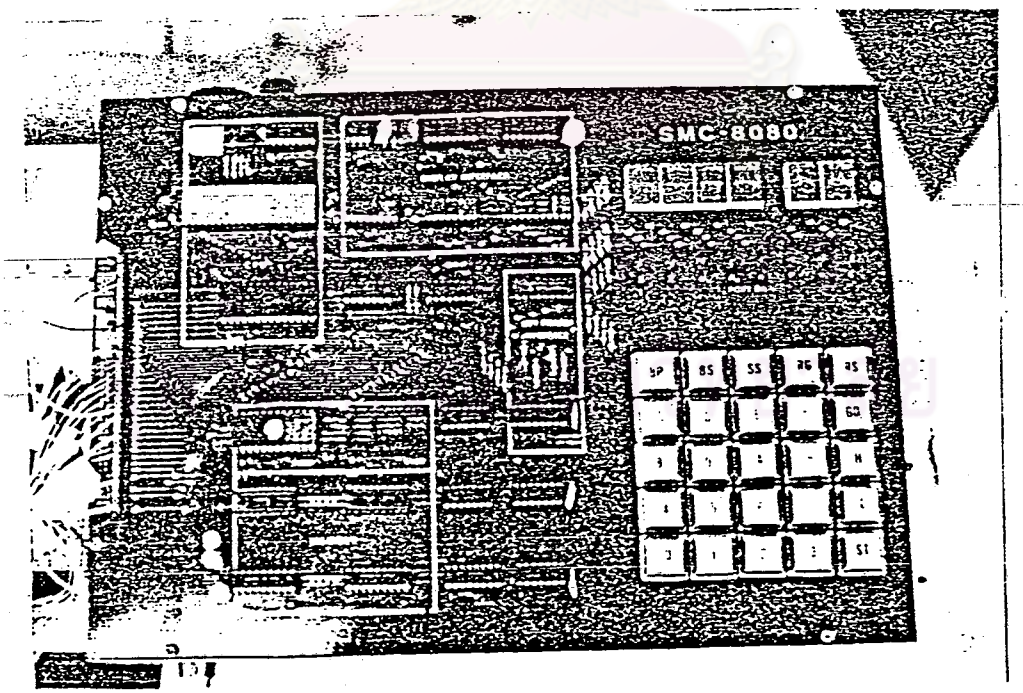
รูปที่ 28 แสดงแผงหน่วยความจำ



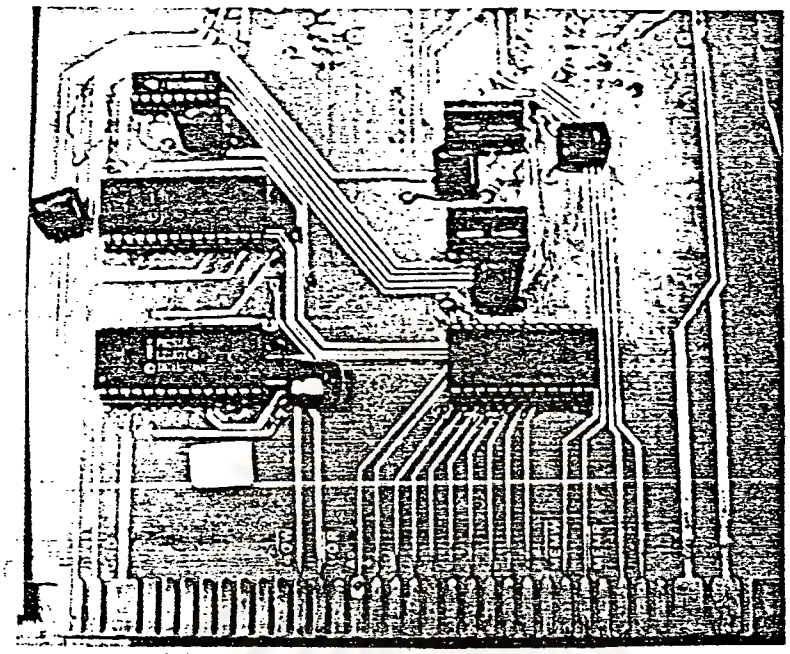
รูปที่ 29 แสดงชุดแหล่งจ่ายกำลังไฟ



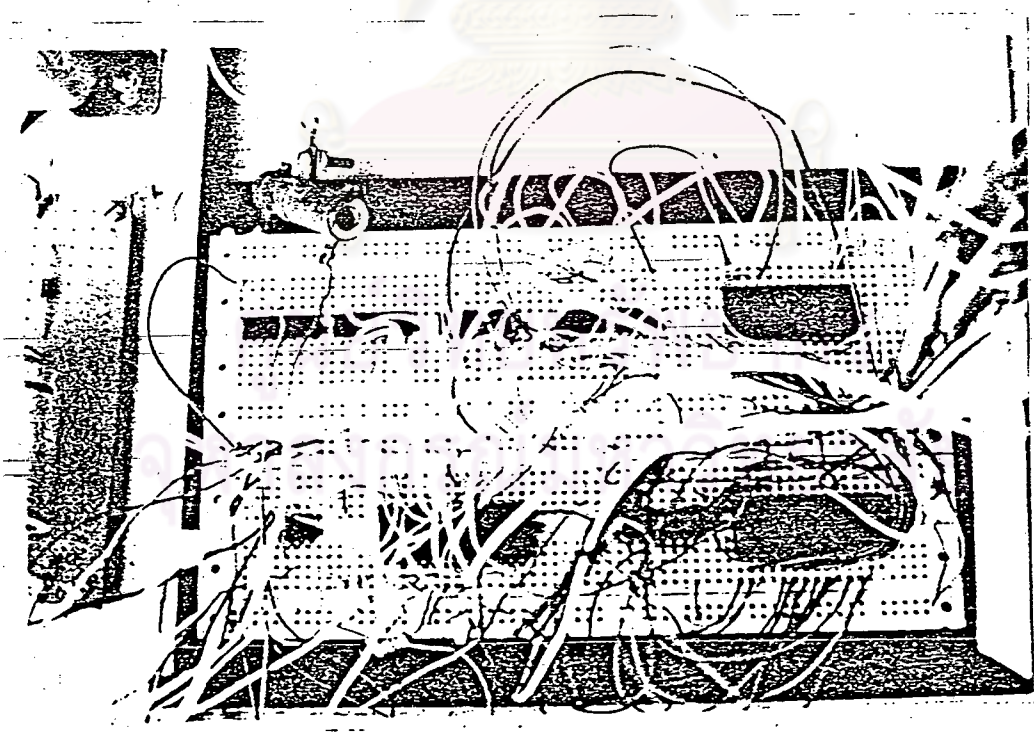
รูปที่ 30 LINE INTERFACE



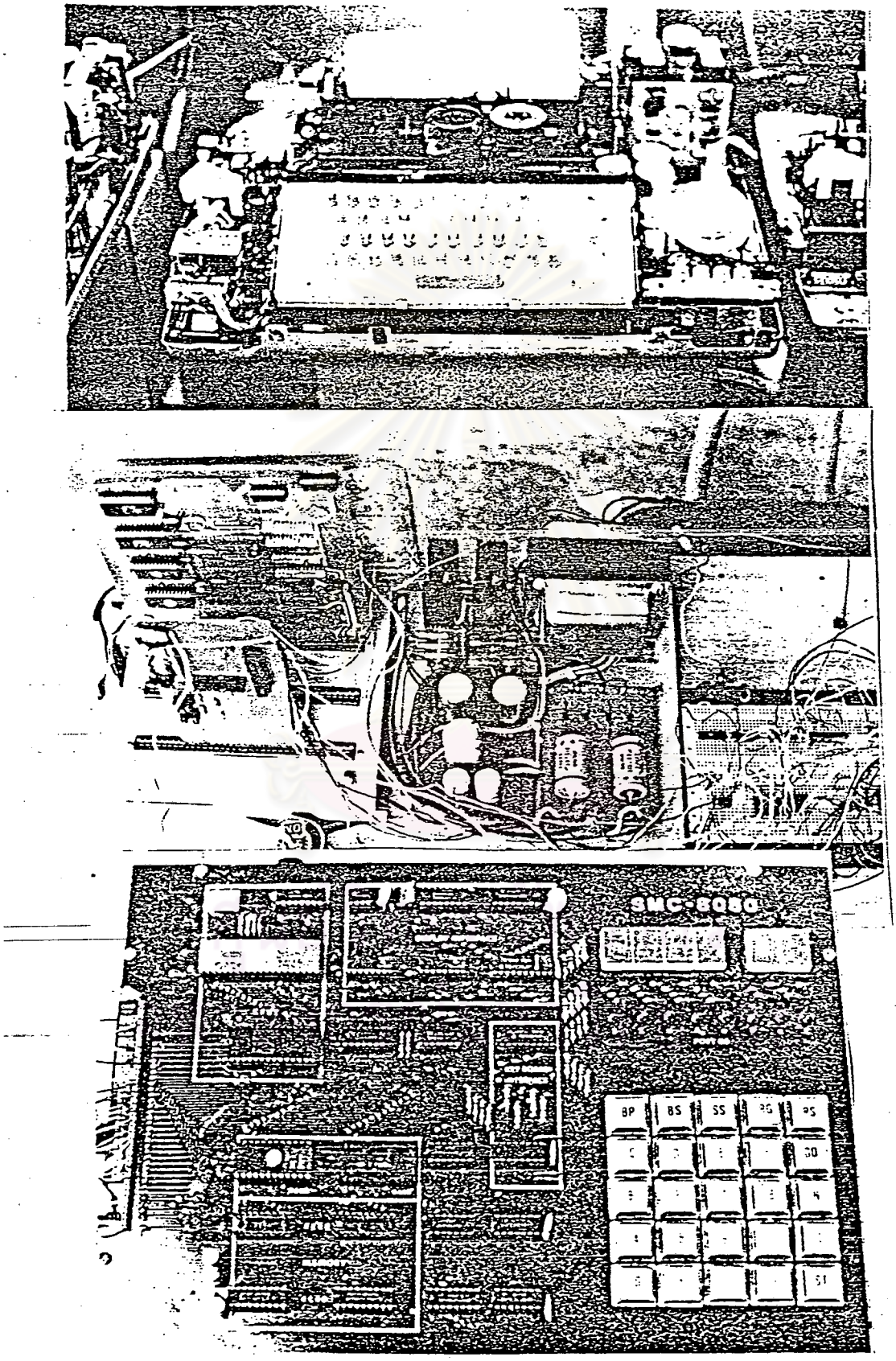
รูปที่ 31 CPU BOARD



รูปที่ 32 แสดงแผงอินเตอร์เฟส



รูปที่ 33 แสดงแผงทดลองอินเตอร์เฟสและไทม์เมอร์



รูปที่ 34 เครื่องเทเล็กซ์ต่อร่วมกับอินเตอร์เฟสและซีพียู

รูปที่ 28 แสดงแผงหน่วยความจำโดยใช้ IC เบอร์ 2716 จำนวน 2 ตัว เพื่อทำหน้าที่เก็บโปรแกรม ซึ่งมีขนาดความจุ 4 K BYTES รวมทั้ง IC เบอร์ 6116 จำนวน 2 ตัว เพื่อให้ทำหน้าที่เก็บข้อความเทเล็กซ์จำนวน 3 KBYTES และใช้สำหรับเป็น WORKING AREA อีก 1 K BYTES แผงหน่วยความจำนี้ได้ออกแบบไว้เพื่อให้สามารถขยายหน่วยความจำเพิ่มเติมได้อีก 8 K BYTES

รูปที่ 29 แสดงส่วนของแหล่งจ่ายกำลังไฟซึ่งจ่ายไฟขนาด ±60V เพื่อส่งให้แก่ชุมสายเทเล็กซ์ฯ

รูปที่ 34 แสดงรูปเครื่องเทเล็กซ์แบบ TELETYPE M-32 โดยต่อใช้งานร่วมกับเครื่องช่วยส่งเทเล็กซ์แบบอัตโนมัติซึ่งประกอบด้วยส่วนอินเตอร์เฟสและซีพียู เพื่อให้ทำงานได้ตามที่มุ่งหวังไว้

ต่อไปจะได้แสดงผลการทำงานของเครื่องเทเล็กซ์เมื่อต่อร่วมกับเครื่องช่วยส่งเทเล็กซ์แบบอัตโนมัติ

```
CMD ? A
? 1+                    ใช้หมายเลขย่อ 1 ซึ่งหมายเลขเต็มคือ
                                        80800

BKK GA
80800++
80816 TLXTEST TH
MAR 07 1400 027285
80800 CTESERV TH

THE QUICK BROWN FOX THAT JUMPS OVER THE LAZY DOG
RYRYRYRYRYRYRYRY
RYRYRYRYRYRYRYRY

MMMMM
1401 000.6

THANK YOU
```

```
CMD ? B
13+
80800+
80809+
+
+
70013+
70033+
+
+
+
?2
?80001+
?3
?80812+
?B
13+
80800+
80001+
80812+
+
70013+
70033+
+
+
+
```

เลขเต็มที่เก็บไว้ 10 หมายเลข

ขอแก้หมายเลขยอ 2 เป็น 80001

ขอแก้หมายเลขยอ 3 เป็น 80812

ขอดูผลที่แก้ไข ซึ่งจะพิมพ์ออกมาทั้ง 10 หมายเลข

```
CMD ?.C
? 70703+5
```

หมายเลขที่จะให้เรียกคือ 70703
ถ้าสายไม่ว่าง จะติดตามผลให้อีก
5 ครั้ง ห่างกันครั้งละ 2 นาที

```
BKK GA
70703++
80816 TLXTEST TH
MAR 07 1359 027182
70703 DOMTLX TH

MMMMM
1359 000.0

THANK YOU
```

```
CMD ? D
MESSAGE IN MEMORY - 1 2 - 4 5 - - - -
MEMORY AREA  7 BLOCKS
MNO P2

TEPAR SOOKPHADOONG
```

ในหน่วยความจำได้เก็บข้อความไว้ 4 ฉบับ คือฉบับที่ 1,2,4 และ 5 มีเนื้อที่ในหน่วยความจำเหลือ 7 ส่วน และผู้ใช้เครื่องฯ ต้องการดูข้อความหมายเลข 2

```
CMD ? D
MESSAGE IN MEMORY - 1 2 - 4 5 - - - -
MEMORY AREA  7 BLOCKS
MNO 3
THE QUICK BROWN FOX THAT JUMPS OVER THE LAZY DOG
RYRYRYRYRYRYRYRY
RYRYRYRYRYRYRYRY
RYRYRYRYRYRYRYRY    MMMMM
```

อธิบายได้เช่นเดียวกับด้านบน ช่วงนี้ผู้ใช้เครื่องฯ ขอเก็บข้อความฉบับหมายเลข 3 และจบข้อความที่เก็บไว้ด้วย MMMMM

```
CMD ? D
MESSAGE IN MEMORY - 1 2 3 4 5 - - - -
MEMORY AREA  6 BLOCKS
MNO 2
MNO 2
RYRYRYRYRYRYRYRYRYRYRYRYRYRY
RYRYRYRYRYRYRYRYRYRYRYRYRYRY
RYRYRYRYRYRYRYRYRYRYRYRYRYRY
MMMMM
```

อธิบายได้เช่นเดียวกับด้านบน ช่วงนี้ผู้ใช้เครื่องฯ ขอเก็บข้อความฉบับหมายเลข 2 ซึ่งมีข้อความเดิมเก็บอยู่แล้ว เครื่องฯจะถามย้ำมาอีก 1 ครั้งเพื่อให้ผู้ใช้เครื่องฯ ยืนยันหมายเลขที่ต้องการ

CMD ? E
NO 1+
MNO 2
T ? 1357

ให้ใช้หมายเลขย่อ 1 เรียกออกซึ่ง
หมายเลขเต็มคือ 80800
ให้เรียกออกเวลา 1357 น. โดยใช้
ข้อความหมายเลข 2 ส่งออกไป

EKK GA
80800++
80816 TLXTEST TH
MAR 07 1357 027072
80800 CTESERV TH

RYRYRYRYRYRYRYRYRY
RYRYRYRYRYRYRYRYRY
RYRYRYRYRYRYRYRYRY
MMMMM
1358.000.3

THANK YOU

ภาคผนวก ข

intel Silicon Gate MOS 8080A

SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

The 8080A is functionally and electrically compatible with the Intel® 8080.

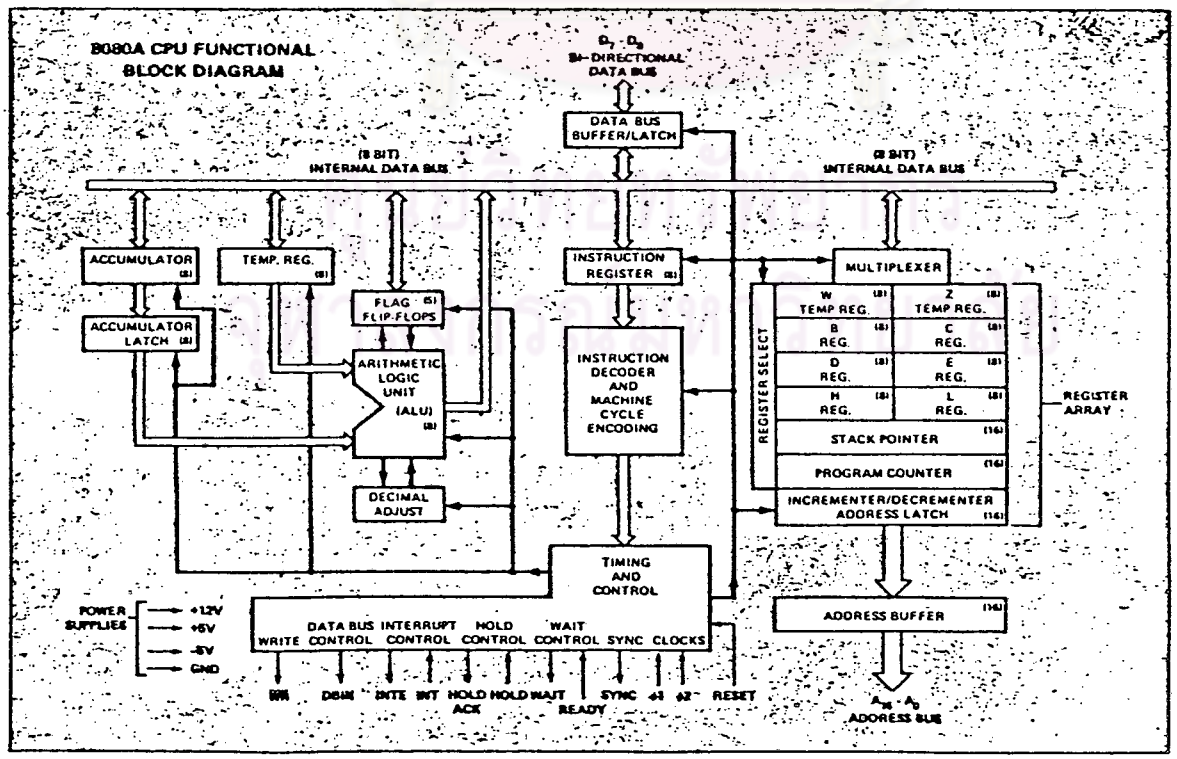
- TTL Drive Capability
- 2 μs Instruction Cycle
- Powerful Problem Solving Instruction Set
- Six General Purpose Registers and an Accumulator
- Sixteen Bit Program Counter for Directly Addressing up to 64K Bytes of Memory
- Sixteen Bit Stack Pointer and Stack Manipulation Instructions for Rapid Switching of the Program Environment
- Decimal, Binary and Double Precision Arithmetic
- Ability to Provide Priority Vectored Interrupts
- 512 Directly Addressed I/O Ports

The Intel® 8080A is a complete 8-bit parallel central processing unit (CPU). It is fabricated on a single LSI chip using Intel's n-channel silicon gate MOS process. This offers the user a high performance solution to control and processing applications.

The 8080A contains six 8-bit general purpose working registers and an accumulator. The six general purpose registers may be addressed individually or in pairs providing both single and double precision operators. Arithmetic and logical instructions set or reset four testable flags. A fifth flag provides decimal arithmetic operation.

The 8080A has an external stack feature wherein any portion of memory may be used as a last in/first out stack to store/retrieve the contents of the accumulator, flags, program counter and all of the six general purpose registers. The sixteen bit stack pointer controls the addressing of this external stack. This stack gives the 8080A the ability to easily handle multiple level priority interrupts by rapidly storing and restoring processor status. It also provides almost unlimited subroutine nesting.

This microprocessor has been designed to simplify systems design. Separate 16-line address and 8-line bi-directional data busses are used to facilitate easy interface to memory and I/O. Signals to control the interface to memory and I/O are provided directly by the 8080A. Ultimate control of the address and data busses resides with the HOLD signal. It provides the ability to suspend processor operation and force the address and data busses into a high impedance state. This permits ORtying these busses with other controlling devices for (DMA) direct memory access or multi-processor operation.



SILICON GATE MOS 8080A

8080A FUNCTIONAL PIN DEFINITION

The following describes the function of all of the 8080A I/O pins. Several of the descriptions refer to internal timing periods.

A_{15}-A_0 (output three-state)
ADDRESS BUS; the address bus provides the address to memory (up to 64K 8-bit words) or denotes the I/O device number for up to 256 input and 256 output devices. A_0 is the least significant address bit.

D_7-D_0 (input/output three-state)
DATA BUS; the data bus provides bi-directional communication between the CPU, memory, and I/O devices for instructions and data transfers. Also, during the first clock cycle of each machine cycle, the 8080A outputs a status word on the data bus that describes the current machine cycle. D_0 is the least significant bit.

SYNC (output)
SYNCHRONIZING SIGNAL; the SYNC pin provides a signal to indicate the beginning of each machine cycle.

DBIN (output)
DATA BUS IN; the DBIN signal indicates to external circuits that the data bus is in the input mode. This signal should be used to enable the gating of data onto the 8080A data bus from memory or I/O.

READY (input)
READY; the READY signal indicates to the 8080A that valid memory or input data is available on the 8080A data bus. This signal is used to synchronize the CPU with slower memory or I/O devices. If after sending an address out the 8080A does not receive a READY input, the 8080A will enter a WAIT state for as long as the READY line is low. READY can also be used to single step the CPU.

WAIT (output)
WAIT; the WAIT signal acknowledges that the CPU is in a WAIT state.

$\overline{WR}$ (output)
WRITE; the $\overline{WR}$ signal is used for memory WRITE or I/O output control. The data on the data bus is stable while the $\overline{WR}$ signal is active low ($\overline{WR}$ = 0).

HOLD (input)
HOLD; the HOLD signal requests the CPU to enter the HOLD state. The HOLD state allows an external device to gain control of the 8080A address and data bus as soon as the 8080A has completed its use of these buses for the current machine cycle. It is recognized under the following conditions:

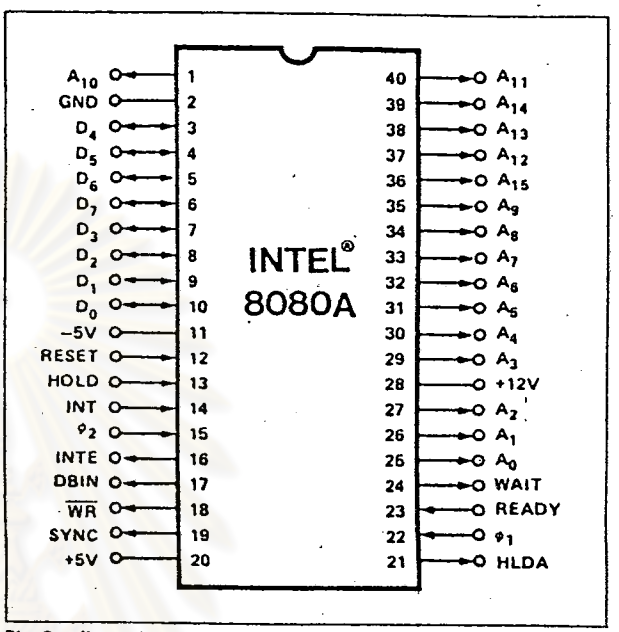
- the CPU is in the HALT state.
- the CPU is in the T2 or TW state and the READY signal is active.

As a result of entering the HOLD state the CPU ADDRESS BUS (A_{15}-A_0) and DATA BUS (D_7-D_0) will be in their high impedance state. The CPU acknowledges its state with the HOLD ACKNOWLEDGE (HLDA) pin.

HLDA (output)
HOLD ACKNOWLEDGE; the HLDA signal appears in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at:

- T3 for READ memory or input.
- The Clock Period following T3 for WRITE memory or OUTPUT operation.

In either case, the HLDA signal appears after the rising edge of ϕ_1 and high impedance occurs after the rising edge of ϕ_2.



Pin Configuration

INTE (output)
INTERRUPT ENABLE; indicates the content of the internal interrupt enable flip/flop. This flip/flop may be set or reset by the Enable and Disable Interrupt instructions and inhibits interrupts from being accepted by the CPU when it is reset. It is automatically reset (disabling further interrupts) at time T1 of the instruction fetch cycle (M1) when an interrupt is accepted and is also reset by the RESET signal.

INT (input)
INTERRUPT REQUEST; the CPU recognizes an interrupt request on this line at the end of the current instruction or while halted. If the CPU is in the HOLD state or if the Interrupt Enable flip/flop is reset it will not honor the request.

RESET (input)[1]
RESET; while the RESET signal is activated, the content of the program counter is cleared. After RESET, the program will start at location 0 in memory. The INTE and HLDA flip/flops are also reset. Note that the flags, accumulator, stack pointer, and registers are not cleared.

V_{SS}	Ground Reference.
V_{DD}	+12 ± 5% Volts.
V_{CC}	+5 ± 5% Volts.
V_{BB}	-5 ±5% Volts (substrate bias).
ϕ_1, ϕ_2	2 externally supplied clock phases. (non TTL compatible)

intel

Schottky Bipolar 8224

CLOCK GENERATOR AND DRIVER FOR 8080A CPU

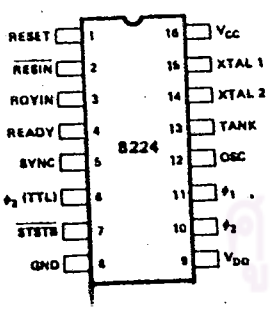
- Single Chip Clock Generator/Driver for 8080A CPU
- Power-Up Reset for CPU
- Ready Synchronizing Flip-Flop
- Advanced Status Strobe
- Oscillator Output for External System Timing
- Crystal Controlled for Stable System Operation
- Reduces System Package Count

The 8224 is a single chip clock generator/driver for the 8080A CPU. It is controlled by a crystal, selected by the designer, to meet a variety of system speed requirements.

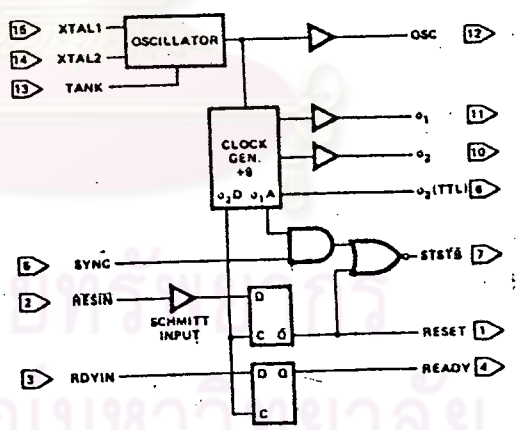
Also included are circuits to provide power-up reset, advance status strobe and synchronization of ready.

The 8224 provides the designer with a significant reduction of packages used to generate clocks and timing for 8080A.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

RESIN	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
STSTB	STATUS STB (ACTIVE LOW)
φ1	8080 CLOCKS
φ2	

XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
φ2 (TTL)	φ2 CLK (TTL LEVEL)
VCC	+5V
VDD	+12V
GND	0V

intel®

Schottky Bipolar 8228

SYSTEM CONTROLLER AND BUS DRIVER FOR 8080A CPU

- Single Chip System Control for MCS-80™ Systems
- Built-In Bi-Directional Bus Driver for Data Bus Isolation
- Allows the use of Multiple Byte Instructions (e.g. CALL) for Interrupt Acknowledge
- User Selected Single Level Interrupt Vector (RST 7)
- 28 Pin Dual In-Line Package
- Reduces System Package Count

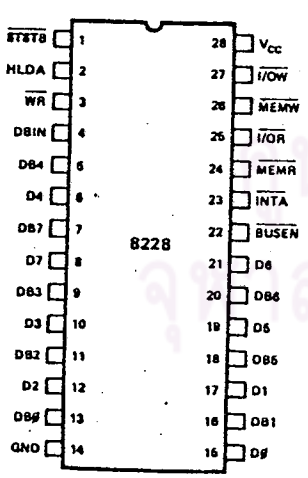
The 8228 is a single chip system controller and bus driver for MCS-80. It generates all signals required to directly interface MCS-80 family RAM, ROM, and I/O components.

A bi-directional bus driver is included to provide high system TTL fan-out. It also provides isolation of the 8080 data bus from memory and I/O. This allows for the optimization of control signals, enabling the systems deisgner to use slower memory and I/O. The isolation of the bus driver also provides for enhanced system noise immunity.

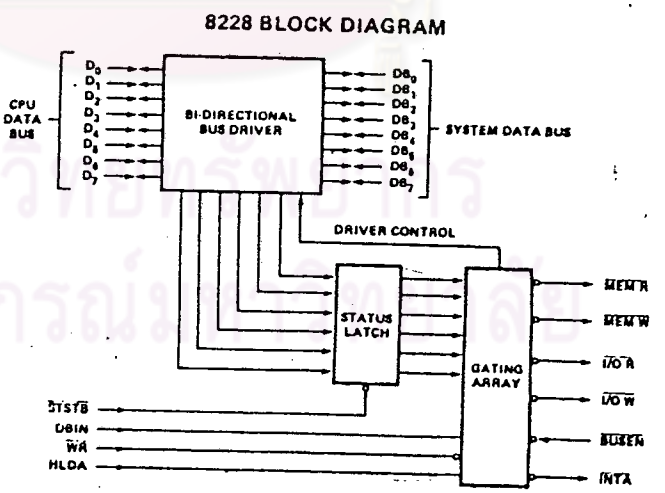
A user selected single level interrupt vector (RST 7) is provided to simplify real time, interrupt driven, small system requirements. The 8228 also generates the correct control signals to allow the use of multiple byte instructions (e.g., CALL) in response to an INTERRUPT ACKNOWLEDGE by the 8080A. This feature permits large, interrupt driven systems to have an unlimited number of interrupt levels.

The 8228 is designed to support a wide variety of system bus structures and also reduce system package count for cost effective, reliable, design of the MCS-80 systems.

PIN CONFIGURATION



8228 BLOCK DIAGRAM



PIN NAMES

D7-D0	DATA BUS (8080 SIDE)	INTA	INTERRUPT ACKNOWLEDGE
DB7-DB0	DATA BUS (SYSTEM SIDE)	HLDA	HLDA (FROM 8080)
I/OR	I/O READ	WR	WR (FROM 8080)
I/OW	I/O WRITE	BUSEN	BUS ENABLE INPUT
MEMR	MEMORY READ	STSTB	STATUS STROBE (FROM 8224)
MEMW	MEMORY WRITE	VCC	+5V
DBIN	DBIN (FROM 8080)	GND	0 VOLTS

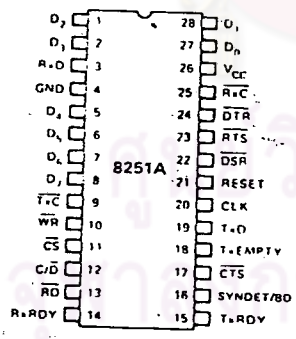
intel®

8251A
PROGRAMMABLE COMMUNICATION INTERFACE

- Synchronous and Asynchronous Operation
  - Synchronous:
    - 5-8 Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
  - Asynchronous:
    - 5-8 Bit Characters
    - Clock Rate — 1, 16 or 64 Times Baud Rate
    - Break Character Generation
    - 1, 1½, or 2 Stop Bits
    - False Start Bit Detection
    - Automatic Break Detect and Handling
- Baud Rate —DC to 64k Baud
- Full Duplex, Double Buffered Transmitter and Receiver
- Error Detection — Parity, Overrun, and Framing
- Fully Compatible with 8080/8085 CPU
- 28-Pin DIP Package
- All Inputs and Outputs Are TTL Compatible
- Single 5 Volt Supply
- Single TTL Clock

The 8251A is the enhanced version of the industry standard, Intel® 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communications with Intel's new high performance family of microprocessors such as the 8085. The 8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM Bi-Sync). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is constructed using N-channel silicon gate technology.

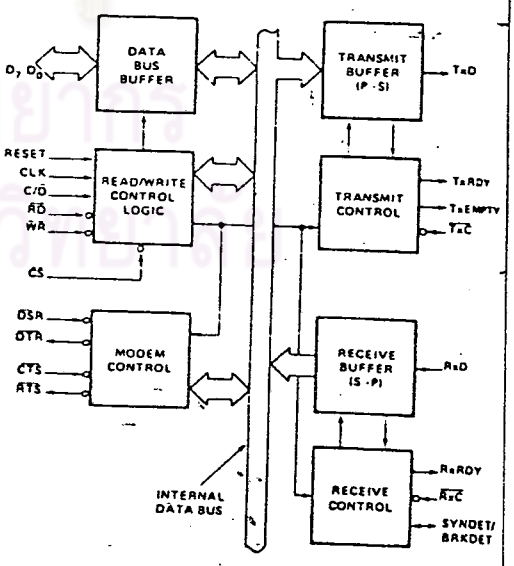
PIN CONFIGURATION



Pin Name	Pin Function
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Select
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock
TxD	Transmitter Data
RxC	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for CPU)
TxRDY	Transmitter Ready (ready for char. from CPU)

Pin Name	Pin Function
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET/BD	Sync Detect/ Break Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxEMPTY	Transmitter Empty
Vcc	+5 Volt Supply
GND	Ground

BLOCK DIAGRAM



PRELIMINARY

8251A BASIC FUNCTIONAL DESCRIPTION

General

The 8251A is a Universal Synchronous/Asynchronous Receiver/Transmitter designed specifically for the 80/85 Microcomputer Systems. Like other I/O devices in a Microcomputer System, its functional configuration is programmed by the system's software for maximum flexibility. The 8251A can support virtually any serial data technique currently in use (including IBM "bi-sync").

In a communication environment an interface device must convert parallel format system data into serial format for transmission and convert incoming serial format data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear "transparent" to the CPU, a simple input or output of byte-oriented system data.

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the 8251A to the system Data Bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions of the CPU. Control words, Command words and Status information are also transferred through the Data Bus Buffer. The command status and data in, and data out are separate 8-bit registers to provide double buffering.

This functional block accepts inputs from the system Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for the device functional definition.

RESET (Reset)

A "high" on this input forces the 8251A into an "Idle" mode. The device will remain at "Idle" until a new set of control words is written into the 8251A to program its functional definition. Minimum RESET pulse width is 6 t_{CY} (clock must be running).

CLK (Clock)

The CLK input is used to generate internal device timing and is normally connected to the Phase 2 (TTL) output of the 8224 Clock Generator. No external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver or Transmitter data bit rates.

$\overline{WR}$ (Write)

A "low" on this input informs the 8251A that the CPU is writing data or control words to the 8251A.

$\overline{RD}$ (Read)

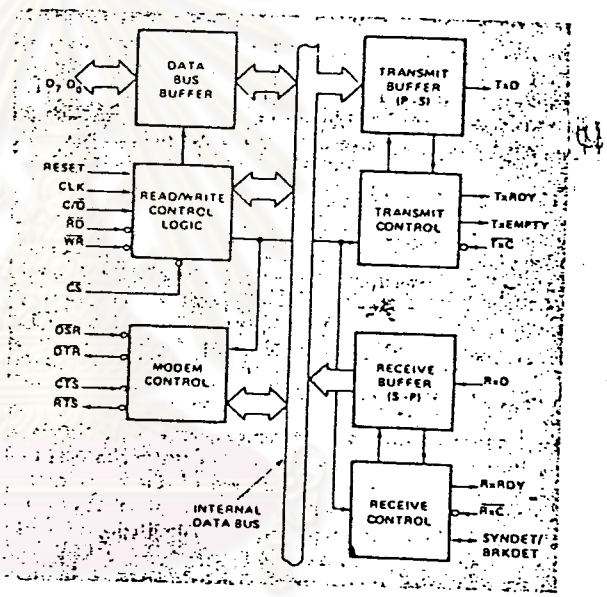
A "low" on this input informs the 8251A that the CPU is reading data or status information from the 8251A.

C/$\overline{D}$ (Control/Data)

This input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the 8251A that the word on the Data Bus is either a data character, control word or status information.
1 = CONTROL/STATUS 0 = DATA

$\overline{CS}$ (Chip Select)

A "low" on this input selects the 8251A. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the Data Bus in the float state and $\overline{RD}$ and $\overline{WR}$ will have no effect on the chip.



C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	8251A DATA → DATA BUS
0	1	0	0	DATA BUS → 8251A DATA
1	0	1	0	STATUS → DATA BUS
1	1	0	0	DATA BUS → CONTROL
X	1	1	0	DATA BUS → 3-STATE
X	X	X	1	DATA BUS → 3-STATE

Modem Control

The 8251A has a set of control inputs and outputs that can be used to simplify the interface to almost any Modem. The Modem control signals are general purpose in nature and can be used for functions other than Modem control, if necessary.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input signal is a general-purpose, 1-bit inverting input port. Its condition can be tested by the CPU using a Status Read operation. The $\overline{DSR}$ input is normally used to test Modem conditions such as Data Set Ready.

$\overline{DTR}$ (Data Terminal Ready)

The $\overline{DTR}$ output signal is a general purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{DTR}$ output signal is normally used for Modem control such as Data Terminal Ready or Rate Select.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output signal is a general purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{RTS}$ output signal is normally used for Modem control such as Request to Send.

$\overline{CTS}$ (Clear to Send)

A "low" on this input enables the 8251A to transmit serial data if the Tx Enable bit in the Command byte is set to a "one." If either a Tx Enable off or CTS off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART, written prior to Tx Disable command before shutting down.

Transmitter Buffer

The Transmitter Buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin on the falling edge of $\overline{TxC}$. The transmitter will begin transmission upon being enabled if $\overline{CTS}$ = 0. The TxD line will be held in the marking state immediately upon a master Reset or when Tx Enable/$\overline{CTS}$ off or TxEMPTY.

Transmitter Control

The transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function.

TxRDY (Transmitter Ready)

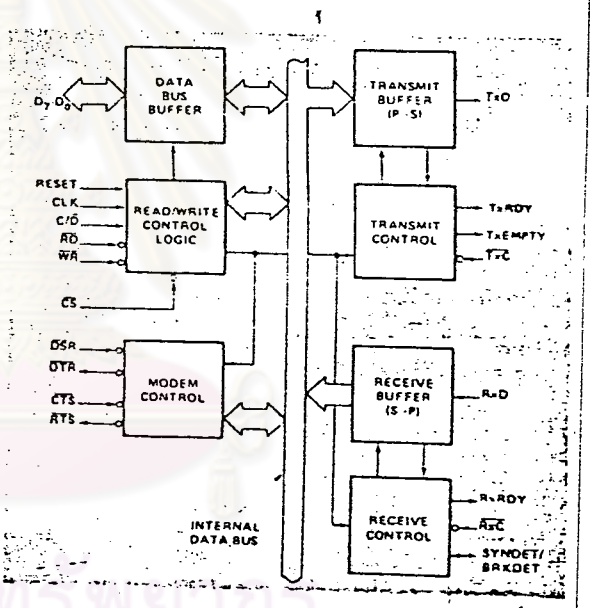
This output signals the CPU that the transmitter is ready to accept a data character. The TxRDY output pin can be used as an interrupt to the system, since it is masked by Tx Disabled, or, for Polled operation, the CPU can check TxRDY using a Status Read operation. TxRDY is automatically reset by the leading edge of $\overline{WR}$ when a data character is loaded from the CPU.

Note that when using the Polled operation, the TxRDY status bit is *not* masked by Tx Enabled, but will only indicate the Empty/Full Status of the Tx Data Input Register.

TxE (Transmitter Empty)

When the 8251A has no characters to transmit, the TxEMPTY output will go "high". It resets automatically upon receiving a character from the CPU. TxEMPTY can be used to indicate the end of a transmission mode, so that the CPU "knows" when to "turn the line around" in the half-duplexed operational mode. TxEMPTY is independent of the Tx Enable bit in the Command instruction.

In SYNChronous mode, a "high" on this output indicates that a character has not been loaded and the SYNC character or characters are about to be or are being transmitted automatically as "fillers". TxEMPTY does not go low when the SYNC characters are being shifted out.



$\overline{TxC}$ (Transmitter Clock)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the Baud Rate (1x) is equal to the $\overline{TxC}$ frequency. In Asynchronous transmission mode the baud rate is a fraction of the actual $\overline{TxC}$ frequency. A portion of the mode instruction selects this factor; it can be 1, 1/16 or 1/64 the $\overline{TxC}$.

For Example:

If Baud Rate equals 110 Baud,
$\overline{TxC}$ equals 110 Hz (1x).
$\overline{TxC}$ equals 1.76 kHz (16x)
$\overline{TxC}$ equals 7.04 kHz (64x).

The falling edge of $\overline{TxC}$ shifts the serial data out of the 8251A.

Receiver Buffer

The Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU. Serial data is input to RxD pin, and is clocked in on the rising edge of $\overline{RxC}$.

Receiver Control

This functional block manages all receiver-related activities which consist of the following features:

The RxD initialization circuit prevents the 8251A from mistaking an unused input line for an active low data line in the "break condition". Before starting to receive serial characters on the RxD line, a valid "1" must first be detected after a chip master Reset. Once this has been determined, a search for a valid low (Start bit) is enabled. This feature is only active in the asynchronous mode, and is only done once for each master Reset.

The False Start bit detection circuit prevents false starts due to a transient noise spike by first detecting the falling edge and then strobing the nominal center of the Start bit (RxD = low).

The Parity Toggle F/F and Parity Error F/F circuits are used for parity error detection and set the corresponding status bit.

The Framing Error Flag F/F is set if the Stop bit is absent at the end of the data byte (asynchronous mode), and also sets the corresponding status bit.

RxRDY (Receiver Ready)

This output indicates that the 8251A contains a character that is ready to be input to the CPU. Rx RDY can be connected to the interrupt structure of the CPU or, for Polled operation, the CPU can check the condition of RxRDY using a Status Read operation.

Rx Enable off both masks and holds RxRDY in the Reset Condition. For Asynchronous mode, to set RxRDY, the Receiver must be Enabled to sense a Start Bit and a complete character must be assembled and transferred to the Data Output Register. For Synchronous mode, to set RxRDY, the Receiver must be enabled and a character must finish assembly and be transferred to the Data Output Register.

Failure to read the received character from the Rx Data Output Register prior to the assembly of the next Rx Data character will set overrun condition error and the previous character will be written over and lost. If the Rx Data is being read by the CPU when the internal transfer is occurring, overrun error will be set and the old character will be lost.

$\overline{RxC}$ (Receiver Clock)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the Baud Rate (1x) is equal to the actual frequency of $\overline{RxC}$. In Asynchronous Mode, the Baud Rate is a fraction of the actual $\overline{RxC}$ frequency. A portion of the mode instruction selects this factor; 1, 1/16 or 1/64 the $\overline{RxC}$.

For Example:

Baud Rate equals 300 Baud, if
$\overline{RxC}$ equals 300 Hz (1x)
$\overline{RxC}$ equals 4800 Hz (16x)
$\overline{RxC}$ equals 19.2 kHz (64x).

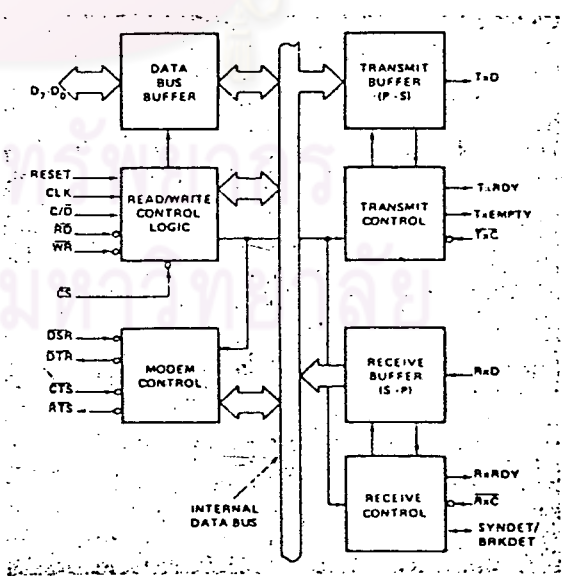
Baud Rate equals 2400 Baud, if
$\overline{RxC}$ equals 2400 Hz (1x)
$\overline{RxC}$ equals 38.4 kHz (16x)
$\overline{RxC}$ equals 153.6 kHz (64x).

Data is sampled into the 8251A on the rising edge of $\overline{RxC}$.

NOTE: In most communications systems, the 8251A will be handling both the transmission and reception operations of a single link. Consequently, the Receive and Transmit Baud Rates will be the same. Both $\overline{TxC}$ and $\overline{RxC}$ will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

SYNDET (SYNC Detect)/BRKDET (Break Detect)

This pin is used in SYNChronous Mode for SYNDET and may be used as either input or output; programmable through the Control Word. It is reset to output mode low upon RESET. When used as an output (internal Sync mode), the SYNDET pin will go "high" to indicate that the 8251A has located the SYNC character in the Receive mode. If the 8251A is programmed to use double Sync characters (bisync), then SYNDET will go "high" in the middle of the last bit of the second Sync character. SYNDET is automatically reset upon a Status Read operation.



Mode Instruction Definition

The 8251A can be used for either Asynchronous or Synchronous data communication. To understand how the Mode Instruction defines the functional operation of the 8251A, the designer can best view the device as two separate components sharing the same package, one Asynchronous the other Synchronous. The format definition can be changed only after a master chip Reset. For explanation purposes the two formats will be isolated.

NOTE: When parity is enabled it is not considered as one of the data bits for the purpose of programming the word length. The actual parity bit received on the Rx Data line cannot be read on the Data Bus. In the case of a programmed character length of less than 8 bits, the least significant Data Bus bits will hold the data; unused bits are "don't care" when writing data to the 8251A, and will be "zeros" when reading the data from the 8251A.

Asynchronous Mode (Transmission)

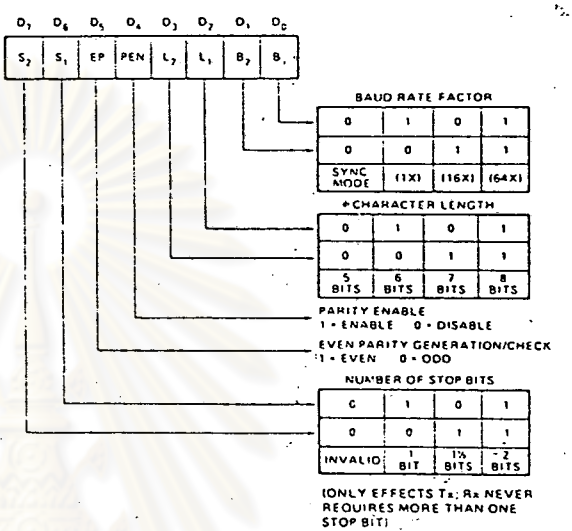
Whenever a data character is sent by the CPU the 8251A automatically adds a Start bit (low level) followed by the data bits (least significant bit first), and the programmed number of Stop bits to each character. Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of $\overline{TxC}$ at a rate equal to 1, 1/16, or 1/64 that of the $\overline{TxC}$, as defined by the Mode Instruction. BREAK characters can be continuously sent to the TxD if commanded to do so.

When no data characters have been loaded into the 8251A the TxD output remains "high" (marking) unless a Break (continuously low) has been programmed.

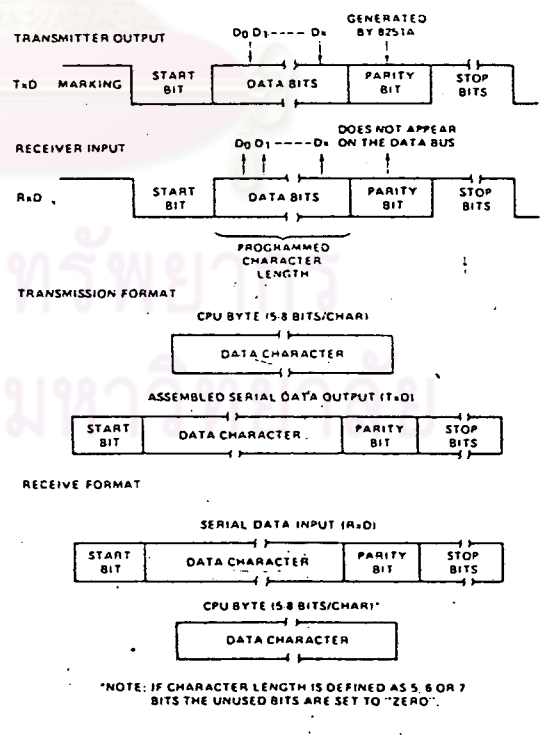
Asynchronous Mode (Receive)

The RxD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center (16X or 64X mode only). If a low is detected again, it is a valid START bit, and the bit counter will start counting. The bit counter thus locates the center of the data bits, the parity bit (if it exists) and the stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of $\overline{RxC}$. If a low level is detected as the STOP bit, the Framing Error flag will be set. The STOP bit signals the end of a character. Note that the *receiver* requires only *one* stop bit, regardless of the number of stop bits programmed. This character is then loaded into the parallel I/O buffer of the 8251A. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the OVERRUN Error flag is raised (thus the previous character is lost). All of the error flags can be reset by an Error Reset Instruction. The occurrence of any of these errors will not affect the operation of the 8251A.

Mode Instruction Format, Asynchronous Mode



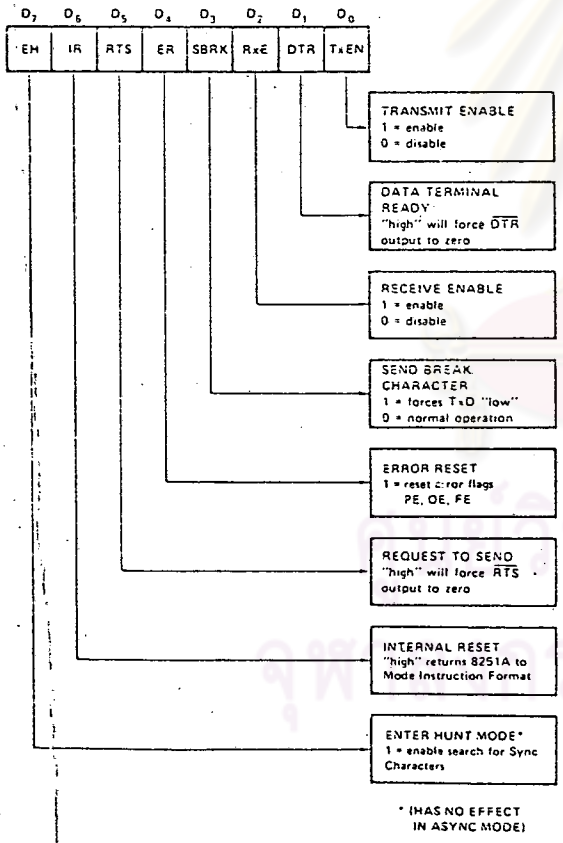
Asynchronous Mode



COMMAND INSTRUCTION DEFINITION

Once the functional definition of the 8251A has been programmed by the Mode Instruction and the Sync Characters are loaded (if in Sync Mode) then the device is ready to be used for data communication. The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset and Modem Controls are provided by the Command Instruction.

Once the Mode Instruction has been written into the 8251A and Sync characters inserted, if necessary, then all further "control writes" ($C/\overline{D}$ = 1) will load a Command Instruction. A Reset Operation (internal or external) will return the 8251A to the Mode Instruction format.



Note: Error Reset must be performed whenever RxEnable and Enter Hunt are programmed.

Command Instruction Format

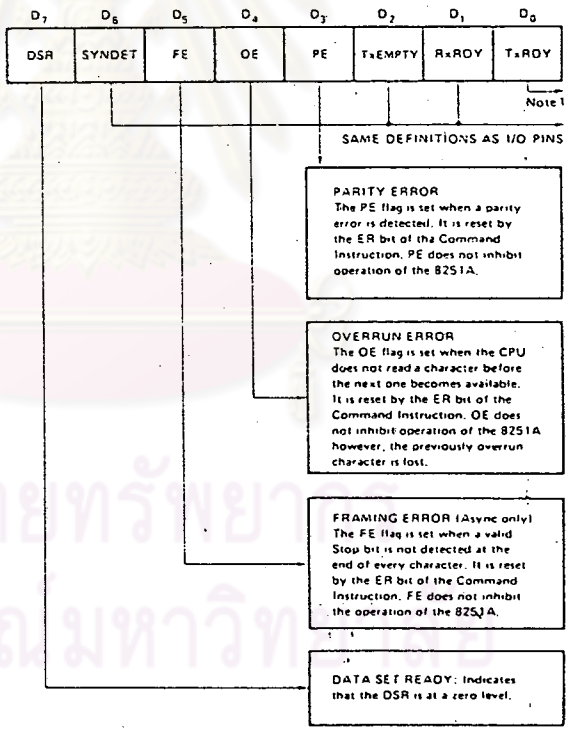
STATUS READ DEFINITION

In data communication systems it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The 8251A has facilities that allow the programmer to "read" the status of the device at any time during the functional operation. (The status update is inhibited during status read).

A normal "read" command is issued by the CPU with $C/\overline{D}$ = 1 to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins so that the 8251A can be used in a completely Polled environment or in an interrupt driven environment. TxRDY is an exception.

Note that status update can have a maximum delay of 28 clock periods from the actual event affecting the status.



Status Read Format

Note 1: TxRDY status bit has different meanings from the TxRDY output pin: The former is not conditioned by $\overline{CTS}$ and TxEN; the latter is conditioned by both $\overline{CTS}$ and TxEN.

i.e. TxRDY status bit = D0 Buffer Empty

TxRDY pin out = D0 Buffer Empty · (CTS=0) · (TxEN=1)

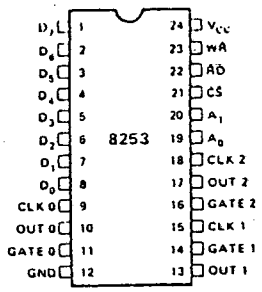
8253, 8253-5
PROGRAMMABLE INTERVAL TIMER

- MCS-85™ Compatible 8253-5
- 3 Independent 16-Bit Counters
- DC to 2 MHz
- Programmable Counter Modes
- Count Binary or BCD
- Single +5V Supply
- 24 Pin Dual-In-Line Package

The 8253 is a programmable counter/timer chip designed for use as an Intel Microcomputer peripheral. It uses nMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as three independent 16-bit counters, each with a count rate of up to 2 MHz. All modes of operation are software programmable.

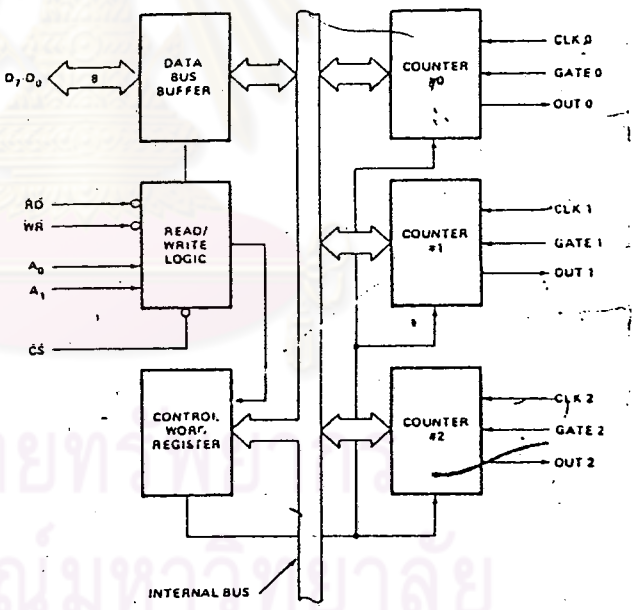
PIN CONFIGURATION



PIN NAMES

D_7-D_0	DATA BUS (8 BIT)
CLK N	COUNTER CLOCK INPUTS
GATE N	COUNTER GATE INPUTS
OUT N	COUNTER OUTPUTS
RD	READ COUNTER
WR	WRITE COMMAND OR DATA
CS	CHIP SELECT
A_0, A_1	COUNTER SELECT
V_{CC}	+5 VOLTS
GND	GROUND

BLOCK DIAGRAM



8253 BASIC FUNCTIONAL DESCRIPTION

General

The 8253 is a programmable interval timer/counter specifically designed for use with the Intel™ Microcomputer systems. Its function is that of a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 8253 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in systems software, the programmer configures the 8253 to match his requirements, initializes one of the counters of the 8253 with the desired quantity, then upon command the 8253 will count out the delay and interrupt the CPU when it has completed its tasks. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained by assignment of priority levels.

Other counter/timer functions that are non-delay in nature but also common to most microcomputers can be implemented with the 8253.

- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8253 to the system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput CPU instructions. The Data Bus Buffer has three basic functions.

1. Programming the MODES of the 8253.
2. Loading the count registers.
3. Reading the count values.

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation. It is enabled or disabled by CS so that no operation can occur to change the function unless the device has been selected by the system logic.

$\overline{RD}$ (Read)

A "low" on this input informs the 8253 that the CPU is inputting data in the form of a counters value.

$\overline{WR}$ (Write)

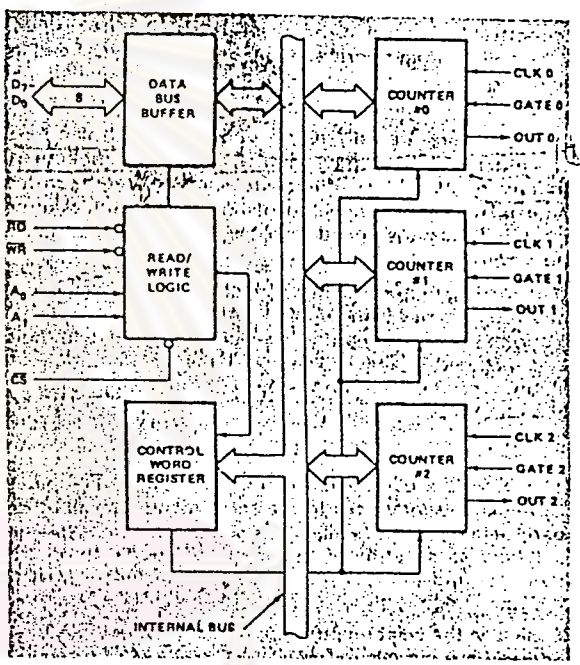
A "low" on this input informs the 8253 that the CPU is outputting data in the form of mode information or loading counters.

A0, A1

These inputs are normally connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for mode selection.

$\overline{CS}$ (Chip Select)

A "low" on this input enables the 8253. No reading or writing will occur unless the device is selected. The $\overline{CS}$ input has no effect upon the actual operation of the counters.



8253 BLOCK DIAGRAM

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation 3-State
1	X	X	X	X	Disable 3-State
0	1	1	X	X	No-Operation 3-State

CONTROL WORD

Control Word Register

The Control Word Register is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational MODE of each counter, selection of binary or BCD counting and the loading of each count register.

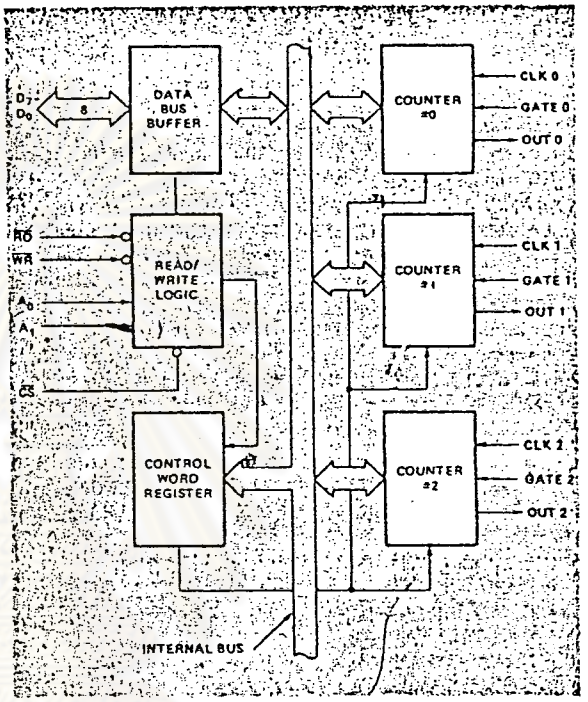
The Control Word Register can only be written into; no read operation of its contents is available.

Counter #0, Counter #1, Counter #2

These three functional blocks are identical in operation so only a single Counter will be described. Each Counter consists of a single, 16-bit, pre-settable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

The counters are fully independent and each can have separate Mode configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications and special commands and logic are included in the 8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

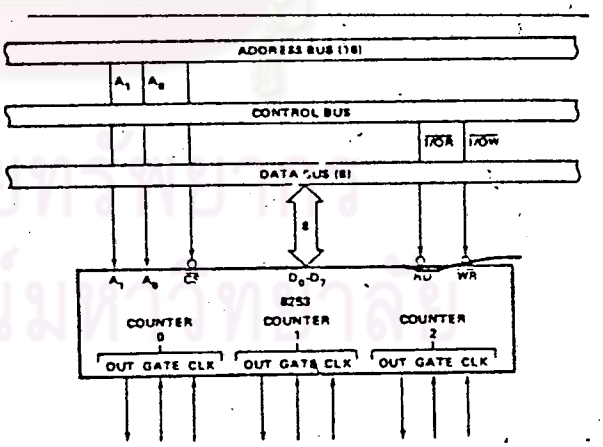


8253 BLOCK DIAGRAM

8253 SYSTEM INTERFACE

The 8253 is a component of the Intel™ Microcomputer Systems and Interfaces in the same manner as all other peripherals of the family. It is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel® 8205 for larger systems.



8253 SYSTEM INTERFACE

8253 DETAILED OPERATIONAL DESCRIPTION

General

The complete functional definition of the 8253 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize each counter of the 8253 with the desired MODE and quantity information. These control words program the MODE, Loading sequence and selection of binary or BCD counting.

Once programmed, the 8253 is ready to perform whatever timing tasks it is assigned to accomplish.

The actual counting operation of each counter is completely independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

Programming the 8253

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the 8253 is individually programmed by writing a control word into the Control Word Register. (A0, A1 = 11)

Control Word Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Definition of Control Fields

SC-Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RL-Read/Load

RL1	RL0	
0	0	Counter Latching operation (see READ/WRITE Procedure Section)
1	0	Read/Load most significant byte only.
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, then most significant byte.

M-MODE

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

MODE Definition

MODE 0: Interrupt on terminal count.
The OUTput will be initially low after the Mode set operation. After the count is loaded into the selected count register, the OUTput will remain low and the counter will count. When terminal count is reached the OUTput will go high and remain high until the selected count register is reloaded with the Mode.

Reloading a counter register during counting results in the following:

(1) Load 1st byte stops the current counting.

(2) Load 2nd byte starts the new count.

The GATE input will enable the counting when high and inhibit counting when low.

MODE 1: Programmable One-Shot.
The OUTput will go low on the count following the rising edge of the GATE input.

The OUTput will go high on the terminal count. If a new count value is loaded while the OUTput is low it will not affect the duration of the One-Shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

MODE 2: Rate Generator

Divide by N counter. The OUTput will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The GATE input, when low, will force the OUTput high. When the GATE input goes high, the counter will start from the initial count. Thus, the GATE input can be used to synchronize the counter.

When this MODE is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

MODE 3: Square Wave Rate Generator.

Similar to MODE 2 except that the OUTput will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count. If the count is odd, the OUTput will be high for (N+1)/2 counts and low for (N-1)/2 counts.

If the counter register is reloaded with a new value during counting, this new value will be reflected immediately after the output transition of the current count.

MODE 4: Software triggered strobe.

After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value. The count will be inhibited while the gate input is low. Reloading the counter register will restart counting beginning with the new number.

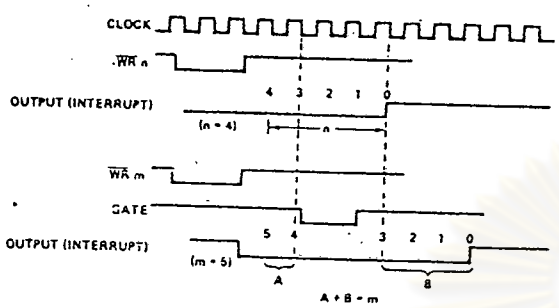
MODE 5: Hardware triggered strobe.

The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

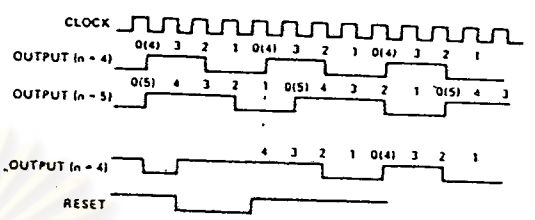
GATE Pin Operations Summary

Modes \ Signal Status	Low Or Going Low	Rising	High
0	Disables counting	——	Enables counting
1	——	1) Initiates counting 2) Resets output after next clock	——
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	——	Enables counting
5	——	Initiates counting	——

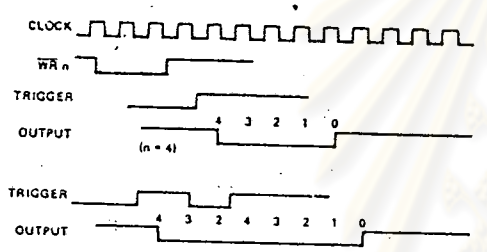
MODE 0



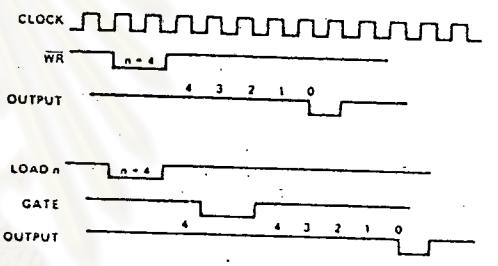
MODE 3



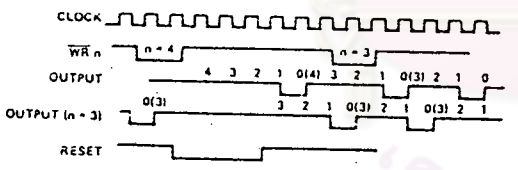
MODE 1



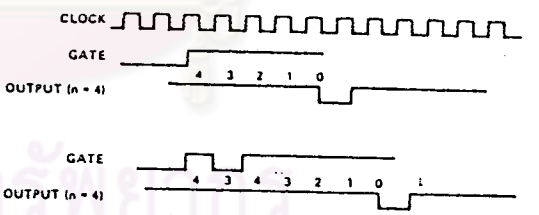
MODE 4



MODE 2



MODE 5



8253 TIMING DIAGRAMS

ภาคผนวก ค

```
2000 3E82       MVI  A,82    ;
2002 D3C0       OUT  C0      ;

2004 3E15       MVI A,15
2006 D3C0       OUT  C0      ;
2008 3E34       MVI  A,34    ;
200A D313       OUT  13      ;
200C 21D007     LXI  H,07D0  ;
200F 7D         MOV  A,L     ;
2010 D310       OUT  10      ;
2012 7C         MOV  A,H     ;
2013 D310       OUT  10      ;
2015 3E70       MVI  A,70    ;
2017 D313       OUT  13      ;
2019 21E803     LXI  H,03E8  ;
201C 7D         MOV  A,L     ;
201D D311       OUT  11      ;
201F 7C         MOV  A,H     ;
2020 D311       OUT  11      ;
2022 3E11       MVI  A,11    ;
2024 321011     STA  1110    ;
2027 322011     STA  1120    ;
202A 323011     STA  1130    ;
202D 324011     STA  1140    ;
2030 325011     STA  1150    ;
2033 326011     STA  1160    ;
2036 327011     STA  1170    ;
```

```
2039 328011      STA  1180   ;
203C [illegible] STA  1190   ;
203F 32A011      STA  11A0   ;
2042 21FF14      LXI  H,14FF ;
2045 3E15        MVI  A,15   ;
2047 77          MOV  M,A    ;
2048 67          MOV  H,A    ;
2049 3C          INR  A      ;
204A FE1F        CPI  1F     ;
204C C24720      JNZ  2047   ;
204F 77          MOV  M,A    ;
2050 67          MOV  H,A    ;
2051 75          MOV  M,L    ;
2052 21B011      LXI  H,11B0 ;
2055 3EFF        MVI  A,FF   ;
2057 77          MOV  M,A    ;
2058 23          INX  H      ;
2059 7D          MOV  A,L    ;
205A FE0A        CPI  0A     ;
205C C25520      JNZ  2055   ;
205F 3E14        MVI  A,14   ;
2061 32BA11      STA  11BA   ;
2064 3E00        MVI  A,00   ;
2066 32D511      STA  11D5   ;
2069 3EFF        MVI  A,FF   ;
206B 32D411      STA  11D4   ;
206E 210012      LXI  H,1200 ;
```

```
2071 3E00       MVI  A,00   ;
2073 47         MOV  B,A    ;
2074 70         MOV  M,B    ;
2075 3C         INR  A      ;
2076 04         INR  B      ;
2077 23         INX  H      ;
2078 FE0A       CPI  0A     ;
207A C27420     JNZ  2074   ;
207D 7D         MOV  A,L    ;
207E C606       ADI  06     ;
2080 6F         MOV  L,A    ;
2081 3E00       MVI  A,00   ;
2083 C37420     JMP  2074   ;
```

EXECUTIVE PROGRAM

```
2086 DB03       IN   03     ;
2088 E602       ANI  02     ;
208A CA9020     JZ   2090   ;
208D CD8E2E     CALL 2E8E   ;   CALL SUBF
2090 DBC0       IN   C0     ;
2092 E602       ANI  02     ;
2094 CAC520     JZ   20C5   ;
2097 CD3423     CALL 2334   ;
209A 0E1F       MVI  C,1F   ;
209C CD2923     CALL 2329   ;
209F 0E0E       MVI  C,0E   ;
```

```
20A1 CD2923     CALL  2329    ;
20A4 0E1C       MVI   C,1C    ;
20A6 CD2923     CALL  2329    ;
20A9 0E09       MVI   C,09    ;
20AB CD2923     CALL  2329    ;
20AE 0E04       MVI   C,04    ;
20B0 CD2923     CALL  2329    ;
20B3 0E1B       MVI   C,1B    ;
20B5 CD2923     CALL  2329    ;
20B8 0E19       MVI   C,19    ;
20BA CD2923     CALL  2329    ;
20BD 0E04       MVI   C,04    ;
20BF CD2923     CALL  2329    ;
20C2 CDDE22     CALL  22DE    ;      CALL SUBCHK
20C5 3AD411     LDA   11D4    ;
20C8 FEFF       CPI   FF      ;
20CA CA8620     JZ    2086    ;
20CD 210010     LXI   H,1000  ;
20D0 47         MOV   B,A     ;
20D1 1600       MVI   D,00    ;
20D3 1E16       MVI   E,16    ;
20D5 05         DCR   B       ;
20D6 19         DAD   D       ;
20D7 78         MOV   A,B     ;
20D8 FE01       CPI   01      ;
20DA C2D520     JNZ   20D5    ;
20DD 3ABD11     LDA   11BD    ;
```

```
20E0 BE        CMP  M      ;
20E1 C28620    JNZ  2086   ;
20E4 23        INX  H      ;
20E5 3ABC11    LDA  11BC   ;
20E8 47        MOV  B,A    ;
20E9 BE        CMP  M      ;
20EA CAF620    JZ   20F6   ;
20ED DA8620    JC   2086   ;
20F0 96        SUB  M      ;
20F1 FE1E      CPI  1E     ;
20F3 D28620    JNC  2086   ;
20F6 2B        DCX  H      ;
20F7 7E        MOV  A,M    ;
20F8 32BF11    STA  11BE   ;
20FB 23        INX  H      ;
20FC 7E        MOV  A,M    ;
20FD 32BE11    STA  11BE   ;
2100 23        INX  H      ;
2101 7E        MOV  A,M    ;
2102 FE00      CPI  00     ;
2104 CA6E21    JZ   216E   ;
2107 32D011    STA  11D0   ;
210A 23        INX  H      ;
210B 7E        MOV  A,M    ;
210C FEFF      CPI  FF     ;
210E CAC521    JZ   21C5   ;
2111 32D111    STA  11D1   ;
```

```
2114 23        INX  H       ;
2115 7D        MOV  A,L     ;
2116 BE        CMP  M       ;
2117 CA2822    JZ   2228    ;
211A 7E        MOV  A,M     ;
211B 32D311    STA  11D3    ;
211E 23        INX  H       ;
211F 7E        MOV  A,M     ;
2120 32D211    STA  11D2    ;
2123 23        INX  H       ;
2124 CD082A    CALL 2A08    ;       CALL SUBEST
2127 78        MOV  A,B     ;
2128 FE00      CPI  00      ;
212A CA8620    JZ   2086    ;
212D CD572D    CALL 2D57    ;       CALL SUBCON
2130 78        MOV  A,B     ;
2131 FEFF      CPI  FF      ;
2133 CA0C22    JZ   220C    ;
2136 21B011    LXI  H,11B0  ;
2139 3AD111    LDA  11D1    ;
213C 85        ADD  L       ;
213D 3D        DCR  A       ;
213E 6F        MOV  L,A     ;
213F 66        MOV  H,M     ;
2140 2E00      MVI  L,00    ;
2142 4E        MOV  C,M     ;
2143 CD2923    CALL 2329    ;
```

```
2146 CD1E23     CALL 231E    ;
2149 23         INX  H       ;
214A FEFF       CPI  FF      ;
214C C24221     JNZ  2142    ;
214F CD2F2F     CALL 2F2F    ;        CALL END
2152 CD8E2E     CALL 2E8E    ;        CALL SUBF
2155 0601       MVI  B,01    ;
2157 210010     LXI  H,1000  ;
215A 1600       MVI  D,00    ;
215C 1E16       MVI  E,16    ;
215E 04         INR  B       ;
215F 19         DAD  D       ;
2160 3AD311     LDA  11D3    ;
2163 BD         CMP  L       ;
2164 C25E21     JNZ  215E    ;
2167 78         MOV  A,B     ;
2168 32D411     STA  11D4    ;
216B C38620     JMP  2086    ;
```



```
216E CD3423     CALL 2334    ;
2171 0E1F       MVI  C,1F    ;
2173 CD2923     CALL 2329    ;
2176 0E0E       MVI  C,0E    ;
2178 CD2923     CALL 2329    ;
217B 0E03       MVI  C,03    ;
```

```
217D CD2923      CALL 2329      ;
2180 0E0C        MVI  C,0C      ;
2182 CD2923      CALL 2329      ;
2185 CD2923      CALL 2329      ;
2188 0E18        MVI  C,18      ;
218A CD2923      CALL 2329      ;
218D 0E10        MVI  C,10      ;
218F CD2923      CALL 2329      ;
2192 0E04        MVI  C,04      ;
2194 CD2923      CALL 2329      ;
2197 0E05        MVI  C,05      ;
2199 CD2923      CALL 2329      ;
219C 0E01        MVI  C,01      ;
219E CD2923      CALL 2329      ;
21A1 0E0C        MVI  C,0C      ;
21A3 CD2923      CALL 2329      ;
21A6 0E09        MVI  C,09      ;
21A8 CD2923      CALL 2329      ;
21AB 0E04        MVI  C,04      ;
21AD CD2923      CALL 2329      ;
21B0 0E1B        MVI  C,1B      ;
21B2 CD2923      CALL 2329      ;
21B5 23          INX  H         ;
21B6 23          INX  H         ;
21B7 23          INX  H         ;
21B8 23          INX  H         ;
21B9 4E          MOV  C,M       ;
```

```
21BA CD2923     CALL 2329    ;
21BD FE11       CPI  11      ;
21BF C2B821     JNZ  21B8    ;
21C2 C38620     JMP  2086    ;



21C5 23         INX  H       ;
21C6 7D         MOV  A,L     ;
21C7 BE         CMP  M       ;
21C8 CAE621     JZ   21E6    ;
21CB 23         INX  H       ;
21CC 7E         MOV  A,M     ;
21CD 32D311     STA  11D3    ;
21D0 23         INX  H       ;
21D1 7E         MOV  A,M     ;
21D2 32D211     STA  11D2    ;
21D5 CD082A     CALL 2A08    ;       CALL SUBEST
21D8 78         MOV  A,B     ;
21D9 FE00       CPI  00      ;
21DB CA8620     JZ   2086    ;
21DE CD572D     CALL 2D57    ;       CALL SUBCON
21E1 78         MOV  A,B     ;
21E2 FEFF       CPI  FF      ;
21E4 CA0C22     JZ   220C    ;
21E7 CD8E2E     CALL 2E8E    ;       CALL SUBF
21EA C35521     JMP  2155    ;
```

```
21ED 23          INX  H        ;
21EE 23          INX  H        ;
21EF CD082A      CALL 2A08     ;        CALL SUBEST
21F2 78          MOV  A,B      ;
21F3 FE00        CPI  00       ;
21F5 CA8620      JZ   2086     ;
21F8 CD572D      CALL 2D57     ;        CALL SUBCON
21FB 78          MOV  A,B      ;
21FC FEFF        CPI  FF       ;
21FE CA0C22      JZ   220C     ;
2201 CD8E2E      CALL 2E8E     ;        CALL SUBF
2204 3EFF        MVI  A,FF     ;
2206 32D411      STA  11D4     ;
2209 C38620      JMP  2086     ;

220C 3AD011      LDA  11D0     ;
220F 3D          DCR  A        ;
2210 32D011      STA  11D0     ;
2213 3ABF11      LDA  11BF     ;
2216 57          MOV  D,A      ;
2217 3ABE11      LDA  11BE     ;
221A 5F          MOV  E,A      ;
221B 13          INX  D        ;
221C 13          INX  D        ;
221D 7A          MOV  A,D      ;
```

```
221E 3ABF11     LDA  11BF    ;
2221 7B         MOV  A,E     ;
2222 3ABE11     LDA  11BE    ;
2225 C38620     JMP  2086    ;



2228 23         INX  H       ;
2229 23         INX  H       ;
222A CD082A     CALL 2A08    ;     CALL SUBEST
222D 78         MOV  A,B     ;
222E FE00       CPI  00      ;
2230 CA8620     JZ   2086    ;
2233 CD572D     CALL 2D57    ;     CALL SUBCON
2236 78         MOV  A,B     ;
2237 FEFF       CPI  FF      ;
2239 CA0C22     JZ   220C    ;
223C 21B011     LXI  H,11B0  ;
223F 3AD111     LDA  11D1    ;
2242 85         ADD  L       ;
2243 3D         DCR  A       ;
2244 6F         MOV  L,A     ;
2245 66         MOV  H,M     ;
2246 2E00       MVI  L,00    ;
2248 4E         MOV  C,M     ;
2249 CD2923     CALL 2329    ;
224C CD1E23     CALL 231E    ;
```

```
224F 23          INX  H       ;
2250 FEFF        CPI  FF      ;
2252 C24822      JNZ  2248    ;
2255 CD2F2F      CALL 2F2F    ;      CALL END
2258 CD8E2E      CALL 2E8E    ;      CALL SUBF
225B 3EFF        MVI  A,FF    ;
225D 32D411      STA  11D4    ;
2260 C38620      JMP  2086    ;
```

PROGRAM SUBS

```
2263 CD3423      CALL 2334    ;
2266 0E1F        MVI  C,1F    ;
2268 CD2923      CALL 2329    ;
226B 0E05        MVI  C,05    ;
226D CD2923      CALL 2329    ;
2270 0E01        MVI  C,01    ;
2272 CD2923      CALL 2329    ;
2275 0E10        MVI  C,10    ;
2277 CD2923      CALL 2329    ;
227A 0E04        MVI  C,04    ;
227C CD2923      CALL 2329    ;
227F 0E10        MVI  C,10    ;
2281 CD2923      CALL 2329    ;
2284 0E06        MVI  C,06    ;
2286 CD2923      CALL 2329    ;
2289 0E1C        MVI  C,1C    ;
```

```
228B CD2923      CALL 2329    ;
228E 0E01        MVI  C,01    ;
2290 CD2923      CALL 2329    ;
2293 CD3F23      CALL 233F    ;
2296 CD0000      CALL 0000    ;
2299 32BD11      STA  11BD    ;
229C CD3F23      CALL 233F    ;
229F CD0000      CALL 0000    ;
22A2 32BC11      STA  11BC    ;
22A5 CD3F23      CALL 233F    ;
22A8 CD0000      CALL 0000    ;
22AB 32BB11      STA  11BB    ;
22AE C9          RET          ;
```

PROROGRAM UPDATE

REAL TIME CLOCK

```
22AF F5          PUSH PSW     ;
22B0 E5          PUSH H       ;
22B1 21E803      LXI  H,03E8  ;
22B4 7D          MOV  A,L     ;
22B5 D311        OUT  11      ;
22B7 7C          MOV  A,H     ;
22B8 D311        OUT  11      ;
22BA 21BB11      LXI  H,11BB  ;
22BD 7E          MOV  A,M     ;
22BE 3C          INR  A       ;
22BF FE3C        CPI  3C      ;
```

```
22C1 C2D922     JNZ  22D9    ;
22C4 AF         XRA  A       ;
22C5 77         MOV  M,A     ;
22C6 23         INX  H       ;
22C7 7E         MOV  A,M     ;
22C8 3C         INR  A       ;
22C9 FE3C       CPI  3C      ;
22CB C2D922     JNZ  22D9    ;
22CE AF         XRA  A       ;
22CF 77         MOV  M,A     ;
22D0 23         INX  H       ;
22D1 7E         MOV  A,M     ;
22D2 3C         INR  A       ;
22D3 FE18       CPI  18      ;
22D5 C2D922     JNZ  22D9    ;
22D8 AF         XRA  A       ;
22D9 77         MOV  M,A     ;
22DA E1         POP  H       ;
22DB F1         POP  PSW     ;
22DC FB         EI           ;
22DD C9         RET          ;
```

PROGRAM SUBCHK

```
22DE CD3F23     CALL 233F    ;
22E1 FE03       CPI  03      ;
22E3 C2EA22     JNZ  22EA    ;
```

```
22E6 CD5323     CALL  2353    ;        CALL SUBA
22E9 C9         RET           ;

22EA FE19       CPI   19      ;
22EC C2F322     JNZ   22F3    ;
22EF CD9223     CALL  2392    ;        CALL SUBB
22F2 C9         RET           ;

22F3 FE0E       CPI   0E      ;
22F5 C2FC22     JNZ   22FC    ;
22F8 CD742A     CALL  2A74    ;        CALL SUBC
22FB C9         RET           ;

22FC FE09       CPI   09      ;
22FE C20523     JNZ   2305    ;
2301 CD1025     CALL  2510    ;        CALL SUBD
2304 C9         RET           ;
```

```
2305 FE01       CPI  01     ;
2307 C20E23     JNZ  230E     ;
230A CD142B     CALL 2B14     ;        CALL SUBE
230D C9         RET           ;

230E FE0D       CPI  0D       ;
2310 C21723     JNZ  2317     ;
2313 CD8E2E     CALL 2E8E     ;        CALL SUBF
2316 C9         RET           ;

2317 FE05       CPI  05       ;
2319 C0         RNZ           ;
231A CD6322     CALL 2263     ;        CALL SUBS
231D C9         RET           ;

                                       TRANSFER DATA TO EXCHANGE
231E DB03       IN   03       ;
2320 E601       ANI  01       ;
2322 CA1E23     JZ   231E     ;
2325 79         MOV  A,C      ;
2326 D301       OUT  01       ;
2328 C9         RET           ;
```

```
2329 DBC0       IN   C0      ;      TRANSFER DATA TO MACHINE
232B E601       ANI  01      ;
232D CA2923     JZ   2329    ;
2330 79         MOV  A,C     ;
2331 D340       OUT  40      ;
2333 C9         RET          ;

2334 0E08       MVI  C,08    ;      GET LINEFEED
2336 CD2923     CALL 2329    ;
2339 0E02       MVI  C,02    ;
233B CD2923     CALL 2329    ;
233E C9         RET          ;

233F DBC0       IN   C0      ;      CHECK FIGURE SHIFT
2341 E602       ANI  02      ;      AND LETTER SHIFT
2343 CA3F23     JZ   233F    ;
2346 DB40       IN   40      ;
2348 FE1B       CPI  1B      ;
234A CA3F23     JZ   233F    ;
234D FE1F       CPI  1F      ;
234F CA3F23     JZ   233F    ;
2352 C9         RET          ;
```

```
2353 CD3423     CALL  2334    ;
2356 ØE1B       MVI   C,1B    ;       PROGRAM SUBA
2358 CD2923     CALL  2329    ;
235B ØE13       MVI   C,13    ;
235D CD2923     CALL  2329    ;
2360 ØEØ4       MVI   C,Ø4    ;
2362 CD2923     CALL  2329    ;
2365 CD3F23     CALL  233F    ;
2368 47         MOV   B,A     ;
2369 DBCØ       IN    CØ      ;
236B E6Ø1       ANI   Ø1      ;
236D CA6923     JZ    2369    ;
237Ø DB4Ø       IN    4Ø      ;
2372 FE11       CPI   11      ;
2374 CØ         RNZ           ;
2375 78         MOV   A,B     ;
2376 CDB329     CALL  29B3    ;       CALL SUBFIN
2379 CD082A     CALL  2A08    ;       CALL SUBEST
237C 78         MOV   A,B     ;
237D FEØØ       CPI   ØØ      ;
237F C8         RZ            ;
2380 FE1A       CPI   1A      ;
2382 CØ         RNZ           ;
2383 79         MOV   A,C     ;
2384 FEØ3       CPI   Ø3      ;
2386 CØ         RNZ           ;
2387 CD572D     CALL  2D57    ;       CALL SUBCON
```

```
238A 78        MOV  A,B     ;
238B FEFF      CPI  FF      ;
238D C8        RZ           ;
238E CD8E2E    CALL 2E8E    ;     CALL SUBF
2391 C9        RET          ;


2392 CD3423    CALL 2334    ;     PROGRAM SUBB
2395 211011    LXI  H,1110  ;
2398 DBC0      IN   C0      ;
239A E601      ANI  01      ;
239C CA9823    JZ   2398    ;
239F 7E        MOV  A,M     ;
23A0 23        INX  H       ;
23A1 D340      OUT  40      ;
23A3 FE11      CPI  11      ;
23A5 C29823    JNZ  2398    ;
23A8 CD3423    CALL 2334    ;
23AB 212011    LXI  H,1120  ;
23AE DBC0      IN   C0      ;
23B0 E601      ANI  01      ;
23B2 CAAE23    JZ   23AE    ;
23B5 7E        MOV  A,M     ;
23B6 23        INX  H       ;
23B7 D340      OUT  40      ;
23B9 FE11      CPI  11      ;
```

```
23BB C2AE23     JNZ   23AE    ;
23BE CD3423     CALL  2334    ;
23C1 213011     LXI   H,1130  ;
23C4 DBC0       IN    C0      ;
23C6 E601       ANI   01      ;
23C8 CAC423     JZ    23C4    ;
23CB 7E         MOV   A,M     ;
23CC 23         INX   H       ;
23CD D340       OUT   40      ;
23CF FE11       CPI   11      ;
23D1 C2C423     JNZ   23C4    ;
23D4 CD3423     CALL  2334    ;
23D7 214011     LXI   H,1140  ;
23DA DBC0       IN    C0      ;
23DC E601       ANI   01      ;
23DE CADA23     JZ    23DA    ;
23E1 7E         MOV   A,M     ;
23E2 23         INX   H       ;
23E3 D340       OUT   40      ;
23E5 FE11       CPI   11      ;
23E7 C2DA23     JNZ   23DA    ;
23EA CD3423     CALL  2334    ;
23ED 215011     LXI   H,1150  ;
23F0 DBC0       IN    C0      ;
23F2 E601       ANI   01      ;
23F4 CAF023     JZ    23F0    ;
23F7 7E         MOV   A,M     ;
```

```
23F8 23          INX  H       ;
23F9 D340        OUT  40      ;
23FB FE11        CPI  11      ;
23FD C2F023      JNZ  23F0    ;
2400 CD3423      CALL 2334    ;
2403 216011      LXI  H,1160  ;
2406 DBC0        IN   C0      ;
2408 E601        ANI  01      ;
240A CA0624      JZ   2406    ;
240D 7E          MOV  A,M     ;
240E 23          INX  H       ;
240F D340        OUT  40      ;
2411 FE11        CPI  11      ;
2413 C20624      JNZ  2406    ;
2416 CD3423      CALL 2334    ;
2419 217011      LXI  H,1170  ;
241C DBC0        IN   C0      ;
241E E601        ANI  01      ;
2420 CA1C24      JZ   241C    ;
2423 7E          MOV  A,M     ;
2424 23          INX  H       ;
2425 D340        OUT  40      ;
2427 FE11        CPI  11      ;
2429 C21C24      JNZ  241C    ;
242C CD3423      CALL 2334    ;
242F 218011      LXI  H,1180  ;
2432 DBC0        IN   C0      ;
```

```
2434 E601       ANI  01     ;
2436 CA3224     JZ   2432   ;
2439 7E         MOV  A,M    ;
243A 23         INX  H      ;
243B D340       OUT  40     ;
243D FE11       CPI  11     ;
243F C23224     JNZ  2432   ;
2442 CD3423     CALL 2334   ;
2445 211901     LXI  H,1190 ;
2448 DBC0       IN   C0     ;
244A E601       ANI  01     ;
244C CA4824     JZ   2448   ;
244F 7E         MOV  A,M    ;
2450 23         INX  H      ;
2451 D340       OUT  40     ;
2453 FE11       CPI  11     ;
2455 C24824     JNZ  2448   ;
2458 CD3423     CALL 2334   ;
245B 21A011     LXI  H,11A0 ;
245E DBC0       IN   C0     ;
2460 E601       ANI  01     ;
2462 CA5E24     JZ   245E   ;
2465 7E         MOV  A,M    ;
2466 23         INX  H      ;
2467 D340       OUT  40     ;
2469 FE11       CPI  11     ;
246B C25E24     JNZ  245E   ;
```

```
246E CD3423      CALL  2334    ;
2471 DBC0        IN    C0      ;
2473 E601        ANI   01      ;
2475 CA7124      JZ    2471    ;
2478 3E19        MVI   A,19    ;
247A D340        OUT   40      ;
247C CD3F23      CALL  233F    ;
247F FE08        CPI   08      ;
2481 C8          RZ            ;
2482 FE19        CPI   19      ;
2484 CA9223      JZ    2392    ;
2487 FE16        CPI   16      ;
2489 C29124      JNZ   2491    ;
                               ;
248B 211011      LXI   H,1110  ;
248E C3EF24      JMP   24EF    ;

2491 FE17        CPI   17      ;
2493 C29C24      JNZ   249C    ;
2496 212011      LXI   H,1120  ;
2499 C3EF24      JMP   24EF    ;
```

```
249C FE13       CPI  13       ;
249E C2 A724    JNZ  24A7     ;
24A1 213011     LXI  H,1130   ;
24A4 C3 EF24    JMP  24EF     ;


24A7 FE01       CPI  01       ;
24A9 C2 B224    JNZ  24B2     ;
24AC 214011     LXI  H,1140   ;
24AF C3 EF24    JMP  24EF     ;


24B2 FE0A       CPI  0A       ;
24B4 C2 BD24    JNZ  24BD     ;
24B7 215011     LXI  H,1150   ;
24BA C3 EF24    JMP  24EF     ;


24BD FE10       CPI  10       ;
24BF C2 C824    JNZ  24C8     ;
24C2 216011     LXI  H,1160   ;
24C5 C3 EF24    JMP  24EF     ;
```

```
24C8 FE15       CPI  15      ;
24CA C2D324     JNZ  24D3      ;
24CD 217011     LXI  H,1170 ;
24D0 C3EF24     JMP  24EF      ;



24D3 FE07       CPI  07      ;
24D5 C2DE24     JNZ  24DE      ;
24D8 218011     LXI  H,1180 ;
24DB C3EF24     JMP  24EF      ;



24DE FE06       CPI  06      ;
24E0 C2E924     JNZ  24E9      ;
24E3 219011     LXI  H,1190 ;
24E6 C3EF24     JMP  24EF      ;



24E9 FE18       CPI  18      ;
24EB C0         RNZ            ;
24EC 21A011     LXI  H,11A0 ;
24EF CD3423     CALL 2334      ;
24F2 DBC0       IN   C0        ;
24F4 E601       ANI  01        ;
```

```
24F6 CA F224      JZ   24F2     ;
24F9 3E19         MVI  A,19     ;
24FB D340         OUT  40       ;
24FD DBC0         IN   C0       ;
24FF E602         ANI  02       ;
2501 CA FD24      JZ   24FD     ;
2504 DB40         IN   40       ;
2506 23           INX  H        ;
2507 FE11         CPI  11       ;
2509 C2 FD24      JNZ  24FD     ;
250C CD 3423      CALL 2334     ;
250F C3 F224      JMP  24F2     ;
2510 CD3423       CALL 2334     ;       PROGRAM SUBD
2513 0E1F         MVI  C,1F     ;
2515 CD2923       CALL 2329     ;
2518 0E1C         MVI  C,1C     ;
251A 29           DAD  H        ;
251B 23           INX  H        ;
251C 0E01         MVI  C,01     ;
251E CD2923       CALL 2329     ;
2521 0E05         MVI  C,05     ;
2523 CD2923       CALL 2329     ;
2526 CD2923       CALL 2329     ;
2529 0E03         MVI  C,03     ;
252B CD2923       CALL 2329     ;
252E 0E1A         MVI  C,1A     ;
2530 CD2923       CALL 2329     ;
```

```
2533 ØEØ1       MVI  C,Ø1     ;
2535 CD2923     CALL 2329     ;
2538 ØEØ4       MVI  C,Ø4     ;
253A CD2923     CALL 2329     ;
253D ØEØ6       MVI  C,Ø6     ;
253F CD2923     CALL 2329     ;
2542 ØEØC       MVI  C,ØC     ;
2544 CD2923     CALL 2329     ;
2547 ØEØ4       MVI  C,Ø4     ;
2549 CD2923     CALL 2329     ;
254C ØE1C       MVI  C,1C     ;
254E CD2923     CALL 2329     ;
2551 ØEØ1       MVI  C,Ø1     ;
2553 CD2923     CALL 2329     ;
2556 ØE1C       MVI  C,1C     ;
2558 CD2923     CALL 2329     ;
255B ØE18       MVI  C,18     ;
255D CD2923     CALL 2329     ;
2560 ØEØA       MVI  C,ØA     ;
2562 CD2923     CALL 2329     ;
2565 ØE15       MVI  C,15     ;
2567 CD2923     CALL 2329     ;
256A ØEØ4       MVI  C,Ø4     ;
256C CD2923     CALL 2329     ;
256F CD2923     CALL 2329     ;
2572 ØE1B       MVI  C,1B     ;
2574 CD2923     CALL 2329     ;
```

```
2577 Ø60C       MVI  B,ØC    ;
2579 21BØ11     LXI  H,11BØ  ;
257C 7E         MOV  A,M     ;
257D FEFF       CPI  FF      ;
257F C22826     JNZ  2628    ;
2582 ØE03       MVI  C,Ø3    ;
2584 CD2923     CALL 2329    ;
2587 ØE04       MVI  C,Ø4    ;
2589 CD2923     CALL 2329    ;
258C 23         INX  H       ;
258D 7E         MOV  A,M     ;
258E FEFF       CPI  FF      ;
2590 C24726     JNZ  2647    ;
2593 ØE03       MVI  C,Ø3    ;
2595 CD2923     CALL 2329    ;
2598 ØE04       MVI  C,Ø4    ;
259A CD2923     CALL 2329    ;
259D 23         INX  H       ;
259E 7E         MOV  A,M     ;
259F FEFF       CPI  FF      ;
25A1 C26626     JNZ  2666    ;
25A4 ØE03       MVI  C,Ø3    ;
25A6 CD2923     CALL 2329    ;
25A9 ØE04       MVI  C,Ø4    ;
25AB CD2923     CALL 2329    ;
25AE 23         INX  H       ;
25AF 7E         MOV  A,M     ;
```

```
25B0 FEFF       CPI  FF     ;
25B2 C28526     JNZ  2685   ;
25B5 0E03       MVI  C,03   ;
25B7 CD2923     CALL 2329   ;
25BA 0E04       MVI  C,04   ;
25BC CD2923     CALL 2329   ;
25BF 23         INX  H      ;
25C0 7E         MOV  A,M    ;
25C1 FEFF       CPI  FF     ;
25C3 C2A426     JNZ  26A4   ;
25C6 0E03       MVI  C,03   ;
25C8 CD2923     CALL 2329   ;
25CB 0E04       MVI  C,04   ;
25CD CD2923     CALL 2329   ;
25D0 23         INX  H      ;
25D1 7E         MOV  A,M    ;
25D2 FEFF       CPI  FF     ;
25D4 C2C326     JNZ  26C3   ;
25D7 0E03       MVI  C,03   ;
25D9 CD2923     CALL 2329   ;
25DC 0E04       MVI  C,04   ;
25DE CD2923     CALL 2329   ;
25E1 23         INX  H      ;
25E2 7E         MOV  A,M    ;
25E3 FEFF       CPI  FF     ;
25E5 C2E226     JNZ  26E2   ;
25E8 0E03       MVI  C,03   ;
```

```
25EA CD2923      CALL 2329     ;
25ED ØE04        MVI  C,Ø4     ;
25EF CD2923      CALL 2329     ;
25F2 23          INX  H        ;
25F3 7E          MOV  A,M      ;
25F4 FEFF        CPI  FF       ;
25F6 C20127      JNZ  2701     ;
25F9 ØE03        MVI  C,Ø3     ;
25FB CD2923      CALL 2329     ;
25FE ØE04        MVI  C,Ø4     ;
2600 CD2923      CALL 2329     ;
2603 23          INX  H        ;
2604 7E          MOV  A,M      ;
2605 FEFF        CPI  FF       ;
2607 C22027      JNZ  2720     ;
260A ØE03        MVI  C,Ø3     ;
260C CD2923      CALL 2329     ;
260F ØE04        MVI  C,Ø4     ;
2611 CD2923      CALL 2329     ;
2614 23          INX  H        ;
2615 7E          MOV  A,M      ;
2616 FEFF        CPI  FF       ;
2618 C23F27      JNZ  273F     ;
261B ØE03        MVI  C,Ø3     ;
261D CD2923      CALL 2329     ;
2620 ØE04        MVI  C,Ø4     ;
2622 CD2923      CALL 2329     ;
2625 C30000      JMP  0000     ;
```

```
2628 ØE16       MVI  C,16    ;
262A CD2923     CALL 2329    ;
262D ØEØ4       MVI  C,Ø4    ;
262F CD2923     CALL 2329    ;
2632 7E         MOV  A,M     ;
2633 EB         XCHG         ;
2634 67         MOV  H,A     ;
2635 2EFF       MVI  L,FF    ;
2637 BE         CMP  M       ;
2638 CA4226     JZ   2642    ;
263B Ø5         DCR  B       ;
263C 7E         MOV  A,M     ;
263D 67         MOV  H,A     ;
263E BE         CMP  M       ;
263F C23B26     JNZ  263B    ;
2642 Ø5         DCR  B       ;
2643 EB         XCHG         ;
2644 C38C25     JMP  258C    ;

2647 ØE17       MVI  C,17    ;
2649 CD2923     CALL 2329    ;
264C ØEØ4       MVI  C,Ø4    ;
264E CD2923     CALL 2329    ;
2651 7E         MOV  A,M     ;
2652 EB         XCHG         ;
```

```
2653 67        MOV  H,A    ;
2654 2EFF      MVI  L,FF   ;
2656 BE        CMP  M      ;
2657 CA6126    JZ   2661   ;
265A Ø5        DCR  B      ;
265B 7E        MOV  A,M    ;
265C 67        MOV  H,A    ;
265D BE        CMP  M      ;
265E C25726    JNZ  2657   ;
2661 Ø5        DCR  B      ;
2662 EB        XCHG       ;
2663 C39025    JMP  2590   ;



2666 ØE13      MVI  C,13   ;
2668 CD2923    CALL 2329   ;
266B ØEØ4      MVI  C,Ø4   ;
266D CD2923    CALL 2329   ;
2670 7E        MOV  A,M    ;
2671 EB        XCHG       ;
2672 67        MOV  H,A    ;
2673 2EFF      MVI  L,FF   ;
2675 BE        CMP  M      ;
2676 CA8026    JZ   2680   ;
2679 Ø5        DCR  B      ;
267A 7E        MOV  A,M    ;
```

```
267B 67          MOV  H,A    ;
267C BE          CMP  M      ;
267D C2 7926     JNZ  2679   ;
2680 05          DCR  B      ;
2681 EB          XCHG         ;
2682 C3 AE25     JMP  25AE   ;



2685 0E01        MVI  C,01   ;
2687 CD2923      CALL 2329   ;
268A 0E04        MVI  C,04   ;
268C CD2923      CALL 2329   ;
268F 7E          MOV  A,M    ;
2690 EB          XCHG         ;
2691 67          MOV  H,A    ;
2692 2EFF        MVI  L,FF   ;
2694 BE          CMP  M      ;
2695 CA 9F26     JZ   269F   ;
2698 05          DCR  B      ;
2699 7E          MOV  A,M    ;
269A 67          MOV  H,A    ;
269B BE          CMP  M      ;
269C C2 9826     JNZ  2698   ;
269F 05          DCR  B      ;
26A0 EB          XCHG         ;
26A1 C3 BF25     JMP  25BF   ;
```

```
26A4 ØEØA       MVI  C,ØA   ;
26A6 CD2923     CALL 2329   ;
26A9 ØE04       MVI  C,Ø4   ;
26AB CD2923     CALL 2329   ;
26AE 7E         MOV  A,M    ;
26AF EB         XCHG        ;
26BØ 67         MOV  H,A    ;
26B1 2EFF       MVI  L,FF   ;
26B3 BE         CMP  M      ;
26B4 CABE26     JZ   26BE   ;
26B7 Ø5         DCR  B      ;
26B8 7E         MOV  A,M    ;
26B9 67         MOV  H,A    ;
26BA BE         CMP  M      ;
26BB C2B726     JNZ  26B7   ;
26BE Ø5         DCR  B      ;
26BF EB         XCHG        ;
26CØ C3DO25     JMP  25DO   ;
```


```
26C3 ØE1Ø       MVI  C,1Ø   ;
26C5 CD2923     CALL 2329   ;
26C8 ØE04       MVI  C,Ø4   ;
26CA CD2923     CALL 2329   ;
26CD 7E         MOV  A,M    ;
26CE EB         XCHG        ;
```

```
26CF 67        MOV  H,A    ;
26DØ 2EFF      MVI  L,FF   ;
26D2 BE        CMP  M      ;
26D3 CADD26    JZ   26DD   ;
26D6 Ø5        DCR  B      ;
26D7 7E        MOV  A,M    ;
26D8 67        MOV  H,A    ;
26D9 BE        CMP  M      ;
26DA C2D626    JNZ  26D6   ;
26DD Ø5        DCR  B      ;
26DE EB        XCHG        ;
26DF C3E125    JMP  25E1   ;


26E2 ØE15      MVI  C,15   ;
26E4 CD2923    CALL 2329   ;
26E7 ØEØ4      MVI  C,Ø4   ;
26E9 CD2923    CALL 2329   ;
26EC 7E        MOV  A,M    ;
26ED EB        XCHG        ;
26EE 67        MOV  H,A    ;
26EF 2EFF      MVI  L,FF   ;
26F1 BE        CMP  M      ;
26F2 CAFC26    JZ   26FC   ;
26F5 Ø5        DCR  B      ;
26F6 7E        MOV  A,M    ;
```

```
26F7 67        MOV  H,A    ;
26F8 BE        CMP  M      ;
26F9 C2F526    JNZ  26F5   ;
26FC 05        DCR  B      ;
26FD EB        XCHG        ;
26FE C3F225    JMP  25F2   ;
```

```
2701 0E07      MVI  C,07   ;
2703 CD2923    CALL 2329   ;
2706 0E04      MVI  C,04   ;
2708 CD2923    CALL 2329   ;
270B 7E        MOV  A,M    ;
270C EB        XCHG        ;
270D 67        MOV  H,A    ;
270E 2EFF      MVI  L,FF   ;
2710 BE        CMP  M      ;
2711 CA1B27    JZ   271B   ;
2714 05        DCR  B      ;
2715 7E        MOV  A,M    ;
2716 67        MOV  H,A    ;
2717 BE        CMP  M      ;
2718 C21427    JNZ  2714   ;
271B 05        DCR  B      ;
271C EB        XCHG        ;
271D C30326    JMP  2603   ;
```

```
2720 0E06       MVI  C,06    ;
2722 CD2923     CALL 2329    ;
2725 0E04       MVI  C,04    ;
2727 CD2923     CALL 2329    ;
272A 7E         MOV  A,M     ;
272B EB         XCHG         ;
272C 67         MOV  H,A     ;
272D 2EFF       MVI  L,FF    ;
272F BE         CMP  M       ;
2730 CA3A27     JZ   273A    ;
2733 05         DCR  B       ;
2734 7E         MOV  A,M     ;
2735 67         MOV  H,A     ;
2736 BE         CMP  M       ;
2737 C23327     JNZ  2733    ;
273A 05         DCR  B       ;
273B EB         XCHG         ;
273C C31426     JMP  2614    ;
```



```
273F 0E18       MVI  C,18    ;
2741 CD2923     CALL 2329    ;
2744 0E04       MVI  C,04    ;
2746 CD2923     CALL 2329    ;
2749 7E         MOV  A,M     ;
274A EB         XCHG         ;
```

```
274B 67        MOV  H,A    ;
274C 2EFF      MVI  L,FF   ;
274E BE        CMP  M      ;
274F CA5927    JZ   2759   ;
2752 Ø5        DCR  B      ;
2753 7E        MOV  A,M    ;
2754 67        MOV  H,A    ;
2755 BE        CMP  M      ;
2756 C2 5227   JNZ  2752   ;
2759 Ø5        DCR  B      ;
275A EB        XCHG        ;
275B CD3423    CALL 2334   ;
275E ØE1F      MVI  C,1F   ;
2760 CD2923    CALL 2329   ;
2763 ØE1C      MVI  C,1C   ;
2765 CD2923    CALL 2329   ;
2768 ØEØ1      MVI  C,Ø1   ;
276A CD2923    CALL 2329   ;
276D ØE1C      MVI  C,1C   ;
276F CD2923    CALL 2329   ;
2772 ØE18      MVI  C,18   ;
2774 CD2923    CALL 2329   ;
2777 ØEØA      MVI  C,ØA   ;
2779 CD2923    CALL 2329   ;
277C ØE15      MVI  C,15   ;
277E CD2923    CALL 2329   ;
2781 ØEØ4      MVI  C,Ø4   ;
```

```
2783 CD2923      CALL 2329     ;
2786 ØE Ø3       MVI  C,Ø3     ;
2788 CD2923      CALL 2329     ;
278B ØE ØA       MVI  C,ØA     ;
278D CD2923      CALL 2329     ;
2790 ØE Ø1       MVI  C,Ø1     ;
2792 CD2923      CALL 2329     ;
2795 ØE Ø3       MVI  C,Ø3     ;
2797 CD2923      CALL 2329     ;
279A ØE Ø4       MVI  C,Ø4     ;
279C CD2923      CALL 2329     ;
279F CD2923      CALL 2329     ;
27A2 ØE 1B       MVI  C,1B     ;
27A4 CD2923      CALL 2329     ;
27A7 78          MOV  A,B      ;
27A8 FE ØC       CPI  ØC       ;
27AA C2 BA27     JNZ  27BA     ;
27AD ØE 17       MVI  C,17     ;
27AF CD2923      CALL 2329     ;
27B2 ØE 13       MVI  C,13     ;
27B4 CD2923      CALL 2329     ;
27B7 C3 E027     JMP  27EO     ;
```

```
27BA FE0B       CPI  0B     ;
27BC C2CA27     JNZ  27CA    ;
27BF 0E17       MVI  C,17    ;
27C1 CD2923     CALL 2329    ;
27C4 CD2923     CALL 2329    ;
27C7 C3E027     JMP  27E0    ;


27CA FE0A       CPI  0A      ;
27CC C2DC27     JNZ  27DC    ;
27CF 0E17       MVI  C,17    ;
27D1 CD2923     CALL 2329    ;
27D4 0E16       MVI  C,16    ;
27D6 CD2923     CALL 2329    ;
27D9 C3E027     JMP  27E0    ;


27DC 48         MOV  C,B     ;
27DD CD2923     CALL 2329    ;
27E0 0E04       MVI  C,04    ;
27E2 CD2923     CALL 2329    ;
27E5 0E1F       MVI  C,1F    ;
27E7 CD2923     CALL 2329    ;
27EA 0E19       MVI  C,19    ;
27EC CD2923     CALL 2329    ;
```

```
27EF ØE12      MVI  C,12    ;
27F1 CD2923    CALL 2329    ;
27F4 ØE18      MVI  C,18    ;
27F6 CD2923    CALL 2329    ;
27F9 ØEØE      MVI  C,ØE    ;
27FB CD2923    CALL 2329    ;
27FE ØEØF      MVI  C,ØF    ;
2800 CD2923    CALL 2329    ;
2803 78        MOV  A,B     ;
2804 FE01      CPI  01      ;
2806 CA0E28    JZ   280E    ;
2809 0E05      MVI  C,05    ;
280B CD2923    CALL 2329    ;
280E 0600      MVI  B,00    ;
2810 CD3423    CALL 2334    ;
2813 0E1C      MVI  C,1C    ;
2815 CD2923    CALL 2329    ;
2818 0E0C      MVI  C,0C    ;
281A CD2923    CALL 2329    ;
281D 0E18      MVI  C,18    ;
281F CD2923    CALL 2329    ;
2822 0E04      MVI  C,04    ;
2824 CD2923    CALL 2329    ;
2827 CD3F23    CALL 233F    ;
282A FE16      CPI  16      ;
282C CABC27    JZ   27BC    ;
282F CD.B22F   CALL 2FB2    ;        CALL ESA
```

```
2832 B9        CMP  C       ;
2833 CA5C28    JZ   285C    ;
2836 4F        MOV  C,A     ;
2837 21B011    LXI  H,11B0  ;
283A 85        ADD  L       ;
283B 3D        DCR  A       ;
283C 6F        MOV  L,A     ;
283D 7E        MOV  A,M     ;
283E FEFF      CPI  FF      ;
2840 C21028    JNZ  2810    ;
2843 3ABA11    LDA  11BA    ;
2846 77        MOV  M,A     ;
2847 67        MOV  H,A     ;
2848 2E00      MVI  L,00    ;
284A DBC0      IN   C0      ;
284C E602      ANI  02      ;
284E CA4A28    JZ   284A    ;
2851 DB40      IN   40      ;
2853 FE00      CPI  00      ;
2855 C27128    JNZ  2871    ;
2858 2B        DCX  H       ;
2859 C34A28    JMP  284A    ;
```

```
285C 66        MOV  H,M    ;
285D 46        MOV  B,M    ;
285E 7E        MOV  A,M    ;
285F 2EFF      MVI  L,FF   ;
2861 BE        CMP  M      ;
2862 CA6928    JZ   2869   ;
2865 66        MOV  H,M    ;
2866 C35E28    JMP  285E   ;

2869 3ABA11    LDA  11BA   ;
286C 77        MOV  M,A    ;
286D 60        MOV  H,B    ;
286E C34828    JMP  2848   ;

2871 77        MOV  M,A    ;
2872 FE1C      CPI  1C     ;
2874 CA8A28    JZ   288A   ;
2877 7D        MOV  A,L    ;
2878 FEFE      CPI  FE     ;
287A CA8128    JZ   2881   ;
287D 23        INX  H      ;
287E C34A28    JMP  284A   ;
```

```
2881 23       INX  H      ;
2882 7E       MOV  A,M    ;
2883 FEFF     CPI  FF     ;
2885 C8       RZ          ;
2886 66       MOV  H,M    ;
2887 C34828   JMP  2848   ;
```

```
288A 0601     MVI  B,01   ;
288C DBC0     IN   C0     ;
288E E602     ANI  02     ;
2890 CA8C28   JZ   288C   ;
2893 DB40     IN   40     ;
2895 23       INX  H      ;
2896 77       MOV  M,A    ;
2897 7D       MOV  A,L    ;
2898 FEFE     CPI  FE     ;
289A CAB728   JZ   28B7   ;
289D FE1C     CPI  1C     ;
289F C24A28   JNZ  284A   ;
28A2 04       INR  B      ;
28A3 78       MOV  A,B    ;
28A4 FE05     CPI  05     ;
28A6 C28C28   JNZ  288C   ;
28A9 2B       DCX  H      ;
28AA 2B       DCX  H      ;
```

```
28AB 2B          DCX  H      ;
28AC 2B          DCX  H      ;
28AD 36FF        MVI  M,FF   ;
28AF 2EFE        MVI  L,FE   ;
28B1 7E          MOV  A,M    ;
28B2 32BA11      STA  11BA
28B5 74          MOV  M,H    ;
28B6 C9          RET          ;



28B7 23          INX  H      ;
28B8 66          MOV  H,M    ;
28B9 C39C28      JMP  289C   ;



28BC CD3F23      CALL 233F   ;
28BF CDB22F      CALL 2FB2   ;          CALL ESA
28C2 21B011      LXI  H,11B0 ;
28C5 85          ADD  L      ;
28C6 3D          DCR  A      ;
28C7 6F          MOV  L,A    ;
28C8 66          MOV  H,M    ;
28C9 2E00        MVI  L,00   ;
28CB 54          MOV  D,H    ;
28CC DBC0        IN   C0     ;
```

```
28CE E601       ANI  01     ;
28D0 CACC28     JZ   28CC   ;
28D3 7E         MOV  A,M    ;
28D4 D340       OUT  40     ;
28D6 23         INX  H      ;
28D7 FEFF       CPI  FF     ;
28D9 C2CC28     JNZ  28CC   ;
28DC CD3423     CALL 2334   ;
28DF CD3F23     CALL 233F   ;
28E2 FE0A       CPI  0A     ;
28E4 CAF328     JZ   28F3   ;
28E7 FE09       CPI  09     ;
28E9 CA6429     JZ   2964   ;
28EC FE06       CPI  06     ;
28EE C0         RNZ         ;
28EF 2B         DCX  H      ;
28F0 C34A28     JMP  284A   ;


28F3 CD3F23     CALL 233F   ;
28F6 CD7D2F     CALL 2F7D   ;   CALL DIGIT
28F9 47         MOV  B,A    ;
28FA EB         XCHG        ;
28FB E5         PUSH H      ;
28FC 7E         MOV  A,M    ;
28FD 23         INX  H      ;
```

```
28FE FE08       CPI  08      ;
2900 C2FC28     JNZ  28FC      ;
2903 05         DCR  B         ;
2904 78         MOV  A,B       ;
2905 FE00       CPI  00        ;
2907 C2FC28     JNZ  28FC      ;
290A 2B         DCX  H         ;
290B EB         XCHG           ;
290C 4E         MOV  C,M       ;
290D 23         INX  H         ;
290E CD2923     CALL 2329      ;
2911 FE08       CPI  08        ;
2913 C20C29     JNZ  290C      ;
2916 7E         MOV  A,M       ;
2917 FE02       CPI  02        ;
2919 C2AA29     JNZ  29AA      ;
291C EB         XCHG           ;
291D 2B         DCX  H         ;
291E 7E         MOV  A,M       ;
291F FE02       CPI  02        ;
2921 C26029     JNZ  2960      ;
2924 23         INX  H         ;
2925 23         INX  H         ;
2926 DBC0       IN   C0        ;
2928 E602       ANI  02        ;
292A CA2629     JZ   2926      ;
292D DB40       IN   40        ;
```

```
292F FE08       CPI  08    ;
2931 CA5C29     JZ   295C    ;
2934 77         MOV  M,A    ;
2935 23         INX  H      ;
2936 DBC0       IN   C0     ;
2938 E602       ANI  02     ;
293A CA3629     JZ   2936   ;
293D DB40       IN   40     ;
293F FE08       CPI  08     ;
2941 CA5029     JZ   2950   ;
2944 47         MOV  B,A    ;
2945 7E         MOV  A,M    ;
2946 FE08       CPI  08     ;
2948 CA5C29     JZ   295C   ;
294B 70         MOV  M,B    ;
294C 23         INX  H      ;
294D C33629     JMP  2936   ;
```



```
2950 7E         MOV  A,M    ;
2951 FE08       CPI  08     ;
2953 CA5C29     JZ   295C   ;
2956 3600       MVI  M,00   ;
2958 23         INX  H      ;
2959 C35029     JMP  2950   ;
```

```
295C E1          POP  H       ;
295D C3DC28      JMP  28DC    ;
```

```
2960 23          INX  H       ;
2961 C32429      JMP  2924    ;
```

```
2964 CD3F23      CALL 233F    ;
2967 CD7D2F      CALL 2F7D    ;        CALL DIGIT
296A 47          MOV  B,A     ;
296B EB          XCHG         ;
296C E5          PUSH H       ;
296D 7E          MOV  A,M     ;
296E 23          INX  H       ;
296F FE08        CPI  08      ;
2971 C2 6E29     JNZ  296E    ;
2974 05          DCR  B       ;
2975 78          MOV  A,B     ;
2976 FE00        CPI  00      ;
2978 C26E29      JNZ  296E    ;
297B 2B          DCX  H       ;
297C EB          XCHG         ;
```

```
297D 4E          MOV  C,M     ;
297E 23          INX  H       ;
297F CD2923      CALL 2329    ;
2982 FE08        CPI  08      ;
2984 C27D29      JNZ  297D    ;
2987 EB          XCHG         ;
2988 CD3F23      CALL 233F    ;
298B FE08        CPI  08      ;
298D CA5C29      JZ   295C    ;
2990 2B          DCX  H       ;
2991 7E          MOV  A,M     ;
2992 FE02        CPI  02      ;
2994 CA9829      JZ   2998    ;
2997 23          INX  H       ;
2998 23          INX  H       ;
2999 23          INX  H       ;
299A 7E          MOV  A,M     ;
299B FE08        CPI  08      ;
299D CA5C29      JZ   295C    ;
29A0 FE02        CPI  02      ;
29A2 CA9929      JZ   2999    ;
29A5 3608        MVI  M,08    ;
29A7 C31C29      JMP  291C    ;
```

```
29AA 2B          DCX  H       ;
29AB 3602        MVI  M,02    ;
29AD 2B          DCX  H       ;
29AE 3608        MVI  M,08    ;
29B0 C31C29      JMP  291C    ;
```

```
29B3 FE16        CPI  16      ;       PROGRAM  SUBFIN
29B5 C2BC29      JNZ  29BC    ;
29B8 211011      LXI  H,1110  ;
29BB C9          RET          ;
```

```
29BC FE17        CPI  17      ;
29BE C2C529      JNZ  29C5    ;
29C1 212011      LXI  H,1120  ;
29C4 C9          RET          ;
```



```
29C5 FE13        CPI  13      ;
29C7 C2CE29      JNZ  29CE    ;
29CA 213011      LXI  H,1130  ;
29CD C9          RET          ;
```

```
29CE FE01       CPI  01      ;
29D0 C2D729     JNZ  29D7    ;
29D3 214011     LXI  H,1140  ;
29D6 C9         RET          ;
```

```
29D7 FE0A       CPI  0A      ;
29D9 C2E029     JNZ  29E0    ;
29DC 215011     LXI  H,1150  ;
29DF C9         RET          ;
```

```
29E0 FE10       CPI  10      ;
29E2 C2E929     JNZ  29E9    ;
29E5 216011     LXI  H,1160  ;
29E8 C9         RET          ;
```

```
29E9 FE15       CPI  15      ;
29EB C2F229     JNZ  29F2    ;
29EE 217011     LXI  H,1170  ;
29F1 C9         RET          ;
```

```
29F2 FE07        CPI  07      ;
29F4 C2FB29      JNZ  29FB     ;
29F7 218011      LXI  H,1180   ;
29FA C9          RET            ;
```

```
29FB FE06        CPI  06       ;
29FD C2042A      JNZ  2A04     ;
2A00 219011      LXI  H,1190   ;
2A03 C9          RET            ;
```

```
2A04 21A011      LXI  H,11A0   ;
2A07 C9          RET            ;
```

PROGRAM SUBEST

```
2A08 06F0        MVI  B,F0     ;
2A0A 05          DCR  B        ;
2A0B 78          MOV  A,B      ;
2A0C FE00        CPI  00       ;
2A0E CA572A      JZ   2A57     ;
2A11 0E1F        MVI  C,1F     ;
2A13 CD1E23      CALL 231E     ;
2A16 DB03        IN   03       ;
```

```
2A18 E601       ANI  01     ;
2A1A CA0A2A     JZ   2A0A   ;
2A1D DB01       IN   01     ;
2A1F 4F         MOV  C,A    ;
2A20 CD2923     CALL 2329   ;
2A23 FE1A       CPI  1A     ;
2A25 CA2F2A     JZ   2A2F   ;
2A28 DB03       IN   03     ;
2A2A E602       ANI  02     ;
2A2C CA1D2A     JZ   2A1D   ;
2A2F 47         MOV  B,A    ;
2A30 DB03       IN   03     ;
2A32 E602       ANI  02     ;
2A34 CA302A     JZ   2A30   ;
2A37 DB01       IN   01     ;
2A39 4F         MOV  C,A    ;
2A3A CD2923     CALL 2329   ;
2A3D FE03       CPI  03     ;
2A3F CA442A     JZ   2A44   ;
2A42 48         MOV  C,B    ;
2A43 C9         RET         ;
```


```
2A44 DB03       IN   03     ;
2A46 E602       ANI  02     ;
2A48 CA442A     JZ   2A44   ;
```

```
2A4B DB01       IN   01      ;
2A4D 4F         MOV  C,A     ;
2A4E CD2923     CALL 2329    ;
2A51 FE08       CPI  08      ;
2A53 C2442A     JNZ  2A44    ;
2A56 C9         RET          ;



2A57 CD3423     CALL 2334    ;
2A5A 0E1F       MVI  C,1F    ;
2A5C CD2923     CALL 2329    ;
2A5F 0E0D       MVI  C,0D    ;
2A61 CD2923     CALL 2329    ;
2A64 0E03       MVI  C,03    ;
2A66 CD2923     CALL 2329    ;
2A69 0E06       MVI  C,06    ;
2A6B CD2923     CALL 2329    ;
2A6E 0E12       MVI  C,12    ;
2A70 CD2923     CALL 2329    ;
2A73 C9         RET          ;
```

PROGRAM SUBC

```
2A74 CD0E1B     CALL 1B0E    ;
2A77 CD2923     CALL 2329    ;
2A7A 0E19       MVI  C,19    ;
```

```
2A7C CD2923      CALL 2329     ;
2A7F ØE04        MVI  C,04     ;
2A81 CD2923      CALL 2329     ;
2A84 CD3F23      CALL 233F     ;
2A87 47          MOV  B,A      ;
2A88 DBCØ        IN   CØ       ;
2A8A E6Ø2        ANI  Ø2       ;
2A8C CA882A      JZ   2A88     ;
2A8F DB4Ø        IN   4Ø       ;
2A91 FE11        CPI  11       ;
2A93 CAE92A      JZ   2AE9     ;
2A96 21CØ11      LXI  H,11CØ   ;
2A99 23          INX  H        ;
2A9A 77          MOV  M,A      ;
2A9B 2B          DCX  H        ;
2A9C 7Ø          MOV  M,B      ;
2A9D 23          INX  H        ;
2A9E DBCØ        IN   CØ       ;
2AAØ E6Ø2        ANI  Ø2       ;
2AA2 CADB4Ø      JZ   4ØDB     ;
2AA5 23          INX  H        ;
2AA6 77          MOV  M,A      ;
2AA7 FE11        CPI  11       ;
2AA9 C29E2A      JNZ  2A9E     ;
2AAC DBCØ        IN   CØ       ;
2AAE E6Ø2        ANI  Ø2       ;
2ABØ CAAC2A      JZ   2AAC     ;
```

```
2AB3 DB40        IN   40      ;
2AB5 32D011      STA  11D0    ;
2AB8 CD082A      CALL 2A08    ;          CALL SUBEST
2ABB 78          MOV  A,B     ;
2ABC FE00        CPI  00      ;
2ABE C8          RZ           ;
2ABF 21C011      LXI  H,11C0  ;
2AC2 CD572D      CALL 2D57    ;          CALL SUBCON
2AC5 78          MOV  A,B     ;
2AC6 FEFF        CPI  FF      ;
2AC8 C2102B      JNZ  2B10    ;
2ACB 3ABD11      LDA  11BD    ;
2ACE 32BF11      STA  11BF    ;
2AD1 3ABC11      LDA  11BC    ;
2AD4 3C          INR  A       ;
2AD5 3C          INR  A       ;
2AD6 32BE11      STA  11BE    ;
2AD9 3AD011      LDA  11D0    ;
2ADC 3D          DCR  A       ;
2ADD 32D011      STA  11D0    ;
2AE0 3EFF        MVI  A,FF    ;
2AE2 32D111      STA  11D1    ;
2AE5 CD332C      CALL 2C33    ;          CALL SUBWLT
2AE8 C9          RET          ;
```

```
2AE9 DBC0       IN   C0      ;
2AEB E602       ANI  02      ;
2AED CA E92A    JZ   2AE9    ;
2AF0 DB40       IN   40      ;
2AF2 32D011     STA  11D0    ;
2AF5 78         MOV  A,B     ;
2AF6 CDB329     CALL 29B3    ;          CALL SUBFIN
2AF9 EB         XCHG         ;
2AFA 21C011     LXI  H,11C0  ;
2AFD 1A         LDAX D       ;
2AFE 77         MOV  M,A     ;
2AFF 13         INX  D       ;
2B00 23         INX  H       ;
2B01 FE11       CPI  11      ;
2B03 C2 FD2A    JNZ  2AFD    ;
2B06 CD082A     CALL 2A08    ;          CALL SUBEST
2B09 78         MOV  A,B     ;
2B0A FE00       CPI  00      ;
2B0C C2 BF2A    JNZ  2ABF    ;
2B0F C9         RET          ;
```



```
2B10 CD8E2E     CALL 2E8E    ;          CALL SUB F
2B13 C9         RET          ;
```

```
2B14 CD3423       CALL 2334     ;
2B17 ØE1F         MVI  C,1F     ;
2B19 CD2923       CALL 2329     ;
2B1C ØEØC         MVI  C,ØC     ;
2B1E CD2923       CALL 2329     ;
2B21 ØE18         MVI  C,18     ;
2B23 CD2923       CALL 2329     ;
2B26 ØEØ4         MVI  C,Ø4     ;
2B28 CD2923       CALL 2329     ;
2B2B CD2923       CALL 2329     ;
2B2E CD3F23       CALL 233F     ;
2B31 47           MOV  B,A      ;
2B32 DBCØ         IN   CØ       ;
2B34 E6Ø2         ANI  Ø2       ;
2B36 CA 362B      JZ   2B36     ;
2B39 DB4Ø         IN   4Ø       ;
2B3B FE11         CPI  11       ;
2B3D CA E62B      JZ   2BE6     ;
2B4Ø 21CØ11       LXI  H,11CØ   ;
2B43 23           INX  H        ;
2B44 77           MOV  M,A      ;
2B45 2B           DCX  H        ;
2B46 7Ø           MOV  M,B      ;
2B47 23           INX  H        ;
2B48 DBCØ         IN   CØ       ;
2B4A E6Ø2         ANI  Ø2       ;
```

```
2B4C CA482B      JZ   2B48    ;
2B4F DB40        IN   40      ;
2B51 23          INX  H       ;
2B52 77          MOV  M,A     ;
2B53 FE11        CPI  11      ;
2B55 C2 482B     JNZ  2B48    ;
2B58 CD3423      CALL 2334    ;
2B5B 0E1F        MVI  C,1F    ;
2B5D CD2923      CALL 2329    ;
2B60 0E1C        MVI  C,1C    ;
2B62 CD2923      CALL 2329    ;
2B65 0E0C        MVI  C,0C    ;
2B67 CD2923      CALL 2329    ;
2B6A 0E18        MVI  C,18    ;
2B6C CD2923      CALL 2329    ;
2B6F 0E04        MVI  C,04    ;
2B71 CD2923      CALL 2329    ;
2B74 CD3F23      CALL 233F    ;
2B77 32D111      STA  11D1    ;
2B7A CD3423      CALL 2334    ;
2B7D 0E1F        MVI  C,1F    ;
2B7F CD2923      CALL 2329    ;
2B82 0E10        MVI  C,10    ;
2B84 CD2923      CALL 2329    ;
2B87 0E1B        MVI  C,1B    ;
2B89 CD2923      CALL 2329    ;
2B8C 0E19        MVI  C,19    ;
```

```
2B8E CD2923      CALL 2329      ;
2B91 0E04        MVI  C,04      ;
2B93 CD2923      CALL 2329      ;
2B96 CD2923      CALL 2329      ;
2B99 CD3F23      CALL 233F      ;
2B9C FE0C        CPI  0C        ;
2B9E C2012A      JNZ  2A01      ;
2BA1 CD082A      CALL 2A08      ;
2BA4 78          MOV  A,B       ;
2BA5 FE00        CPI  00        ;
2BA7 C8          RZ             ;
2BA8 21C011      LXI  H,11C0    ;
2BAB CD572D      CALL 2D57      ;
2BAE 78          MOV  A,B       ;
2BAF FEFF        CPI  FF        ;
2BB1 C2132C      JNZ  2C13      ;
2BB4 3ABD11      LDA  11BD      ;
2BB7 32BF11      STA  11BF      ;
2BBA 3ABC11      LDA  11BC      ;
2BBD FE3A        CPI  3A        ;
2BBF CACC2B      JZ   2BCC      ;
2BC2 FE3B        CPI  3B        ;
2BC4 CAE12B      JZ   2BE1      ;
2BC7 3C          INR  A         ;
2BC8 3C          INR  A         ;
2BC9 32BE11      STA  11BE      ;
2BCC 3E00        MVI  A,00      ;
```

CALL SUBEST

CALL SUBCON

```
2BCE 32BE11     STA  11BE    ;
2BD1 3ABD11     LDA  11BD    ;
2BD4 3C         INR  A       ;
2BD5 32BF11     STA  11BF    ;
2BD8 3E05       MVI  A,05    ;
2BDA 32D011     STA  11D0    ;
2BDD CD332C     CALL 2C33    ;          CALL SUBWLT
2BE0 C9         RET          ;

2BE1 3E01       MVI  A,01    ;
2BE3 C3CE2B     JMP  2BCE    ;

2BE6 78         MOV  A,B     ;
2BE7 CDB329     CALL 29B3    ;          CALL SUBFIN
2BEA EB         XCHG         ;
2BEB 21C011     LXI  H,11C0  ;
2BEE 1A         LDAX D       ;
2BEF 77         MOV  M,A     ;
2BF0 13         INX  D       ;
2BF1 23         INX  H       ;
2BF2 FE11       CPI  11      ;
2BF4 C2EE2B     JNZ  2BEE    ;
2BF7 CD082A     CALL 2A08    ;          CALL SUBEST
```

```
2BFA 78          MOV  A,B     ;
2BFB FE00        CPI  00      ;
2BFD C2A82B      JNZ  2BA8    ;
2C00 C9          RET           ;
```

```
2C01 CD7D2F      CALL 2F7D    ;        CALL DIGIT
2C04 32BF11      STA  11BF    ;
2C07 CD3F23      CALL 233F    ;
2C0A CD7D2F      CALL 2F7D    ;        CALL DIGIT
2C0D 32BE11      STA  11BE    ;
2C10 C3D82B      JMP  2BD8    ;
```

```
2C13 21B011      LXI  H,11B0  ;
2C16 3AD111      LDA  11D1    ;
2C19 85          ADD  L       ;
2C1A 3D          DCR  A       ;
2C1B 6F          MOV  L,A     ;
2C1C 66          MOV  H,M     ;
2C1D 2E00        MVI  L,00    ;
2C1F 4E          MOV  C,M     ;
2C20 CD2923      CALL 2329    ;
2C23 CD1E23      CALL 231E    ;
2C26 23          INX  H       ;
```

```
2C27 FEFF       CPI  FF      ;
2C29 C21F2C     JNZ  2C1F    ;
2C2C CD2F2F     CALL 2F2F    ;          CALL END
2C2F CD8E2E     CALL 2E8E    ;          CALL SUBF
2C32 C9         RET          ;
```

PROGRAM SUBWLT

```
2C33 210010     LXI  H,1000  ;
2C36 3AD411     LDA  11D4    ;
2C39 FEFF       CPI  FF      ;
2C3B CABA2C     JZ   2CBA    ;
2C3E 47         MOV  B,A     ;
2C3F 1600       MVI  D,00    ;
2C41 1E16       MVI  E,16    ;
2C43 05         DCR  B       ;
2C44 19         DAD  D       ;
2C45 78         MOV  A,B     ;
2C46 FE01       CPI  01      ;
2C48 C2432C     JNZ  2C43    ;
2C4B 3ABF11     LDA  11BF    ;
2C4E BE         CMP  M       ;
2C4F CAF62C     JZ   2CF6    ;
2C52 DAD32C     JC   2CD3    ;
2C55 23         INX  H       ;
2C56 23         INX  H       ;
2C57 23         INX  H       ;
```

```
2C58 23          INX  H      ;
2C59 7E          MOV  A,M    ;
2C5A BD          CMP  L      ;
2C5B CA7C2C      JZ   2C7C   ;
2C5E 6E          MOV  L,M    ;
2C5F 23          INX  H      ;
2C60 66          MOV  H,M    ;
2C61 3ABF11      LDA  11BF   ;
2C64 BE          CMP  M      ;
2C65 CA052D      JZ   2D05   ;
2C68 DA112D      JC   2D11   ;
2C6B 23          INX  H      ;
2C6C 23          INX  H      ;
2C6D 23          INX  H      ;
2C6E 23          INX  H      ;
2C6F 7C          MOV  A,H    ;
2C70 32D211      STA  11D2   ;
2C73 7D          MOV  A,L    ;
2C74 32D311      STA  11D3   ;
2C77 7E          MOV  A,M    ;
2C78 BD          CMP  L      ;
2C79 C2 5E2C     JNZ  2C5E   ;
2C7C E5          PUSH H      ;
2C7D 210010      LXI  H,1000 ;
2C80 3A473C      LDA  3C47   ;
2C83 32D511      STA  11D5   ;
2C86 1600        MVI  D,00   ;
```

```
2C88 1E16       MVI  E,16    ;
2C8A Ø5         DCR  B       ;
2C8B 19         DAD  D       ;
2C8C 78         MOV  A,B     ;
2C8D FEØ1       CPI  Ø1      ;
2C8F C28A2C     JNZ  2C8A    ;
2C92 44         MOV  B,H     ;
2C93 4D         MOV  C,L     ;
2C94 E1         POP  H       ;
2C95 71         MOV  M,C     ;
2C96 23         INX  H       ;
2C97 7Ø         MOV  M,B     ;
2C98 6Ø         MOV  H,B     ;
2C99 69         MOV  L,C     ;
2C9A C3C62C     JMP  2CC6    ;
```

```
2C9D 3ABF11     LDA  11BF    ;
2CAØ 77         MOV  M,A     ;
2CA1 23         INX  H       ;
2CA2 23         INX  H       ;
2CA3 3ABE11     LDA  11BE    ;
2CA6 77         MOV  M,A     ;
2CA7 23         INX  H       ;
2CA8 3ADØ11     LDA  11DØ    ;
2CAB 77         MOV  M,A     ;
```

```
2CAC 23          INX  H      ;
2CAD 3AD111      LDA  11D1   ;
2CB0 77          MOV  M,A    ;
2CB1 C3462D      JMP  2D46
```

```
2CBA 3AD511      LDA  11D5   ;
2CB7 32D411      STA  11D4   ;
2CBA 47          MOV  B,A    ;
2CBB 3C          INR  A      ;
2CBC 32D511      STA  11D5   ;
2CBF 1600        MVI  D,00   ;
2CC1 1E16        MVI  E,16   ;
2CC3 19          DAD  D      ;
2CC4 44          MOV  B,H    ;
2CC5 4D          MOV  C,L    ;
2CC6 E5          PUSH H      ;
2CC7 23          INX  H      ;
2CC8 23          INX  H      ;
2CC9 23          INX  H      ;
2CCA 23          INX  H      ;
2CCB 23          INX  H      ;
2CCC 75          MOV  M,L    ;
2CCD 23          INX  H      ;
2CCE 74          MOV  M,H    ;
2CCF E1          POP  H      ;
2CD0 C3 9D2C     JMP  2C9D   ;
```

```
2CD3 E5          PUSH H        ;
2CD4 210010      LXI  H,1000   ;
2CD7 3AD511      LDA  11D5     ;
2CDA 32D411      STA  11D4     ;
2CDD 47          MOV  B,A      ;
2CDE 3C          INR  A        ;
2CDF 32D511      STA  11D5     ;
2CE2 1600        MVI  D,00     ;
2CE4 1E16        MVI  E,16     ;
2CE6 05          DCR  B        ;
2CE7 19          DAD  D        ;
2CE8 78          MOV  A,B      ;
2CE9 FE01        CPI  01       ;
2CEB  C2E62C      JNZ  2CE6     ;
2CEE EB          XCHG          ;
2CEF E1          POP  H        ;
2CF0 44          MOV  B,H      ;
2CF1 4D          MOV  C,L      ;
2CF2 EB          XCHG          ;
2CF3 C3C62C      JMP  2CC6     ;
```

```
2CF6 23          INX  H        ;
2CF7 3ABEE11      LDA  11BE     ;
2CFA BE          CMP  M        ;
2CFB CA012D      JZ   2D01     ;
```

```
2CFE D2562C      JNC  2C56     ;
2D01 2B          DCX  H        ;
2D02 C3D32C      JMP 2CD3      ;


2D05 23          INX  H        ;
2D06 3ABE11      LDA  11BE     ;
2D09 BE          CMP  M        ;
2D0A CA1D2D      JZ   2D1D     ;
2D0D D26C2C      JNC 2C6C      ;
2D10 2B          DCX  H        ;
2D11 E5          PUSH H        ;
2D12 210010      LXI  H,1000   ;
2D15 3AD511      LDA  11D5     ;
2D18 47          MOV   B,A     ;
2D19 3C          INR  A        ;
2D1A 32D511      STA  11D5     ;
2D1D 1600        MVI  D,00     ;
2D1F 1E16        MVI  E,16     ;
2D21 05          DCR  B        ;
2D22 19          DAD  D        ;
2D23 78          MOV  A,B      ;
2D24 FE01        CPI  01       ;
2D26 C2212D      JNZ  2D21     ;
2D29 EB          XCHG           ;
2D2A E1          POP  H        ;
```

```
2D2B D5          PUSH D       ;
2D2C 13          INX  D       ;
2D2D 13          INX  D       ;
2D2E 13          INX  D       ;
2D2F 13          INX  D       ;
2D30 13          INX  D       ;
2D31 7D          MOV  A,L     ;
2D32 12          STAX D       ;
2D33 13          INX  D       ;
2D34 7C          MOV  A,H     ;
2D35 12          STAX D       ;
2D36 D1          POP  D       ;
2D37 33AD311     LDA  11D3    ;
2D3A 6F          MOV  L,A     ;
2D3B 3AD211      LDA  11D2    ;
2D3E 67          MOV  H,A     ;
2D3F 73          MOV  M,E     ;
2D40 23          INX  H       ;
2D41 72          MOV  M,D     ;
2D42 EB          XCHG         ;
2D43 C39D2C      JMP  2C9D    ;
```

```
2D46 23          INX  H       ;
2D47 23          INX  H       ;
2D48 23          INX  H       ;
```

```
2D49 EB          XCHG          ;
2D4A 21C010      LXI  H,10C0   ;
2D4D 7E          MOV  A,,M     ;
2D4E 12          STAX D        ;
2D4F 13           INX  D       ;
2D50 23          INX  H        ;
2D51 FE11        CPI  11       ;
2D53 C24D2D      JNZ  2D4D     ;
2D56 C9          RET           ;
```

PROGRAM SUBCON

```
2D57 CD3423      CALL 2334     ;
2D5A 0E1B        MVI  C,1B     ;
2D5C CD2923      CALL 2329     ;
2D5F CD1E23      CALL 231E     ;
2D62 4E          MOV  C,M      ;
2D63 23          INX  H        ;
2D64 CD29923      CALL 2329    ;
2D67 CD1E23      CALL 231E     ;
2D6A FE11        CPI  11       ;
2D6C C2622D      JNZ  2D62     ;
2D6F DB03        IN   03       ;
2D71 E602        ANI  02       ;
2D73 CA6E2D      JZ   2D6E     ;
2D76 DB01        IN   01       ;
2D78 4F          MOV  C,A      ;
```

```
2D79 CD2923      CALL 2329    ;
2D7C FE09        CPI  09      ;
2D7E C26F2D      JJNZ 2D6F    ;
2D81 0600        MVI  B,00    ;
2D83 DBC0        IN   C0      ;
2D85 E602        ANI  02      ;
2D87 CA832D      JZ   2D83    ;
2D8A DB40        IN   40      ;
2D8C 4F          MOV  C,A     ;
2D8D CD1E23      CALL 231E    ;
2D90 04          INR  B       ;
2D91 78          MOV  A,B     ;
2D92 FE14        CPI  14      ;
2D94 C2832D      JNZ  2D83    ;
2D97 DB03        IN   03      ;
2D99 E602        ANI  02      ;
2D9B CA972D      JZ   2D97    ;
2D9E DB01        IN   01      ;
2DA0 FE1B        CPI  1B      ;
2DAA2 CAC82D     JZ   2DC8    ;
2DA5 FE1F        CPI  1F      ;
2DA7 CAC82D      JZ   2DC8    ;
2DAA FE08        CPI  08      ;
2DAC CAC82D      JZ   2DC8    ;
2DAF FE02        CPI  02      ;
2DB1 CAC82D      JZ   2DC8    ;
2DB4 FE04        CPI  04      ;
```

```
2DB6 CA.C82D      JZ   2DC8     ;
2DB9 FE18         CPI  18       ;
2DBB CA.CC2D      JZ   2DCC     ;
2DBE FE09         CPI  09       ;
2DC0 CA.0B2E      JZ   2E0B     ;
2DC3 FE0C         CPI  0C       ;
2DC5 CA362E       JZ    2E36    ;
2DC8 4F           MOV  C,A      ;
2DC9 CD2923       CALL 2329     ;
2DCC 4F           MOV  C,A      ;
2DCD CD2923       CALLL 2329     ;
2DD0 DB03         IN   03       ;
2DD2 E602         ANI  02       ;
2DD4 CAD02D       JZ    2DD0    ;
2DD7 DB01         IN   01       ;
2DD9 FE0E         CPI  0E       ;
2DDB C2592E       JNZ  2E59     ;
2DDE 4F           MOV  C,A      ;
2DDF CD2923       CALL 2329     ;
2DE2 DB03         IN   03       ;
2DE4 E602         ANI  02       ;
2DE6 CAE22D       JZ   2DE2     ;
2DE9 DB01         IN   01       ;
2DEB FE0E         CPI  0E       ;
2DED C2592E       JNZ  2E59     ;
2DF0 4F           MOV  C,A      ;
2DF1 CD2923       CALL 2329     ;
```

```
2DF4 Ø6FF       MVI  B,FF    ;
2DF6 ØE17       MVI  C,17    ;
2DF8 CD2923     CALL 2329    ;
2DFB ØE1D       MVI  C,1D    ;
2DFD CD2923     CALL 2329    ;
2EØØ ØE17       MVI  C,17    ;
2EØ2 CD2923     CALL 2329    ;
2EØ5 ØE1D       MVI  C,1D    ;
2EØ7 CD2923     CALL 2329    ;
2EØA C9         RET          ;

2EØB 4F         MOV  C,A     ;
2EØC CD2923     CALL 2329    ;
2EØF DBØ3       IN   Ø3      ;
2E11 E6Ø2       ANI  Ø22     ;
2E13 CAOF2E     JZ   2EOF    ;
2E16 DBØ1       IN   Ø1      ;
2E18 FEØ1       CPI  Ø1      ;
2E1A C2592E     JNZ  2E59    ;
2E1D 4F         MOV  C,A     ;
2E1E CD2923     CALL 2329    ;
2E21 DBØ3       IN   Ø3      ;
2E23 E6Ø2       ANI  ØZ      ;
2E25 CA212E     JZ   2E21    ;
2E28 DBØ1       IN   Ø1      ;
```

```
2E2A FE0A       CPI  0A      ;
2E2C C2592E     JNZ  2E59     ;
2E2F 4F         MOV  C,A      ;
2E30 CD2923     CALL 2329     ;
2E33 06FF       MVI  B,FF     ;
2E35 C9         RET           ;
```

```
2E36 4F         MOV  C,A      ;
2E37 CD2923     CALL 2329     ;
2E3A DB03       IN   03       ;
2E3C E602       ANI  02       ;
2E3E CA3A2E     JZ   2E3A     ;
2E41 DB01       IN   01       ;
2E43 FE03       CPI  03       ;
2E45 CA522E     JZ   2E52     ;
2E48 FE16       CPI  16       ;
2E4A CA522E     JZ   2E52     ;
2E4D FE0E       CPI  0E       ;
2E4F C2592E     JNZ  2E59     ;
2E52 4F         MOV  C,A      ;
2E53 CD2923     CALL 2329     ;
2E56 06FF       MVI  B,FF     ;
2E58 C9         RET           ;
```

```
2E59 4F          MOV  C,A     ;
2E5A CD2923      CALL 2329    ;
2E5D 3ABB11      LDA  11BB    ;
2E60 FE1E        CPI  1E      ;
2E62 DA473E      JC   3E47    ;
2E65 3C          INR  A       ;
2E66 90          SUB  B       ;
2E67 47          MOV  B,A     ;
2E68 3E1E        MVI  A,1E    ;
2E6A 90          SUB  B       ;
2E6B 47          MOV  B,A     ;
2E6C DB03        IN   03      ;
2E6E E602        ANI  02      ;
2E70 CA6C2E      JZ   2E6C    ;
2E73 DB01        IN   01      ;
2E75 4F          MOV  C,A     ;
2E76 CD2923      CALL 2329    ;
2E79 3ABB11      LDA  11BB    ;
2E7C B8          CMP  B       ;
2E7D C8          RZ           ;
2E7E DB03        IN   03      ;
2E80 E620        ANI  20      ;
2E82 C26C2E      JNZ  2E6C    ;
2E85 06FF        MVI  B,FF    ;
2E87 C9          RET          ;
```

```
2E88 C61E        ADI   1E      ;
2E8A 47          MOV   B,A     ;
2E8B C36C2E      JMP   2E6C    ;
```

PROGRAM SUBF

```
2E8E DB03        IN    03      ;
2E990 E602        ANI   02      ;
2E92 CAA22E      JZ    2EA2    ;
 2E95 DB01        IN    01      ;
2E97 4F          MOV   C,A     ;
2E98 CD29923      CALL  2329    ;
2E9B DB03        IN    03      ;
2E9D E602        ANI   02      ;
2E9F C2952E      JNZ   2E95    ;
2EA2 DBC0        IN    C0      ;
2EA4 E602        ANI   02      ;
2EA6 CAD62E      JZ    2ED6    ;
2EA9 DB40        IN    40      ;
2EAB 4F           MOV   C,A     ;
2EAC FEFF        CPI   FF      ;
2EAE CACD2E      JZ    2ECD    ;
2EB1 FE1C        CPI   1C      ;
2EB3 CADE2E      JZ    2EDE    ;
2EB6 FE12        CPI   12      ;
2EB8 CAA92E      JZ    2EA9    ;
2EBB CD1E23      CALL  231E    ;
```

```
2EBE DBC0       IN   C0      ;
2EC0 E620       ANI  20      ;
2EC2 C8         RZ           ;
2EC3 DBC0       IN   C0      ;
2EC5 E602       ANII 02      ;
2EC7 C2A92E     JNZ  2EA9    ;
2ECA C38E2E     JMP  2E8E    ;


2ECD CD3423     CALL 2334    ;
2ED0 CD2F2F     CALL 2F2F    ;
2ED3 C38E2E     JMP  2E8E    ;


2ED6 DB03       IN   03      ;
2ED8 E620       ANI  20      ;
2EDA C28E2E     JNZ  2E8E    ;
2EDD C9         RET          ;


2EDE 0601       MVI  B,01    ;
2EE0 CD1E23     CALL 231E    ;
2EE3 DBC0       IN   C0      ;
2EE5 E602       ANI  02      ;
```

```
2EE7 CA.E32E      JZ   2EE3     ;
2EEA DB40         IN   40       ;
2EEC 4F           MOV  C,A      ;
2EED CD1E23       CALL 231E     ;
2EF0 FE1C         CPI  1C       ;
2EF2 C2FF2E       JNZ  2EFF     ;
2EF5 04           INR  B        ;
2EF6 78           MOV  A,B      ;
2EF7 FE05         CPI  05       ;
2EF9 C2E32E       JNZ  2EE3     ;
2EFC C38E2E       JMP  2E8E     ;
```

```
2EFF FE12         CPI  12       ;
2F01 C2BB2E       JNZ  2EBB     ;
2F04 0601         MVI  B,01     ;
2F06 DB CO        IN   CO       ;
2F08 E602         ANI  02       ;
2F0A CA062F       JZ   2F06     ;
2F0D DB40         IN   40       ;
2F0F 4F           MOV  C,A      ;
2F10 CD1E23       CALL 2331E    ;
2F13 FE12         CPI  12       ;
2F15 C2252F       JNZ  2F25     ;
2F18 04           INR  B        ;
2F19 78           MOV  A,B      ;
```

```
2F1A FE05       CPI  05      ;
2F1C C2062F     JNZ  2F06    ;
2F1F CD1E23     CALL 231E    ;
2F22 C3042F     JMP  2F04    ;



2F25 FE1C       CPI  1C      ;
2F27 C2BE2E     JNZ  2EBE    ;
2F2A 0601       MVI  B,01    ;
2F2C C3E32E     JMP  2EE3    ;



2F2F 0E1B       MVI  C,1B    ;        PROGRAM END
2F31 CD1E23     CALL 231E    ;
2F34 0E09       MVI  C,09    ;
2F36 CD1E23     CALL 231E    ;
2F39 DB03       IN   03      ;
2F3B E602       ANI  02      ;
2F3D CA6E2F     JZ   2F6E    ;
2F40 DB01       IN   01      ;
2F42 4F         MOV  C,A     ;
2F43 CD2923     CALL 2329    ;
2F46 DB03       IN   03      ;
2F48 E602       ANI  02      ;
2F4A C2402F     JNZ  2F40    ;
```

```
2F4D 0E1C       MVI   C,1C    ;
2F4F CD2923     CALL  2329    ;
2F52 CD1E23     CALL  231E    ;
2F55 CD2923     CALL  2329    ;
2F58 CD1E23     CALL  231E    ;
2F5B CD2923     CALL  2329    ;
2F5E CD1E23     CALL  231E    ;
2F61 CD2923     CALL  2329    ;
2F64 CD1E23     CALL  231E    ;
2F67 CD2923     CALL  2329    ;
2F6A CD1E23     CALL  231E    ;
2F6D C9         RET           ;
2F6E DBC0       IN    C0      ;
2F70 E602       ANI   02      ;
2F72 CA392F     JZ    2F39    ;
2F75 DB40       IN    40      ;
2F77 CD2923     CALL  2329    ;
2F7A C3392F     JMP   2F39    ;

2F7D FE0E       CPI   0E      ;  PROGRAM DIGIT
2F7F CA7D2F     JZ    2F7D    ;
2F82 FE1C       CPI   1C      ;
2F84 CA7D2F     JZ    2F7D    ;
2F87 FE16       CPI   16      ;
2F89 CAAA2F     JZ    2FAA    ;
2F8C CDB22F     CALL  2FB2    ;  CALL ESA
2F8F 47         MOV   B,A     ;
```

```
2F90 17          RAL          ;
2F91 17          RAL          ;
2F92 17          RAL          ;
2F93 17          RAL          ;
2F94 6F          MOV  L,A     ;
2F95 CD3F23      CALL 233F    ;
2F98 FE0E        CPI  0E      ;
2F9A CAAE2F      JZ   2FAE    ;
2F9D FE1C        CPI  1C      ;
2F9F CAAE2F      JZ   2FAE    ;
2FA2 CDB22F      CALL 2FB2    ;
2FA5 B5          ORA  L       ;
2FA6 2612        MVI  H,12    ;
2FA8 7E          MOV  A,M     ;
2FA9 C9          RET          ;


2FAA 6F          MOV  L,A     ;
2FAB C3952F      JMP  2F95    ;


2FAE 68          MOV  L,B     ;
2FAF C3A62F      JMP  2FA6    ;
```

```
2FB2 FE16       CPI  16      ;
2FB4 C2BA2F     JNZ  2FBA    ;
2FB7 3E00       MVI  A,00    ;
2FB9 C9         RET          ;


2FBA FE17       CPI  17      ;
2FBC C2C22F     JNZ  2FC2    ;
2FBF 3E01       MVI  A,01    ;
2FC1 C9         RET          ;


2FC2 FE13       CPI  13      ;
2FC4 C2CA2F     JNZ  2FCA    ;
2FC7 3E02       MVI  A,02    ;
2FC9 C9         RET          ;


2FCA FE01       CPI  01      ;
2FCC C2D22F     JNZ  2FD2    ;
2FCF 3E03       MVI  A,03    ;
2FD1 CC9        RET          ;
```

```
2FD2 FE0A       CPI  0A      ;
2FDD4 C2DA2F     JNZ  2FDA    ;
2FD7 3E04       MVI  A,04     ;
2FD9 C9         RET           ;

2FDA FE10       CPI  10       ;
2FDC C2E22F     JNZ  2FE2     ;
2FDF 3E05       MVI  A,05     ;
2FE1 C9         RET           ;

2FE2 FE15       CPI  15       ;
2FE4 C2EA2F     JNZ  2FEA     ;
2FE7 3E06       MVI  A,06     ;
2FE9 C9         RET           ;

 2FEA FE07       CPI  07      ;
2FEC C2F22F     JNZ  2FF2     ;
2FEF 3E07       MVI  A,07      ;
2FF1 C9         RET           ;

2FF2 FE06       CPI  06       ;
2FF4 C2FA2F     JNZ  2FFA     ;
2FF7 3E08       MVI  A,08     ;
2FF9 C9         RET           ;

2FFA 3E09       MVI  A,09     ;
2FFC C9         RET           ;
```

ประวัติ

นายเทพา สุขผดุง เกิดเมื่อวันที่ 26 พฤศจิกายน 2495 ที่จังหวัดพระนครศรีอยุธยา สำเร็จการศึกษา วิศวกรรมศาสตร์บัณฑิต จากคณะวิศวกรรมเทคโนโลยี่ วิทยาลัยเทคโนโลยี่และอาชีวะศึกษา เมื่อปี พ.ศ. 2520

ปัจจุบันทำงานในตำแหน่ง นายช่างโทรคมนาคม ระดับ 4 ประจำสถานีโทรคมนาคมเคเบิลใต้น้ำ ชลี 1 เพชรบุรี กองเคเบิลใต้น้ำ การสื่อสารแห่งประเทศไทย