รายการอ้างอิง

1. Craig Marven and Gillian Ewers. A Simple Approach to Digital Signal Processing. (n.p.): John wiley & sons, 1996.
2. Emmanuel C. Ifeachor and Barrie W. Jervis. Digital Signal Processing A Practical Approach. (n.p.): Addison-Wesley, 1993.
3. John G. Proakis and Dimitris G. Manolakis.Digital Signal Process Principle, Algorithms, and Applications. (n.p.): Macmillan Publishing Company., 1990.
4. TMS320C3X User's Guide. Texas. Texas Instruments, 1994.
5. TMS320C3X DPS Starter Kit User's Guide. Texas. Texas Instruments, 1996.
6. R. Asada and S. Nishikawa. Broadcast Camera Using Digital Signal Processing. (n.p.): Broadcast Convention, 1990.
7. N.F. Jiang, Y.K. Lau and W.C. Siu. Real-Time Multiprocessor System Using Orthogonal Memory Access for Digital Signal Processing. (n.p.): IEEE transaction on circuits and system. Vol.1, May 1989.
8. Pierre. Siohan and Acyl Benslimane. Finite Precision Design of Optimal Linear Phase 2-D FIR Digital Filter. (n.p.): IEEE transaction on circuits and system. Vol.36. No.1, January 1989.

บรรณานุกรม

ภาษาไทย

นเรศร์ จันทน์ขาว. เอกสารประกอบการสอนการถ่ายภาพด้วยรังสีเอ็กซ์และรังสีแกมมาในงานอุตสาหกรรม. ภาควิชานิวเคลียร์เทคโนโลยี คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย, 2540.

ภาษาอังกฤษ

1. Bernard Grob. Basic Television Principles and Servicing. (n.p.): McGraw-Hill, 1975.
2. Alan V. Oppenheim and Ronald W. Schafer. Discrete-Time Signal Processing. (n.p.): Prentice-Hall International, 1989.
3. Maher A. Sid-Ahmed. Image Processing Theory, Algorithms, and Architectures. (n.p.): Magraw-Hill, 1995.
4. Rulph Chassaing. Digital Signal Processing Laboratory Experiments Using C and the TMS320C31 DSK. (n.p.): John wiley & sons, 1999.
5. Rafael C. Gonzales and Richad E. Wood. Digital Image Processing. (n.p.): Addison-Wesley Publishing Company, 1993.
6. T. W. Parks and C. S. Burrus. Digital Filter Design. (n.p.): John wiley & son, 1987.
7. TMS320C3X C Source Debugger User's Guide. Texas. Texas Instruments, 1993.
8. TMS320C3X/C4X Optimizing C Complier User's Guide. Texas. Texas Instrument, 1998.
9. Digital Signal Processing Application with the TMS320 family. Texas. Texas Instrument, 1986.

ภาคผนวก

ภาคผนวก ก

ลักษณะสัญญาณของ TMS320C31

ในตารางที่ 1 จะอธิบายสัญญาณของ TMS320C31 ที่ใช้ในโหมดไมโครโปรเซสเซอร์

ตารางที่ 1 แสดงตำแหน่งขาและหน้าที่การทำงานของแต่ละขา

Primary Bus Interfoce (61 pins)		
ชื่อ	จำนวนขา	คำอธิบาย
$D_0 - D_{31}$	32	พอร์ตข้อมูล 32 บิต
$A_0 - A_{23}$	24	พอร์ตแอดเดรส 24 บิต
$\overline{HOLD}$	1	เมื่อ $\overline{HOLD}$ เป็นลอจิกต่ำจะทำให้สัญญาณ A_0–A_{23},D_0–D_{31}, $\overline{STRB}$ และ R / $\overline{W}$ จะมีสภาพเป็น high – impedance และการติดต่อทั้งหมดที่อยู่บนบัสอินเตอร์เฟสจะถูกดีเลย์ไว้จนกระทั่งมีสัญญาณ $\overline{HOLD}$ อีกครั้งเป็นลอจิกสูงหรือจนกระทั่งบิต $\overline{NOHOLD}$ ของคอนโทรลบิตรีจิสเตอร์ primary bus ถูกเซ็ต
$\overline{HOLDA}$	1	สัญญาณแสดงการเริ่มต้นหรือสิ้นสุดของสัญญาณ $\overline{HOLD}$ คือสัญญาณ $\overline{HOLDA}$ จะการตอบสนองการทำงานของลอจิกต่ำของสัญญาณ $\overline{HOLD}$ เมื่อ $\overline{HOLDA}$ เป็นลอจิกต่ำจะทำให้สัญญาณ $A_0 - A_{23}$, $D_0 - D_{31}$, STRB และ R / $\overline{W}$ มีสภาวะเป็น high – impedance และการติดต่อทั้งหมดที่อยู่บนบัสจะถูกดีเลย์ไว้จนกระทั่งสัญญาณ $\overline{HOLDA}$ ตอบสนองสภาวะสูงจากลอจิกของ $\overline{HOLD}$ หรือจนกระทั่งบิท $\overline{NOHOLD}$ ของคอนโทรลรีจิสเตอร์ primary bus ถูกเซ็ต

ชื่อ	จำนวนขา	คำอธิบาย
R / $\overline{W}$	1	สัญญาณ Read / Write จะเป็นสภาวะสูงเมื่อมีการอ่านและจะเป็นสภาวะต่ำเมื่อมีการเขียนบนอินเตอร์เฟสแบบขนาน
$\overline{RDY}$	1	สัญญาณ Ready ขานี้จะทำงานก็ต่อเมื่ออุปกรณ์ภายนอกทำการติดต่อกับชิป
$\overline{STRB}$	1	สัญญาณ strobe จากภายนอก
Control – Signal (10 pins)		
$\overline{INT3}$ - $\overline{INT0}$	4	อินเตอร์เฟสภายนอก
$\overline{IACK}$	1	สัญญาณแสดงการเริ่มต้นหรือ สิ้นสุดของสัญญาณอินเตอร์รัพพ์ โดยปกติ $\overline{IACK}$ จะถูกเซ็ตให้เป็น 1 เพราะฉะนั้น $\overline{IACK}$ จึงแสดงการเริ่มต้น หรือจุดสิ้นสุดของการใช้อินเตอร์รัพพ์รูทีน
MCBL / $\overline{MP}$	1	สัญญาณกำหนดการทำงานระหว่าง Microcomputer boot loader กับ Microprocessor
$\overline{RESET}$	1	สัญญาณ Reset เมื่อสัญญาณ reset เป็นลอจิกต่ำจะยกเลิกการทำงานภายใต้เงื่อนไขที่กำหนดให้
$\overline{SH2}$	1	สัญญาณ shut down high Z เมื่อมีสภาวะต่ำจะยกเลิกการทำงานของ C31 และขาทั้งหมดจะมีสภาวะเป็น high – impedance สัญญาณนี้ใช้ทดสอบ broadlevel นั้นคือจะไม่ปรากฏสภาวะอื่น <u>ข้อควรระวัง</u> เมื่อ $\overline{SH2}$ มีสภาวะต่ำจะทำให้ข้อมูลที่อยู่ภายในหน่วยความจำและรีจิสเตอร์หายไป การรีเซ็ตด้วย $\overline{SH2}$ = 1 เป็นการคืนค่าในสภาวะของการทำงาน
XF0 , XF1	2	สัญญาณ Flag ภายนอกโดยทั่วไปใช้เป็นขา I / O หรือสนันสนุนการทำงานของ Interlocked processor instructions

Serial Port O Signals (6 pins)		
CLK R0 , CLK X0	2	สัญญาณนาฬิกา ที่ใช้สำหรับควบคุมการรับ – ส่งข้อมูลของ serial port 0 receiver และ serial port 0 transmitter
DR0	1	ใช้สำหรับรับข้อมูลจาก serial port 0 receives
DX0	1	ใช้สำหรับส่งข้อมูลจาก serial port 0 transmits
FSR0	1	FRS 0 จะเริ่มต้นนับเมื่อมีการรับข้อมูลบน DR 0
FSX0	1	FRS 0 จะเริ่มต้นนับเมื่อมีการส่งข้อมูลบน DX 0
Timer Signals (2 pins)		
TCLK0	1	Timer 0 จะใช้ขา TCLK 0 ในการนับพลัสจากภายนอก หรือกำเนิดสัญญาณพลัสออกสู่ภายนอก
TCLK1	1	Timer 1 จะใช้ขา TCLK 0 ในการนับพลัสจากภายนอกหรือกำเนิดสัญญาณพลัสออกสู่ภายนอก
Supply and Ocillator Signals (49 pins)		
H1 , H3	2	สัญญาณนาฬิกาภายนอก สัญญาณนาฬิกาจะมีคาบเท่ากับ 2 เท่าของ CLKIN
V_{DD}	20	จ่ายไฟให้ได้ไม่เกิน +5 Vdc
V_{SS}	25	ใช้สำหรับต่อกราวด์
X_1	1	เป็นขา output จากตัวคริสตัลภายในที่จะส่งออกภายนอก ถ้าไม่ใช้คริสตัลขานี้ไม่ต้องต่อ
X_2 / CLKIN	1	เป็นขา input สำหรับสัญญาณนาฬิกาหรือคริสตัลจากภายนอกที่จะส่งเข้าไปภายในชิบ
Reserved (4 pins)		
EMU0 – EMU2	3	ขอสงวนไว้ : ใช้ตัวต้านทาน 20 KΩ ต่อ pull – up กับไฟ +5 Vdc
EMU3	1	ขอสงวนไว้

ภาคผนวก ข

โปรแกรมการประมวลผลภาพโดยตัวประมวลสัญญาณ TMS320C31

```
#include "h:\dsp\c3x_lab\ch3\aiccomc.c"
#include "h:\dsp\c3xtools\math.h"
int AICSEC[4] = {0x162c,0x1,0x4892,0x67};
volatile char *Time1=(volatile char *) 0x300000;
volatile char *Time2=(volatile char *) 0x900000;
void frame(void);
void main(void)
{
   unsigned char a1,a2,a3,a4;
   unsigned int  dataRAM1,i;
    volatile char *RAM2=(volatile char *) 0x100000;
    volatile int  *DUAL=(volatile int *) 0x200000;
    for(i=0;i<=0x7FFF;i++)
    {
       dataRAM1 = *DUAL++;
       a1 = (dataRAM1 & 0x000000ff);
       a2 = (dataRAM1 & 0x0000ff00) / 0x000000ff;
       a3 = (dataRAM1 & 0x00ff0000) / 0x0000ffff;
       a4 = (dataRAM1 & 0xff000000) / 0x00ffffff;
       *RAM2++ = a3;
       *RAM2++ = a4;
       *RAM2++ = a1;
       *RAM2++ = a2;
    }
      frame();
}
void frame(void)
```

```
{
 volatile char *RAM2=(volatile char *) 0x100000;
 volatile char *RAM3=(volatile char *) 0x700000;
 int i,j;
 unsigned char m,n;
 char rst1,rst2,rst3,rst4,rst5,rst6,rst7,rst8;
 unsigned char dataRAM2,r1,r2,r3,r4,r5,r6,r7,r8,r9;
 char rst;
 unsigned char b=0;
 for(i=0;i<=65500;i++)
  *Time1 = 0x00000000;
 for (j=1;j<=254;j++)
 {
   for (i=1;i<=254;i++)
   {
        r1 = *(RAM2 + 254*(j-1) + i-1);
        r2 = *(RAM2 + 254*(j-1) + i);
        r3 = *(RAM2 + 254*(j-1) + i+1);
        r4 = *(RAM2 + 254*j   + i-1);
        r5 = *(RAM2 + 254*j   + i);
        r6 = *(RAM2 + 254*j   + i+1);
        r7 = *(RAM2 + 254*(j+1) + i-1);
        r8 = *(RAM2 + 254*(j+1) + i);
        r9 = *(RAM2 + 254*(j+1) + i+1);
         rst1 =  r1   + r2*2 + r3   - r7   - r8*2 - r9;
         rst2 =  r1*2 + r2   + r4   - r6   - r8   - r9*2;
         rst3 =  r1   - r3   + r4*2 - r6*2 + r7   - r9;
         rst4 = -r2   - r3*2 + r4   - r6   - r7*2 + r8*2;
         rst5 = -r1   - r2*2 - r3   + r7   + r8*2 + r9;
         rst6 = -r1*2 - r2   - r4   + r6   + r8   + r9*2;
         rst7 = -r1   + r3   - r4*2 + r6*2 - r7   + r9;
```

```
            rst8 =  r2   + r3*2 - r4   + r6   - r7*2 + r8;
           rst = rst1;
          if(rst2>rst) rst = rst2;
          if(rst3>rst) rst = rst3;
          if(rst4>rst) rst = rst4;
          if(rst5>rst) rst = rst5;
          if(rst6>rst) rst = rst6;
          if(rst7>rst) rst = rst7;
          if(rst8>rst) rst = rst8;
          b++;
      }
   }
    for(i=0;i<=65500;i++)
    *Time2 = 0x00000000;
}
void frame1(void)       //highpass
{
   volatile char *RAM2=(volatile char *) 0x100000;
   volatile char *RAM3=(volatile char *) 0x700000;
   int i,j,m,n;
   float kn1[3][3] = {-0.25,-0.25,-0.25, -0.25,3,-0.25, -0.25,-0.25,-0.25};   // gx
   float kn2[3][3] = {-1,-1,-1, -1,9,-1, -1,-1,-1};   // gy
   float kn3[3][3] = {0,-1,0, -1,5,-1, 0,-1,0};   // gx
   FILE *ftest3;
   float rst,rst1,rst2,rst3,rst4,rt1,rt2,rt3,rt4,rt5,rt6,rst5,rst6,rst7,rst8;
   ftest3=fopen("c:\\tc\\dsk30\\edge.txt","wb");
   for (j=1;j<=121;j++)
   {
      for (i=1;i<=266;i++)
      {
            rst = 0;     rst1 = 0; rst2 = 0; rst3 = 0; rst4 = 0;
```

```
        rst5 = 0; rst6 = 0; rst7 = 0; rst8 = 0;
        for (n=0;n<=2;n++)
         for (m=0;m<=2;m++)
         {
            rst1 += ling[i-1+m][j-1+n]*kn1[m][n];
            rst2 += ling[i-1+m][j-1+n]*kn2[m][n];
            rst3 += ling[i-1+m][j-1+n]*kn3[m][n];
         }
        rt1 = (rst1>rst2)?rst1:rst2;
        rst = (rt1>rst3)?rt1:rst3;
        if (rst > 255) rst = 255;
        if (rst < 0  ) rst = 0;
        *RAM2++ = rst*0x01000000 + rst*0x00010000 + rst*0x00000100 + rst;
    }
  }
}
```

โปรแกรมแสดงผลทางคอมพิวเตอร์

```
#include "dsklib.h"
#include "io.h"
#include <math.h>
#include <graphics.h>
#ifndef _DAC256_
#define _DAC256_
typedef unsigned char DacPalette256[256][3];
#endif
extern int far _Cdecl Svga256_fdriver[];
/* These are the currently supported modes */
#ifndef SVGA320x200x256
#define SVGA320x200x256          0      /* 320x200x256 Standard VGA */
#define SVGA640x400x256          1      /* 640x400x256 Svga/VESA */
#define SVGA640x480x256          2      /* 640x480x256 Svga/VESA */
#define SVGA800x600x256          3      /* 800x600x256 Svga/VESA */
#define SVGA1024x768x256  4      /* 1024x768x256 Svga/VESA */
#define SVGA640x350x256          5      /* 640x350x256 Svga */
#define SVGA1280x1024x256 6      /* 1280x1024x256 VESA */
#endif
#ifndef XNOR_PUT
#define XNOR_PUT    5
#define NOR_PUT          6
#define NAND_PUT    7
#define TRANS_COPY_PUT    8
#endif
char name[20];
unsigned char ling[270][130];
void frame1(void);
void frame2(void);
```

```
void main()
{
  int sel,i,j,m,x1,y1;
  int Gd=DETECT,Gm;
  int xasp,yasp;
  unsigned int ch;
  unsigned char mm,aa;
  FILE *fptrc,*ftest;
  DacPalette256 a,b;
  clrscr();
  printf("[þ]ÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍ Frame Grabber ÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍÍ[þ]\n");
  printf("   SAVE OR OPEN (1 or 2)n");
  sel = getch();
  printf("   File Name : ");
  gets(name);
  installuserdriver("Svga256",DetectVGA256);
  initgraph(&Gd,&Gm,"");
  getvgapalette256(&b);
  fptrc=fopen("C:\\TC\\DSK30\\bwpal.dat","rb");
  for(i=0;i<256;i++)
   {
  a[i][0]=(char)getc(fptrc);
  a[i][1]=(char)getc(fptrc);
  a[i][2]=(char)getc(fptrc);
  }
 fclose(fptrc);
 setvgapalette256(&a);
 getaspectratio(&xasp,&yasp);
 setaspectratio(xasp,yasp);
  Detect_Windows();
  Init_Communication(10000);
```

```
   HALT_CPU();    // Put C31 into spin0 mode
   for (i=0;i<=269;i++)
   for (j=0;j<=129;j++)
    ling[i][j] = 255;
                              do {
                               if(sel=='1')   testpattern(0x200200L,8192, 0x00000000L,11);
                               if(sel=='2')      readpattern(0x200000L,8192, 0x00000000L,11);
                               m=kbhit();
                              } while (m == 0);
     for (i=0;i<=267;i++)
   {
    for (j=0;j<=122;j++)
     putpixel(i+11,j+5,ling[i][j]);
   }
   getch();
   frame1();
   getch();
   frame2();
   getch();
   setvgapalette256(&b);
   graphdefaults();
   closegraph();
}
}
```

ภาคผนวก ค

Data Sheet

intersil

CA3318

August 2000

CMOS Video Speed, 8-Bit, Flash A/D Converter

Features

- CMOS Low Power with SOS Speed (Typ)..... 150mW
- Parallel Conversion Technique
- 15MHz Sampling Rate (Conversion Time).....67ns
- 8-Bit Latched Three-State Output with Overflow Bit
- Accuracy (Typ)..... ±1 LSB
- Single Supply Voltage..... 4V to 7.5V
- 2 Units in Series Allow 9-Bit Output
- 2 Units in Parallel Allow 30MHz Sampling Rate

Applications

- TV Video Digitizing (Industrial/Security/Broadcast)
- High Speed A/D Conversion
- Ultrasound Signature Analysis
- Transient Signal Analysis
- High Energy Physics Research
- General-Purpose Hybrid ADCs
- Optical Character Recognition
- Radar Pulse Analysis
- Motion Signature Analysis
- µP Data Acquisition Systems

Description

The CA3318 is a CMOS parallel (FLASH) analog-to-digital converter designed for applications demanding both low power consumption and high speed digitization.

The CA3318 operates over a wide full scale input voltage range of 4V up to 7.5V with maximum power consumption depending upon the clock frequency selected. When operated from a 5V supply at a clock frequency of 15MHz, the typical power consumption of the CA3318 is 150mW.

The intrinsic high conversion rate makes the CA3318 ideally suited for digitizing high speed signals. The overflow bit makes possible the connection of two or more CA3318s in series to increase the resolution of the conversion system. A series connection of two CA3318s may be used to produce a 9-bit high speed converter. Operation of two CA3318s in parallel doubles the conversion speed (i.e., increases the sampling rate from 15MHz to 30MHz).

256 paralleled auto balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel bit outputs in the CA3318.

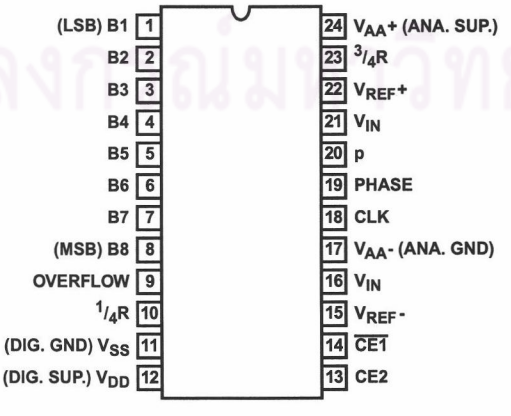
255 comparators are required to quantize all input voltage levels in this 8-bit converter, and the additional comparator is required for the overflow bit.

Part Number Information

PART NUMBER	LINEARITY (INL, DNL)	SAMPLING RATE	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CA3318CE	±1.5 LSB	15MHz (67ns)	-40 to 85	24 Ld PDIP	E24.6
CA3318CM	±1.5 LSB	15MHz (67ns)	-40 to 85	24 Ld SOIC	M24.3
CA3318CD	±1.5 LSB	15MHz (67ns)	-40 to 85	24 Ld SBDIP	D24.6

Pinout

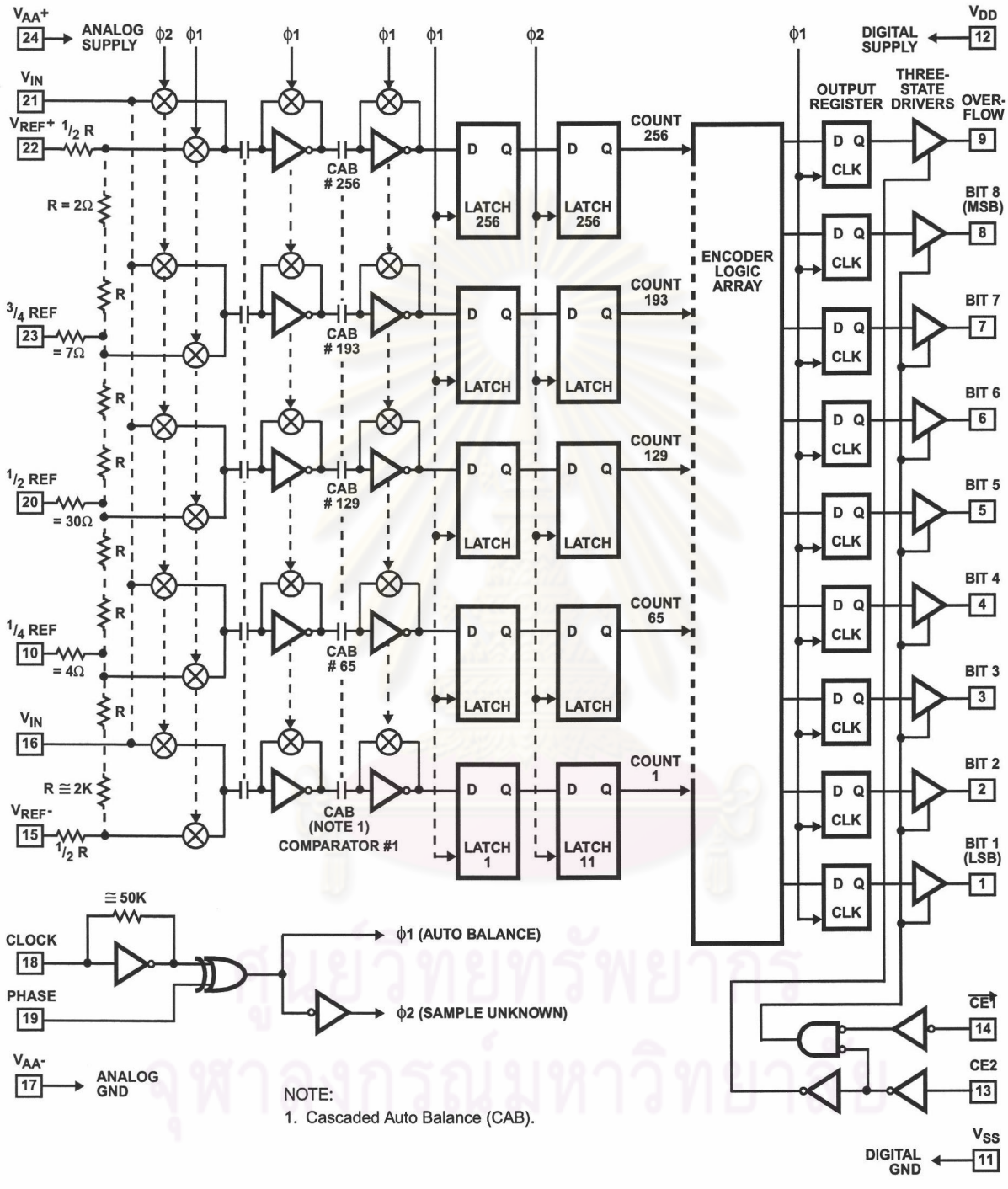
CA3318
(PDIP, SBDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

File Number **3103.2**

Functional Block Diagram



NOTE:
1. Cascaded Auto Balance (CAB).

Absolute Maximum Ratings

DC Supply Voltage Range (V_{DD} or V_{AA}+) . . . . . -0.5V to +8V
(Referenced to V_{SS} or V_{AA}- Terminal, Whichever is More Negative)
Input Voltage Range
CE2 and $\overline{CE1}$ . . . . . V_{AA}- -0.5V to V_{DD} + 0.5V
Clock, Phase, V_{REF}-, $^1/_2$ Ref. . . . . V_{AA}- -0.5V to V_{AA}+ + 0.5V
Clock, Phase, V_{REF}-, $^1/_4$ Ref. . . . . V_{SS}- -0.5V to V_{DD} + 0.5V
V_{IN}, $^3/_4$ REF, V_{REF}+ . . . . . V_{AA}- -0.5V to V_{AA}- + 7.5V
Output Voltage Range, ... V_{SS} - 0.5V to V_{DD} + 0.5V
Bits 1-8, Overflow (Outputs Off)
DC Input Current . . . . . ±20mA
Clock, Phase, $\overline{CE1}$, CE2, V_{IN}, Bits 1-8, Overflow

Operating Conditions

Operating Voltage Range (V_{DD} or V_{AA}+) . . . 4V (Min) to 7.5V (Max)
Recommended V_{AA}+ Operating Range . . . . . V_{DD} ±1V
Recommended V_{AA}- Operating Range . . . . . V_{SS} ±1V
Operating Temperature Range (T_A) . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SBDIP Package	60	22
PDIP Package	60	N/A
SOIC Package	75	N/A

Maximum Junction Temperature
Ceramic Package . . . . . 175°C
Plastic Packages . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 265°C
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

At 25°C, V_{AA}+ = V_{DD} = 5V, V_{REF}+ = 6.4V, V_{REF}- = V_{AA}- = V_{SS}, CLK = 15MHz, All Reference Points Adjusted, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Resolution		8	-	-	Bits
Integral Linearity Error		-	-	±1.5	LSB
Differential Linearity Error		-	-	+1, -0.8	LSB
Offset Error, Unadjusted	V_{IN} = V_{REF}- + $^1/_2$ LSB	-0.5	4.5	6.4	LSB
Gain Error Unadjusted	V_{IN} = V_{REF}+ - $^1/_2$ LSB	-1.5	0	1.5	LSB
DYNAMIC CHARACTERISTICS					
Maximum Input Bandwidth	(Note 1) CA3318	2.5	5.0	-	MHz
Maximum Conversion Speed	CLK = Square Wave	15	17	-	MSPS
Signal to Noise Ratio (SNR)	f_S = 15MHz, f_{IN} = 100kHz	-	47	-	dB
$=\frac{RMS\,Signal}{RMS\,Noise}$	f_S = 15MHz, f_{IN} = 4MHz	-	43	-	dB
Signal to Noise Ratio (SINAD)	f_S = 15MHz, f_{IN} = 100kHz	-	45	-	dB
$=\frac{RMS\,Signal}{RMS\,Noise+Distortion}$	f_S = 15MHz, f_{IN} = 4MHz	-	35	-	dB
Total Harmonic Distortion, THD	f_S = 15MHz, f_{IN} = 100kHz	-	-46	-	dBc
	f_S = 15MHz, f_{IN} = 4MHz	-	-36	-	dBc
Effective Number of Bits (ENOB)	f_S = 15MHz, f_{IN} = 100kHz	-	7.2	-	Bits
	f_S = 15MHz, f_{IN} = 4MHz	-	5.5	-	Bits
Differential Gain Error	Unadjusted	-	2	-	%
Differential Phase Error	Unadjusted	-	1	-	%
ANALOG INPUTS					
Full Scale Range, V_{IN} and (V_{REF}+) - (V_{REF}-)	Notes 2, 4	4	-	7	V
Input Capacitance, V_{IN}		-	30	-	pF
Input Current, V_{IN}, (See Text)	V_{IN} = 5V, V_{REF}+ = 5V	-	-	3.5	mA
REFERENCE INPUTS					
Ladder Impedance		270	500	800	Ω

Electrical Specifications At 25°C, $V_{AA}+ = V_{DD} = 5V$, $V_{REF}+ = 6.4V$, $V_{REF}- = V_{AA}- = V_{SS}$, CLK = 15MHz, All Reference Points Adjusted, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS					
Low Level Input Voltage, V_{OL}					
$\overline{CE1}$, CE2	Note 4	-	-	$0.2V_{DD}$	V
Phase, CLK	Note 4	-	-	$0.2V_{AA}$	V
High Level Input Voltage, V_{IN}					
$\overline{CE1}$, CE2	Note 4	$0.7V_{DD}$	-	-	V
Phase, CLK	Note 4	$0.7V_{AA}$	-	-	V
Input Leakage Current, I_I (Except CLK Input)	Note 3	-	±0.2	±5	µA
Input Capacitance, C_I		-	3	-	pF
DIGITAL OUTPUTS					
Output Low (Sink) Current	$V_O = 0.4V$	4	10	-	mA
Output High (Source) Current	$V_O = 4.5V$	-4	-6	-	mA
Three-State Output Off-State Leakage Current, I_{OZ}		-	±0.2	±5	µA
Output Capacitance, C_O		-	4	-	pF
TIMING CHARACTERISTICS					
Auto Balance Time (ϕ1)		33	-	∞	ns
Sample Time (ϕ2)	Note 4	25	-	500	ns
Aperture Delay		-	15	-	ns
Aperture Jitter		-	100	-	ps
Data Valid Time, t_D	Note 4	-	50	65	ns
Data Hold Time, t_H	Note 4	25	40	-	ns
Output Enable Time, t_{EN}		-	18	-	ns
Output Disable Time, t_{DIS}		-	18	-	ns
POWER SUPPLY CHARACTERISTICS					
Device Current ($I_{DD} + I_A$) (Excludes I_{REF})	Continuous Conversion (Note 4)	-	30	60	mA
	Auto Balance (ϕ1)	-	30	60	mA

NOTES:

1. A full scale sine wave input of greater than $f_{CLOCK}/2$ or the specified input bandwidth (whichever is less) may cause an erroneous code. The -3dB bandwidth for frequency response purposes is greater than 30MHz.
2. V_{IN} (Full Scale) or $V_{REF}+$ should not exceed $V_{AA}+ + 1.5V$ for accuracy.
3. The clock input is a CMOS inverter with a 50kΩ feedback resistor and may be AC coupled with $1V_{P-P}$ minimum source.
4. Parameter not tested, but guaranteed by design or characterization.

Timing Waveforms

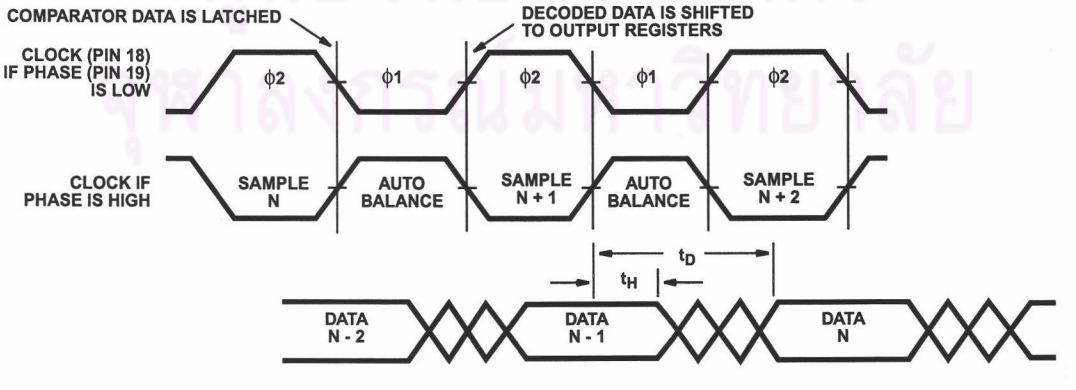


FIGURE 1. INPUT TO OUTPUT TIMING DIAGRAM

Timing Waveforms (Continued)

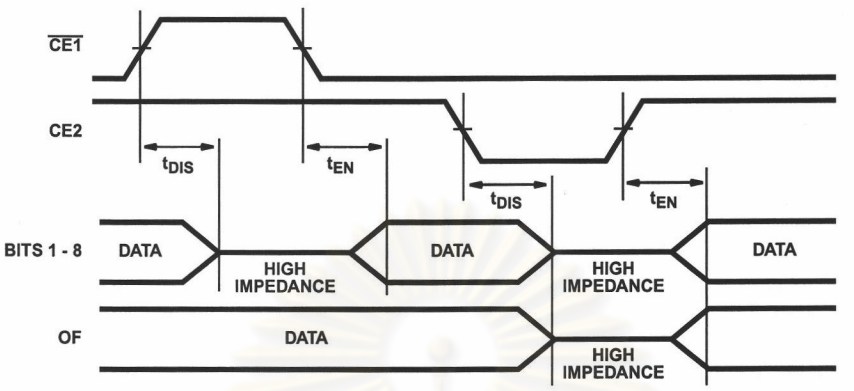


FIGURE 2. OUTPUT ENABLE TIMING DIAGRAM

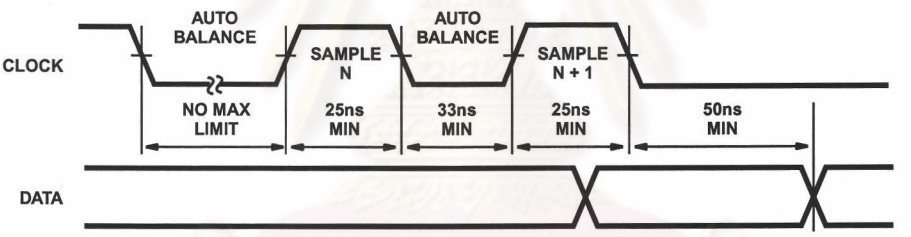


FIGURE 3A. STANDBY IN INDEFINITE AUTO BALANCE (SHOWN WITH PHASE = LOW)

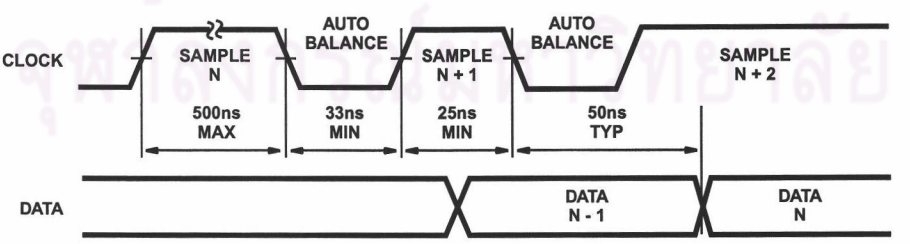


FIGURE 3B. STANDBY IN SAMPLE (SHOWN WITH PHASE = LOW)

FIGURE 3. PULSE MODE OPERATION

Typical Performance Curves

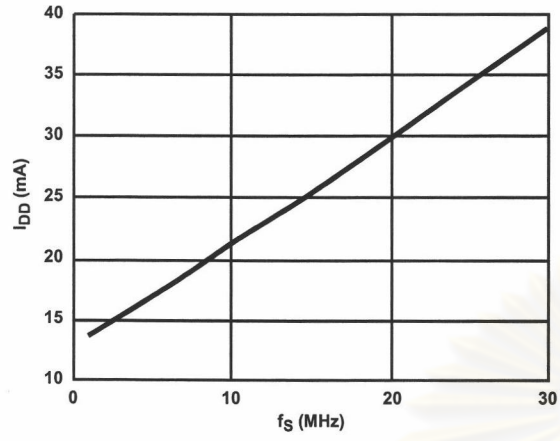


FIGURE 4. DEVICE CURRENT vs SAMPLE FREQUENCY

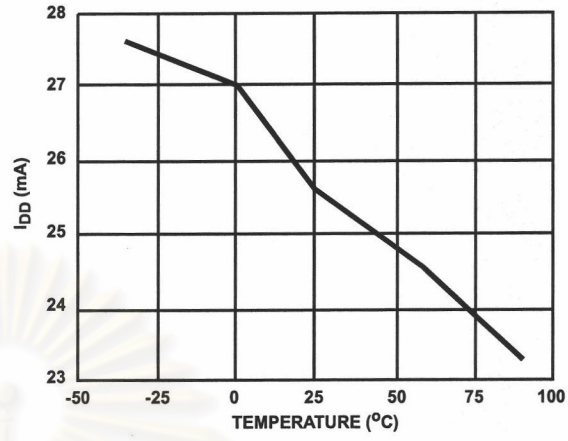


FIGURE 5. DEVICE CURRENT vs TEMPERATURE

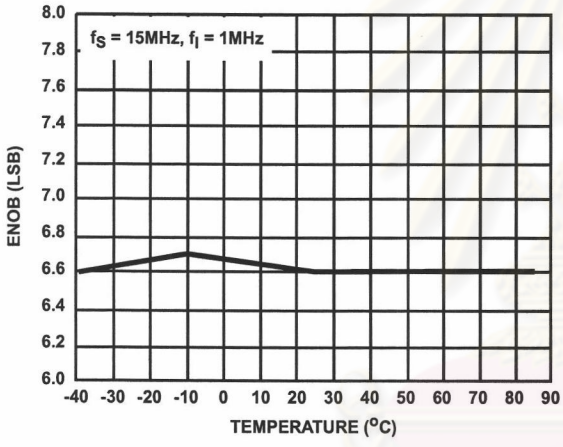


FIGURE 6. ENOB vs TEMPERATURE

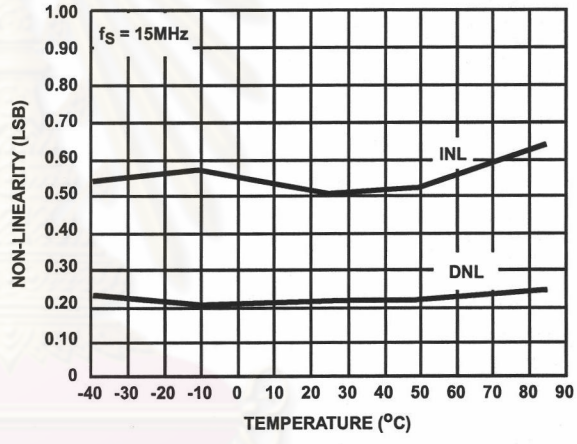


FIGURE 7. NON-LINEARITY vs TEMPERATURE

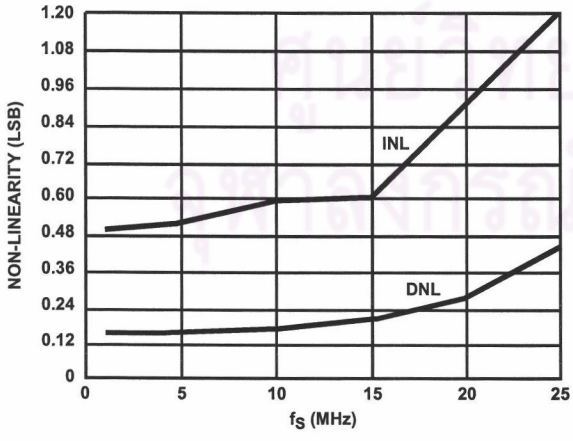


FIGURE 8. NON-LINEARITY vs SAMPLE FREQUENCY

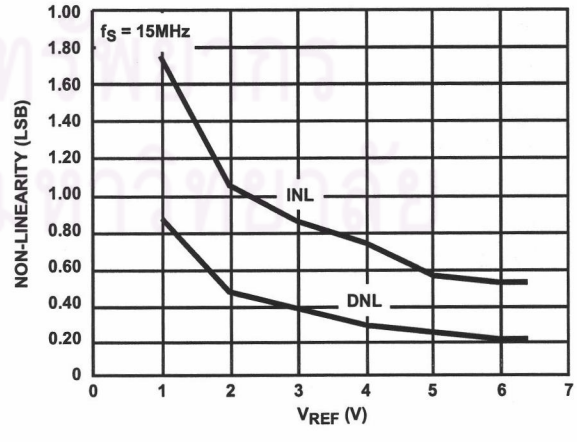


FIGURE 9. NON-LINEARITY vs REFERENCE VOLTAGE

Typical Performance Curves (Continued)

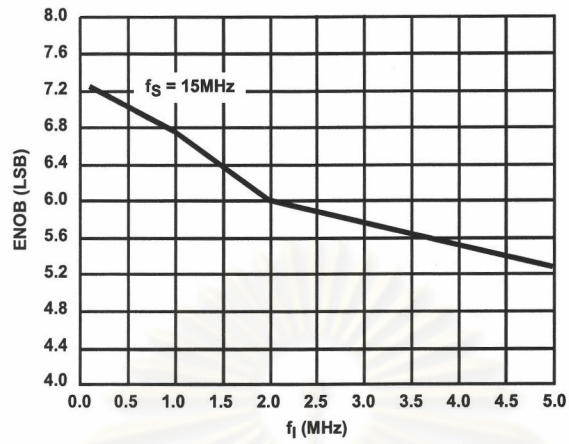


FIGURE 10. ENOB vs INPUT FREQUENCY

Pin Descriptions

PIN	NAME	DESCRIPTION	
1	B1	Bit 1 (LSB)	Output Data Bits (High = True)
2	B2	Bit 2	
3	B3	Bit 3	
4	B4	Bit 4	
5	B5	Bit 5	
6	B6	Bit 6	
7	B7	Bit 7	
8	B8	Bit 8 (MSB)	
9	OF	Overflow	
10	$^1/_4$ R	Reference Ladder $^1/_4$ Point	
11	V_{SS}	Digital Ground	
12	V_{DD}	Digital Power Supply, +5V	
13	CE2	Three-State Output Enable Input, Active Low, See Truth Table.	
14	$\overline{CE1}$	Three-State Output Enable Input Active High. See Truth Table.	
15	V_{REF}-	Reference Voltage Negative Input	
16	V_{IN}	Analog Signal Input	
17	V_{AA}-	Analog Ground	
18	CLK	Clock Input	
19	PHASE	Sample clock phase control input. When PHASE is low, "Sample Unknown" occurs when the clock is low and "Auto Balance" occurs when the clock is high (see text).	
20	$^1/_2$ R	Reference Ladder Midpoint	
21	V_{IN}	Analog Signal Input	
22	V_{REF}+	Reference Voltage Positive Input	
23	$^3/_4$ R	Reference Ladder $^3/_4$ Point	
24	V_{AA}+	Analog Power Supply, +5V	

CHIP ENABLE TRUTH TABLE

$\overline{CE1}$	CE2	B1 - B8	OF
0	1	Valid	Valid
1	1	Three-State	Valid
X	0	Three-State	Three-State

X = Don't Care

Theory of Operation

A sequential parallel technique is used by the CA3318 converter to obtain its high speed operation. The sequence consists of the "Auto-Balance" phase, ϕ1, and the "Sample Unknown" phase, ϕ2. (Refer to the circuit diagram.) Each conversion takes one clock cycle (see Note). With the phase control (pin 19) high, the "Auto-Balance" (ϕ1) occurs during the high period of the clock cycle, and the "Sample Unknown" (ϕ2) occurs during the low period of the clock cycle.

NOTE: The device requires only a single phase clock The terminology of ϕ1 and ϕ2 refers to the high and low periods of the same clock.

During the "Auto-Balance" phase, a transmission switch is used to connect each of the first set of 256 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{TAP}(N) = [(N/256)\,V_{REF}] - (1/512)\,V_{REF}]$$
$$= [(2N - 1)/512]\,V_{REF},$$

Where:

V_{TAP} (n) = reference ladder tap voltage at point n,

V_{REF} = voltage across V_{REF}- to V_{REF}+,

N = tap number (1 through 256).

The other side of these capacitors are connected to single-stage amplifiers whose outputs are shorted to their inputs by switches. This balances the amplifiers at their intrinsic trip points, which is approximately (V_{AA}+ - V_{AA}-)/2. The first set of capacitors now charges to their associated tap voltages.

At the same time a second set of commutating capacitors and amplifiers is also auto-balanced. The balancing of the second-stage amplifier at its intrinsic trip point removes any tracking differences between the first and second amplifier stages. The cascaded auto-balance (CAB) technique, used here, increases comparator sensitivity and temperature tracking.

In the "Sample Unknown" phase, all ladder tap switches and comparator shorting switches are opened. At the same time V_{IN} is switched to the first set of commutating capacitors. Since the other end of the capacitors are now looking into an effectively open circuit, any input voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators that had tap voltages greater than V_{IN} will go to a "high" state at their outputs. All comparators that had tap voltages lower than V_{IN} will go to a "low" state.

The status of all these comparator amplifiers is AC coupled through the second-stage comparator and stored at the end of this phase ($\phi 2$) by a latching amplifier stage. The latch feeds a second latching stage, triggered at the end of $\phi 1$. This delay allows comparators extra settling time. The status of the comparators is decoded by a 256 to 9-bit decoder array, and the results are clocked into a storage register at the end of the next $\phi 2$.

A 3-stage buffer is used at the output of the 9 storage registers which are controlled by two chip-enable signals. $\overline{CE1}$ will independently disable B1 through B6 when it is in a high state. CE2 will independently disable B1 through B8 and the OF buffers when it is in the low state.

To facilitate usage of this device, a phase control input is provided which can effectively complement the clock as it enters the chip.

Continuous-Clock Operation

One complete conversion cycle can be traced through the CA3318 via the following steps. (Refer to timing diagram.) With the phase control in a "low" state, the rising edge of the clock input will start a "sample" phase. During this entire "high" state of the clock, the comparators will track the input voltage and the first-stage latches will track the comparator outputs. At the falling edge of the clock, all 256 comparator outputs are captured by the 256 latches. This ends the "sample" phase and starts the "auto-balance" phase for the comparators. During this "low" state of the clock, the output of the latches settles and is captured by a second row of latches when the clock returns high. The second-stage latch output propagates through the decode array, and a 9-bit code appears at the D inputs of the output registers. On the next falling edge of the clock, this 9-bit code is shifted into the output registers and appears with time delay t_D as valid data at the output of the three-state drivers. This also marks the end of the next "sample" phase, thereby repeating the conversion process for this next cycle.

Pulse-Mode Operation

The CA3318 needs two of the same polarity clock edges to complete a conversion cycle: If, for instance, a negative going clock edge ends sample "N", then data "N" will appear after the next negative going edge. Because of this requirement, and because there is a maximum sample time of 500ns (due to capacitor droop), most pulse or intermittent sample applications will require double clock pulsing.

If an indefinite standby state is desired, standby should be in auto-balance, and the operation would be as in Figure 3A.

If the standby state is known to last less than 500ns and lowest average power is desired, then operation could be as in Figure 3B.

Increased Accuracy

In most cases the accuracy of the CA3318 should be sufficient without any adjustments. In applications where accuracy is of utmost importance, five adjustments can be made to obtain better accuracy, i.e., offset trim; gain trim; and $^1/_4$, $^1/_2$ and $^3/_4$ point trim.

Offset Trim

In general, offset correction can be done in the preamp circuitry by introducing a DC shift to V_{IN} or by the offset trim of the op amp. When this is not possible the V_{REF}- input can be adjusted to produce an offset trim. The theoretical input voltage to produce the first transition is $^1/_2$ LSB. The equation is as follows:

$$V_{IN} \text{ (0 to 1 transition)} = {}^1/_2 \text{ LSB} = {}^1/_2 (V_{REF}/256)$$
$$= V_{REF}/512.$$

If V_{IN} for the first transition is less than the theoretical, then a single-turn 50Ω pot connected between V_{REF}- and ground will accomplish the adjustment. Set V_{IN} to 1/2 LSB and trim the pot until the 0-to-1 transition occurs.

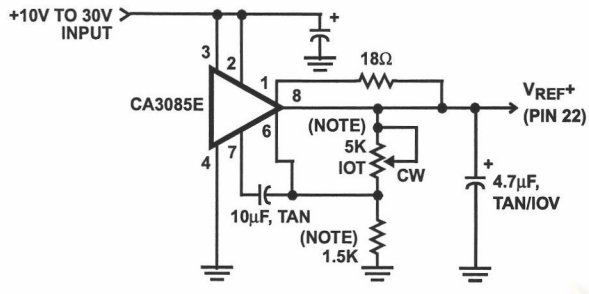
If V_{IN} for the first transition is greater than the theoretical, then the 50Ω pot should be connected between V_{REF}- and a negative voltage of about 2 LSBs. The trim procedure is as stated previously.

Gain Trim

In general, the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the op amp. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V_{IN} should be set to the 255 to overflow transition. That voltage is $^1/_3$ LSB less than V_{REF}+ and is calculated as follows:

$$V_{IN} \text{ (255 to 256 transition)} = V_{REF} - V_{REF}/512$$
$$= V_{REF}(511/512).$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 255 to overflow transition. Now adjust V_{REF}+ until that transition occurs on the outputs.

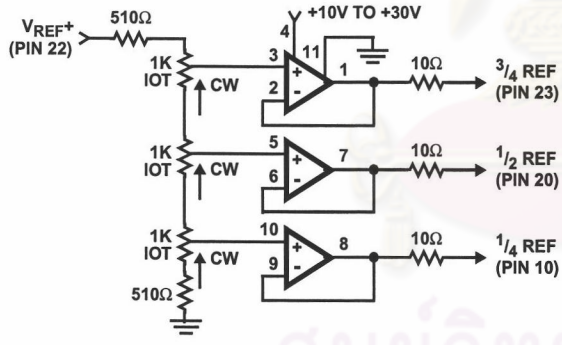


NOTE: Bypass V_{REF}+ to analog GND near A/D with 0.1µF ceramic cap. Parts noted should have low temperature drift.

FIGURE 11. TYPICAL VOLTAGE REFERENCE SOURCE FOR DRIVING V_{REF}+ INPUT

$^1/_4$ Point Trims

The $^1/_4$, $^1/_2$ and $^3/_4$ points on the reference ladder are brought out for linearity adjusting or if the user wishes to create a nonlinear transfer function. The $^1/_4$ points can be driven by the reference drivers shown (Figure 12) or by 2-K pots connected between V_{REF}+ and V_{REF}-. The $^1/_2$ (mid-) point should be set first by applying an input of 257/512 x (V_{REF}) and adjusting for an output changing from 128 to 129. Similarly the $^1/_4$ and $^3/_4$ points can be set with inputs of 129/512 and 385/512 x (V_{REF}) and adjusting for counts of 192 to 193 and 64 to 65. (Note that the points are actually $^1/_4$, $^1/_2$ and $^3/_4$ of full scale +1 LSB.)



NOTES:

1. All Op Amps = $^3/_4$ CA324E.
2. Bypass all reference points to analog ground near A/D with 0.1µF ceramic caps.
3. Adjust V_{REF}+ first, then $^1/_3$, $^3/_4$ and $^1/_4$ points.

FIGURE 12. TYPICAL $^1/_4$ POINT DRIVERS FOR ADJUSTING LINEARITY (USE FOR MAXIMUM LINEARITY)

9-Bit Resolution

To obtain 9-bit resolution, two CA3318s can be wired together. Necessary ingredients include an open-ended ladder network, an overflow indicator, three-state outputs, and chip-enable controls - all of which are available on the CA3318.

The first step for connecting a 9-bit circuit is to totem-pole the ladder networks, as illustrated in Figure 13. Since the absolute resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overflow output of the lower device now becomes the ninth bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overtlow signal to the CE1 control of the lower A/D converter and the CE2 control of the upper A/D converter. The three-state outputs of the two devices (bits 1 through 8) are now connected in parallel to complete the circuitry. The complete circuit for a 9-bit A/D converter is shown in Figure 13.

Grounding/Bypassing

The analog and digital supply grounds of a system should be kept separate and only connected at the A/D. This keeps digital ground noise out of the analog data to be converted. Reference drivers, input amps, reference taps, and the V_{AA} supply should be bypassed at the A/D to the analog side of the ground. See Figure 15 for a block diagram of this concept. All capacitors shown should be low impedance 0.1µF ceramics and should be mounted as close to the A/D as possible. If V_{AA}+ is derived from V_{DD}, a small (10Ω resistor or inductor and additional filtering (4.7µF tantalum) may be used to keep digital noise out of the analog system.

Input Loading

The CA3318 outputs a current pulse to the V_{IN} terminal at the start of every sample period. This is due to capacitor charging and switch feedthrough and varies with input voltage and sampling rate. The signal source must be capable of recovering from the pulse before the end of the sample period to guarantee a valid signal for the A/D to convert. Suitable high speed amplifiers include the HA-5033, HA-2542; and CA3450. Figure 16 is an example of an amplifier which recovers fast enough for sampling at 15MHz.

Output Loading

The CMOS digital output stage, although capable of driving large loads, will reflect these loads into the local ground. It is recommended that a local QMOS buffer such as CD74HC541 E be used to isolate capacitive loads.

Definitions

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the converter. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from fullscale for all these tests.

Signal-to-Noise (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR})/6.02,$$

where: $V_{CORR} = 0.5dB$.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the measured input signal.

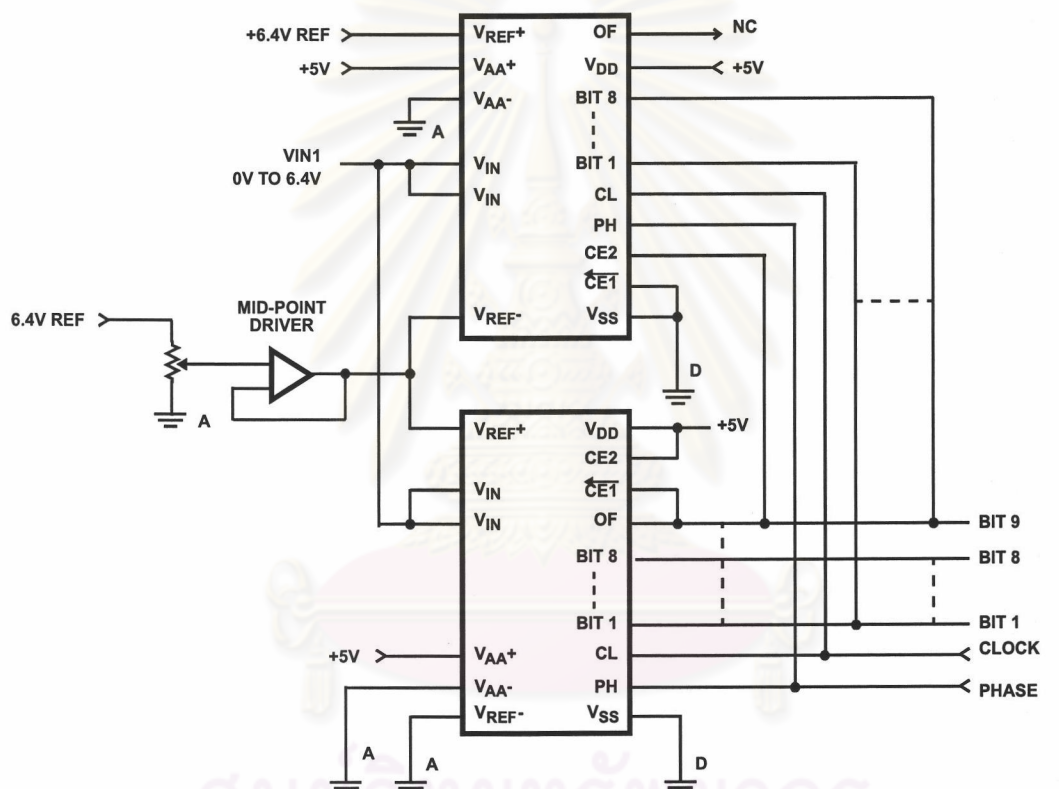


FIGURE 13. USING TWO CA3318s FOR 9-BIT RESOLUTION

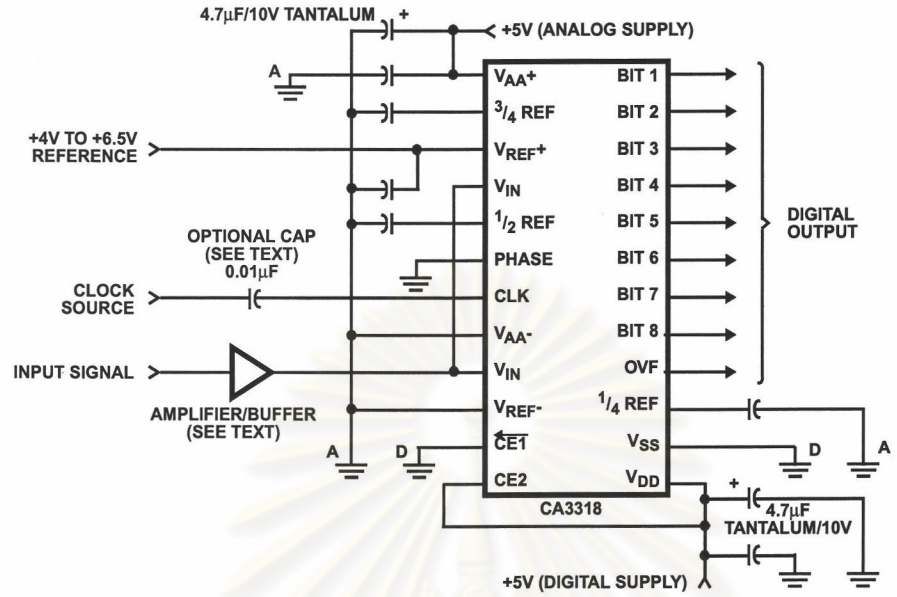


FIGURE 14. TYPICAL CIRCUIT CONFIGURATION FOR THE CA3318 WITH NO LINEARITY ADJUST

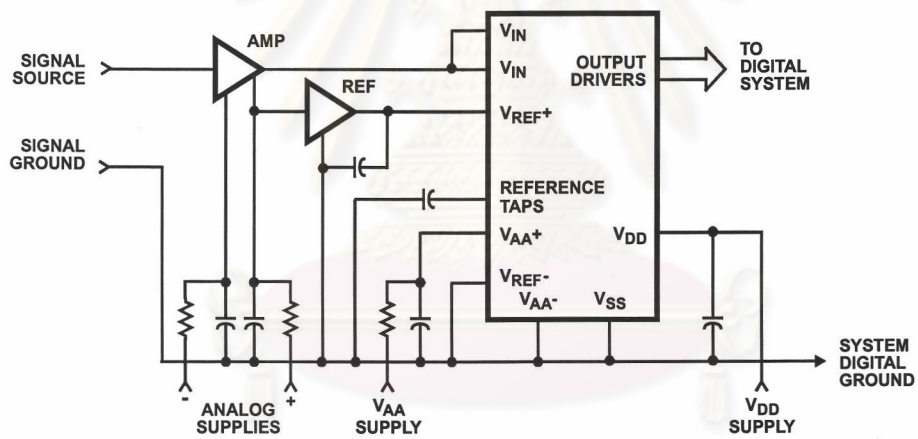
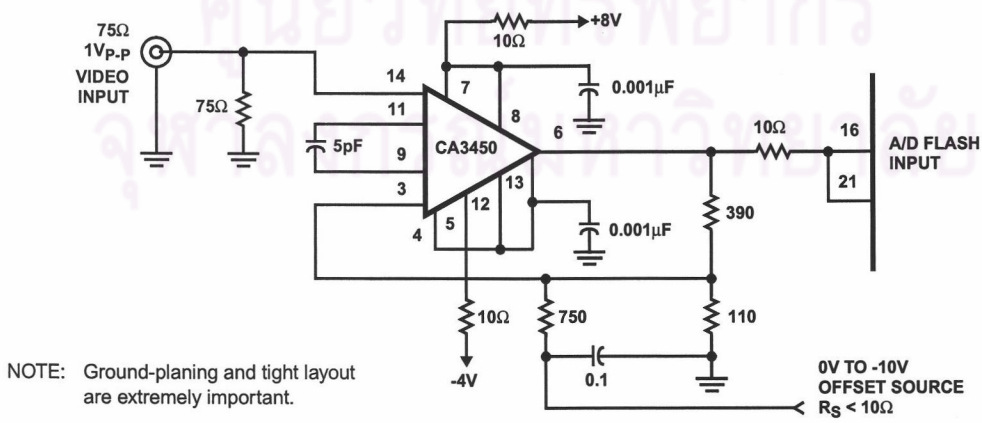


FIGURE 15. TYPICAL SYSTEM GROUNDING/BYPASSING



NOTE: Ground-planing and tight layout are extremely important.

FIGURE 16. TYPICAL HIGH BANDWIDTH AMPLIFIER FOR DRIVING THE CA3318

TABLE 1. OUTPUT CODE TABLE

CODE DESCRIPTION	(NOTE 1) INPUT VOLTAGE		BINARY OUTPUT CODE									DECIMAL COUNT
	V_{REF} 6.40V (V)	V_{REF} 5.12V (V)	OF	MSB B8	B7	B6	B5	B4	B3	B2	LSB B1	
Zero	0.00	0.00	0	0	0	0	0	0	0	0	0	0
1 LSB	0.025	0.02	0	0	0	0	0	0	0	0	1	1
2 LSB	0.05	0.04	0	0	0	0	0	0	0	1	0	2
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
$^1/_4$ Full Scale	1.60	1.28	0	0	1	0	0	0	0	0	0	64
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
$^1/_2$ Full Scale - 1 LSB	3.175	2.54	0	0	1	1	1	1	1	1	1	127
$^1/_2$ Full Scale	3.20	2.56	0	1	0	0	0	0	0	0	0	128
$^1/_2$ Full Scale + 1 LSB	3.225	2.58	0	1	0	0	0	0	0	0	1	129
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
$^3/_4$ Full Scale	4.80	3.84	0	1	1	0	0	0	0	0	0	192
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
Full Scale - 1 LSB	6.35	5.08	0	1	1	1	1	1	1	1	0	254
Full Scale	6.375	5.10	0	1	1	1	1	1	1	1	1	255
Over Flow	6.40	5.12	1	1	1	1	1	1	1	1	1	511

NOTE: 1. The voltages listed above are the ideal centers of each output code shown as a function of its associated reference voltage.

Reducing Power

Most power is consumed while in the auto-balance state. When operating at lower than 15MHz clock speed, power can be reduced by stretching the sample ($\phi 2$) time. The constraints are a minimum balance time ($\phi 1$) of 33ns, and a maximum sample time of 500ns. Longer sample times cause droop in the auto-balance capacitors. Power can also be reduced in the reference string by switching the reference on only during auto-balance.

Clock Input

The Clock and Phase inputs feed buffers referenced to $V_{AA}+$ and $V_{AA}-$. Phase should be tied to one of these two potentials, while the clock (if DC coupled) should be driven at least from 0.2 to 0.7 x ($V_{AA}+$ - $V_{AA}-$). The clock may also be AC coupled with at least a $1V_{P-P}$ swing. This allows TTL drive levels or 5V QMOS levels when $V_{AA}+$ is greater than 5V.

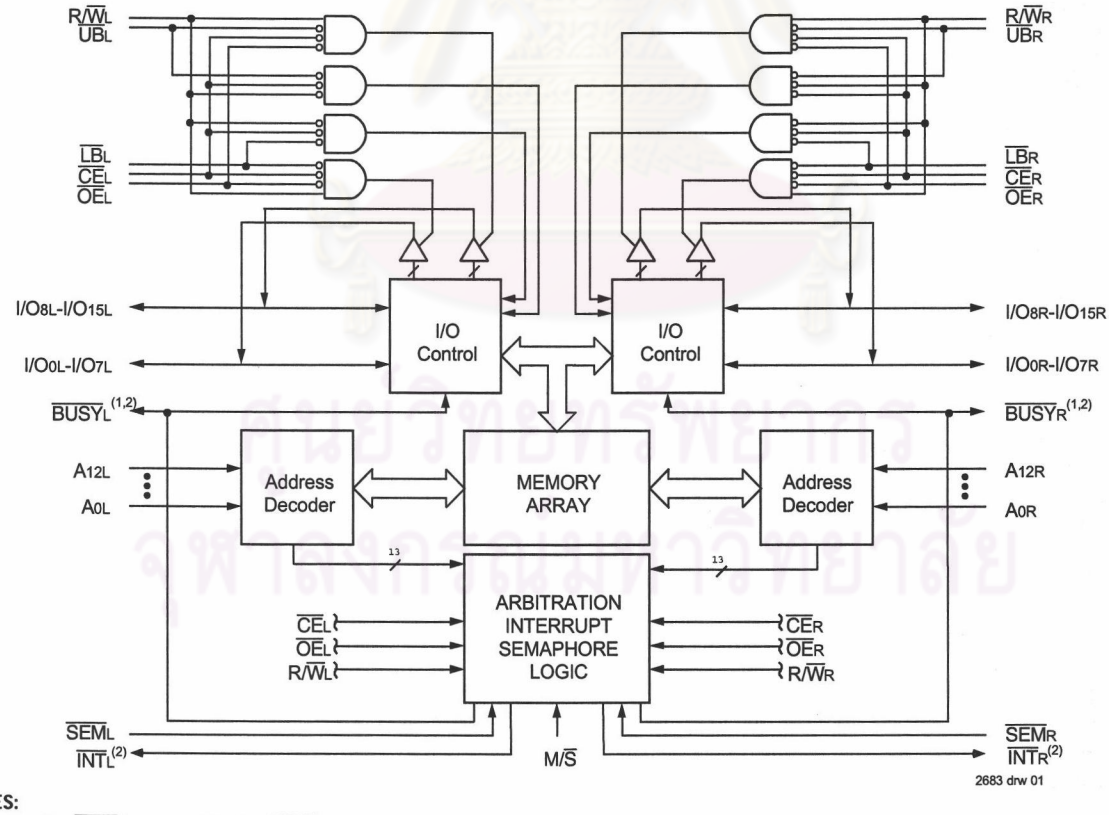
HIGH-SPEED 8K x 16 DUAL-PORT STATIC RAM

IDT7025S/L

Features

- True Dual-Ported memory cells which allow simultaneous reads of the same memory location
- High-speed access
  - *Military: 20/25/35/55/70ns (max.)*
  - *Industrial: 55ns (max.)*
  - *Commercial: 15/17/20/25/35/55ns (max.)*
- Low-power operation
  - *IDT7025S*
    Active: 750mW (typ.)
    Standby: 5mW (typ.)
  - *IDT7025L*
    Active: 750mW (typ.)
    Standby: 1mW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility
- IDT7025 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
- M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- Interrupt Flag
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible, single 5V (±10%) power supply
- Available in 84-pin PGA, Flatpack, PLCC, and 100-pin Thin Quad Flatpack
- Industrial temperature range (–40°C to +85°C) is available for selected speeds

Functional Block Diagram



NOTES:
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. $\overline{BUSY}$ outputs and $\overline{INT}$ outputs are non-tri-stated push-pull.

JANUARY 1999

DSC 2738/6

Description

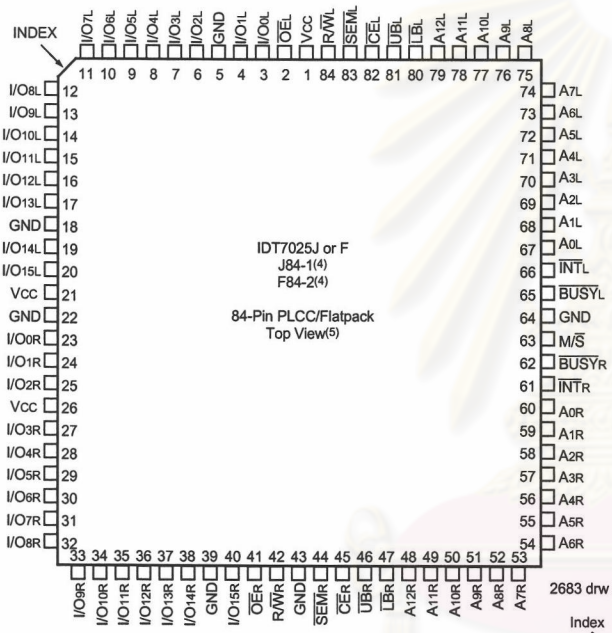
The IDT7025 is a high-speed 8K x 16 Dual-Port Static RAM. The IDT7025 is designed to be used as a stand-alone 128K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit or more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

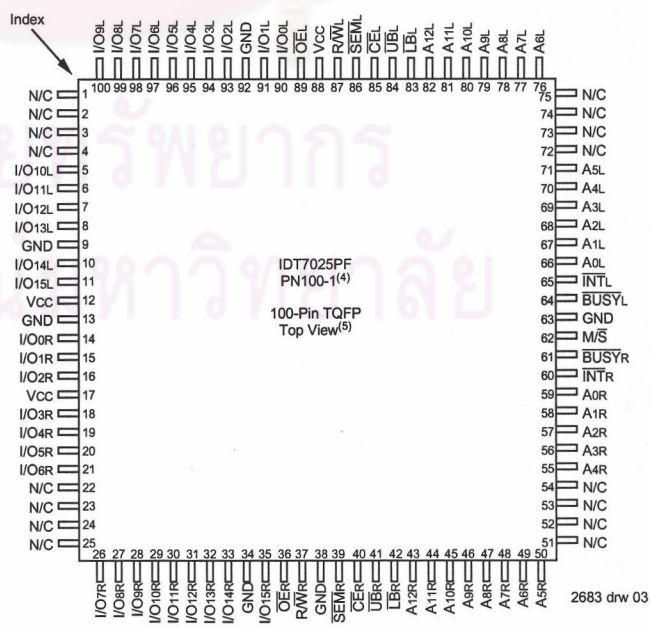
This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by Chip Enable ($\overline{CE}$) permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 750mW of power. Low-power (L) versions offer battery backup data retention capability with typical power consumption of 500µW from a 2V battery.

The IDT7025 is packaged in a ceramic 84-pin PGA, an 84-pin Flatpack, PLCC, and a 100-pin TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Pin Configurations[1,2,3]

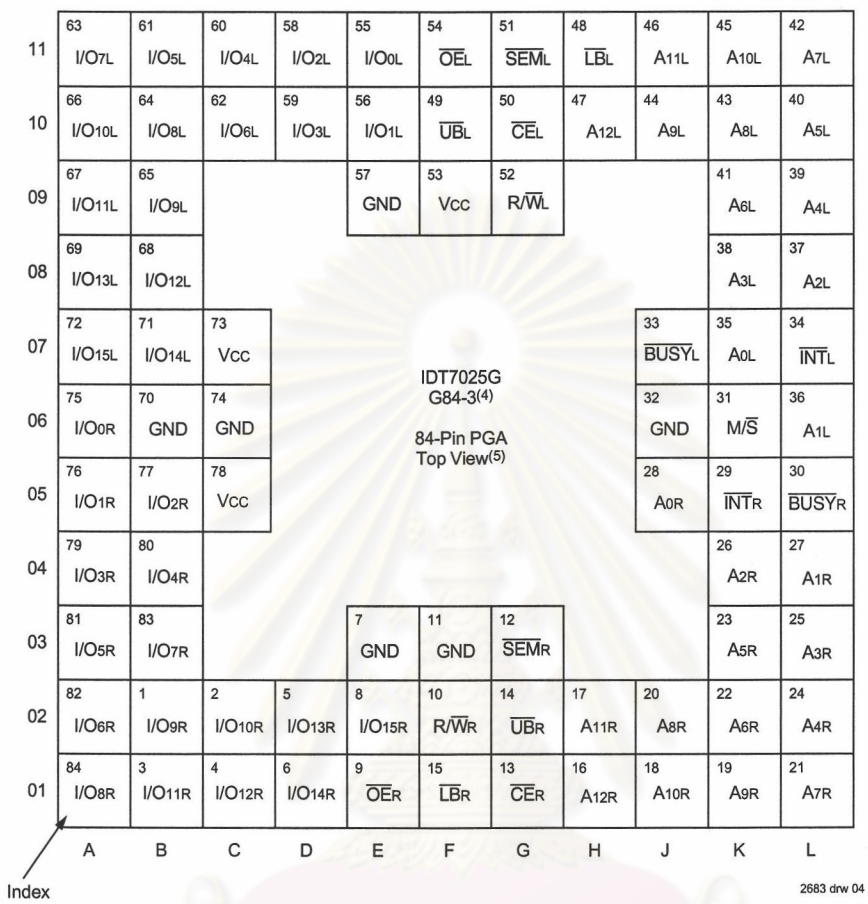




NOTES:

1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. J84-1 package body is approximately 1.15 in x 1.15 in x .17 in.
   F84-2 package body is approximately 1.17 in x 1.17 in x .11 in.
   PN100-1 package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Configurations[1,2,3] (con't.)



NOTES:
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. Package body is approximately 1.12 in x 1.12 in x .16 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L} - A_{12L}	A_{0R} - A_{12R}	Address
I/O_{0L} - I/O_{15L}	I/O_{0R} - I/O_{15R}	Data Input/Output
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
Vcc		Power
GND		Ground

2683 tbl 01

Truth Table I: Non-Contention Read/Write Control

Inputs[1]						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O_{8-15}	I/O_{0-7}	Mode
H	X	X	X	X	H	High-Z	High-Z	Deselected
X	X	X	H	H	H	High-Z	High-Z	Both Bytes Deselected
L	L	X	L	H	H	$DATA_{IN}$	High-Z	Write to Upper Byte Only
L	L	X	H	L	H	High-Z	$DATA_{IN}$	Write to Lower Byte Only
L	L	X	L	L	H	$DATA_{IN}$	$DATA_{IN}$	Write to Both Bytes
L	H	L	L	H	H	$DATA_{OUT}$	High-Z	Read Upper Byte Only
L	H	L	H	L	H	High-Z	$DATA_{OUT}$	Read Lower Byte Only
L	H	L	L	L	H	$DATA_{OUT}$	$DATA_{OUT}$	Read Both Bytes
X	X	H	X	X	X	High-Z	High-Z	Outputs Disabled

2683 tbl 02

NOTE:
1. $A_{0L} - A_{12L} \neq A_{0R} - A_{12R}$.

Truth Table II: Semaphore Read/Write Control[1]

Inputs						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O_{8-15}	I/O_{0-7}	Mode
H	H	L	X	X	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Semaphore Flag Data Out
X	H	L	H	H	L	$DATA_{OUT}$	$DATA_{OUT}$	Read Semaphore Flag Data Out
H	↑	X	X	X	L	$DATA_{IN}$	$DATA_{IN}$	Write I/O_0 into Semaphore Flag
X	↑	X	H	H	L	$DATA_{IN}$	$DATA_{IN}$	Write I/O_0 into Semaphore Flag
L	X	X	L	X	L	—	—	Not Allowed
L	X	X	X	L	L	—	—	Not Allowed

2683 tbl 03

NOTES:
1. There are eight semaphore flags written to via I/O_0 and read from I/O_0 - I/O_{15}. These eight semaphores are addressed by A_0 - A_2.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2683 tbl 04

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20 mA for the period over V_{TERM} ≥ Vcc + 10%.

Capacitance(1) (T_A = +25°C, f = 1.0mhz)

Symbol	Parameter	Conditions(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	10	pF

2683 tbl 07

NOTES:
1. This parameter is determined by device characterization but is not production tested. For TQFP package only.
2. 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

Maximum Operating Temperature and Supply Voltage(1,2)

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

2683 tbl 05

NOTES:
1. This is parameter T_A.
2. Industrial temperature: for other speeds, packages and powers contact your sales office.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2683 tbl 06

NOTES:
1. V_{IL} ≥ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	7025S		7025L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current(1)	Vcc = 5.5V, V_{IN} = 0V to Vcc	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{OUT} = 0V to Vcc	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2683 tbl 08

NOTE:
1. At Vcc ≤ 2.0V input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1,6] (Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7025X15 Com'l Only		7025X17 Com'l Only		7025X20 Com'l & Military		7025X25 Com'l & Military		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	COM'L	S	170	310	170	310	160	290	155	265	mA
				L	170	260	170	260	160	240	155	220	
			MIL & IND	S	—	—	—	—	160	370	155	340	
				L	—	—	—	—	160	320	155	280	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	COM'L	S	20	60	20	60	20	60	16	60	mA
				L	20	50	20	50	20	50	16	50	
			MIL & IND	S	—	—	—	—	20	90	16	80	
				L	—	—	—	—	20	70	16	65	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Open, f=f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L	S	105	190	105	190	95	180	90	170	mA
				L	105	160	105	160	95	150	90	140	
			MIL & IND	S	—	—	—	—	95	240	90	215	
				L	—	—	—	—	95	210	90	180	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ Vcc - 0.2V, V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ Vcc - 0.2V	COM'L	S	1.0	15	1.0	15	1.0	15	1.0	15	mA
				L	0.2	5	0.2	5	0.2	5	0.2	5	
			MIL & IND	S	—	—	—	—	1.0	30	1.0	30	
				L	—	—	—	—	0.2	10	0.2	10	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ Vcc - 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ Vcc - 0.2V V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	COM'L	S	100	170	100	170	90	155	85	145	mA
				L	100	140	100	140	90	130	85	120	
			MIL & IND	S	—	—	—	—	90	225	85	200	
				L	—	—	—	—	90	200	85	170	

2683 tbl 09a

Symbol	Parameter	Test Condition	Version		7025X35 Com'l & Military		7025X55 Com'l, Ind & Military		7025X70 Military Only		Unit
					Typ.[2]	Max.	Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	COM'L	S	150	250	150	250	—	—	mA
				L	150	210	150	210	—	—	
			MIL & IND	S	150	300	150	300	140	300	
				L	150	250	150	250	140	250	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	COM'L	S	13	60	13	60	—	—	mA
				L	13	50	13	50	—	—	
			MIL & IND	S	13	80	13	80	10	80	
				L	13	65	13	65	10	65	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Open, f=f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L	S	85	155	85	155	—	—	mA
				L	85	130	85	130	—	—	
			MIL & IND	S	85	190	85	190	80	190	
				L	85	160	85	160	80	160	
I_{SB3}	Full Standby Current (Both Ports - CMOS Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ Vcc - 0.2V, V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ Vcc - 0.2V	COM'L	S	1.0	15	1.0	15	—	—	mA
				L	0.2	5	0.2	5	—	—	
			MIL & IND	S	1.0	30	1.0	30	1.0	30	
				L	0.2	10	0.2	10	0.2	10	
I_{SB4}	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ Vcc - 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L$ ≥ Vcc - 0.2V V_{IN} ≥ Vcc - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Open, f = f_{MAX}[3]	COM'L	S	80	135	80	135	—	—	mA
				L	80	110	80	110	—	—	
			MIL & IND	S	80	175	80	175	75	175	
				L	80	150	80	150	75	150	

2683 tbl 09b

NOTES:

1. 'X' in part number indicates power rating (S or L)
2. Vcc = 5V, TA = +25°C, and are not production tested. Icc dc = 120mA (TYP)
3. At f = fMAX, address and I/O's are cycling at the maximum frequency read cycle of 1/tRC, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
6. Industrial temperature: for other speeds, packages and powers contact your sales office.

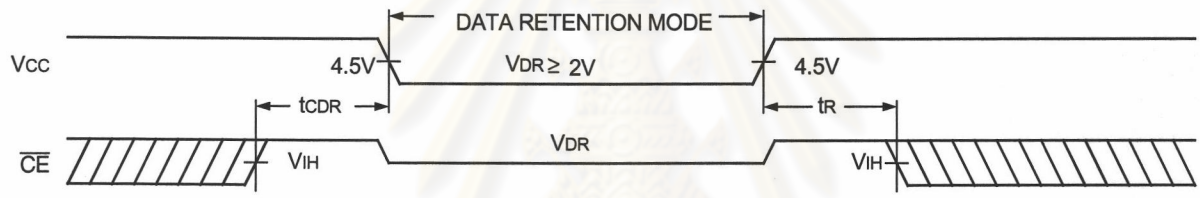
Data Retention Characteristics Over All Temperature Ranges (L Version Only)

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	Vcc for Data Retention	V_{CC} = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL. & IND.	—	100	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	100	1500	
t_{CDR}[3]	Chip Deselect to Data Retention Time	$\overline{SEM} \geq V_{HC}$		0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	V

2683 tbl 10

NOTES:
1. T_A = +25°C, V_{CC} = 2V, and are not production tested.
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed by device characterization, but is not production tested.
4. At $V_{CC} \leq$ 2.0V input leakages are undefined.

Data Retention Waveform



2683 drw 05

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1 and 2

2683 tbl 11

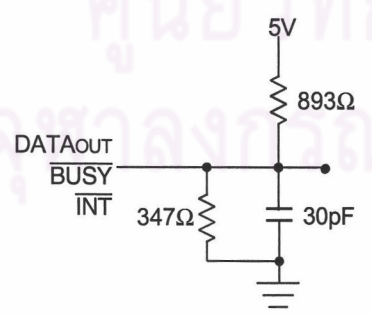
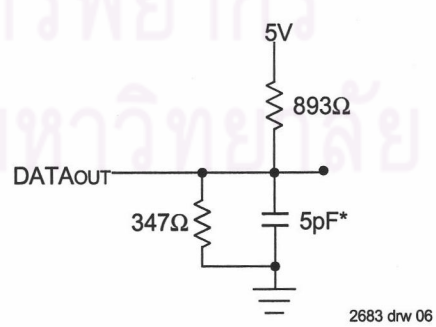


Figure 1. AC Output Test Load



2683 drw 06

Figure 2. Output Test Load (for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
* including scope and jig.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[4,5]

Symbol	Parameter	7025X15 Com'l Only		7025X17 Com'l Only		7025X20 Com'l & Military		7025X25 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE										
t_{RC}	Read Cycle Time	15	—	17	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	15	—	17	—	20	—	25	ns
t_{ACE}	Chip Enable Access Time[3]	—	15	—	17	—	20	—	25	ns
t_{ABE}	Byte Enable Access Time[3]	—	15	—	17	—	20	—	25	ns
t_{AOE}	Output Enable Access Time[3]	—	10	—	10	—	12	—	13	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1,2]	3	—	3	—	3	—	3	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	10	—	10	—	12	—	15	ns
t_{PU}	Chip Enable to Power Up Time[1,2]	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[1,2]	—	15	—	17	—	20	—	25	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10	—	10	—	10	—	10	—	ns
t_{SAA}	Semaphore Address Access[3]	—	15	—	17	—	20	—	25	ns

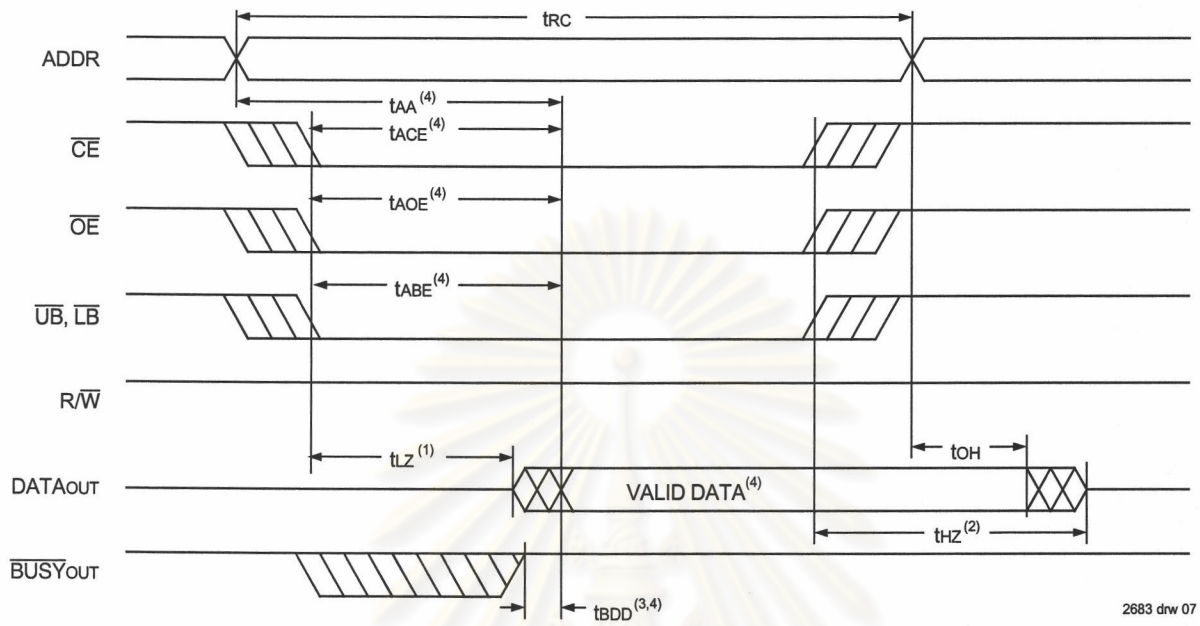
2683 tbl 12a

Symbol	Parameter	7025X35 Com'l & Military		7025X55 Com'l, Ind & Military		7025X70 Military Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	35	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	35	—	55	—	70	ns
t_{ACE}	Chip Enable Access Time[3]	—	35	—	55	—	70	ns
t_{ABE}	Byte Enable Access Time[3]	—	35	—	55	—	70	ns
t_{AOE}	Output Enable Access Time[3]	—	20	—	30	—	35	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1,2]	3	—	3	—	3	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	15	—	25	—	30	ns
t_{PU}	Chip Enable to Power Up Time[1,2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[1,2]	—	35	—	50	—	50	ns
t_{SOP}	Semaphore Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	15	—	15	—	15	—	ns
t_{SAA}	Semaphore Address Access[3]	—	35	—	55	—	70	ns

2683 tbl 12b

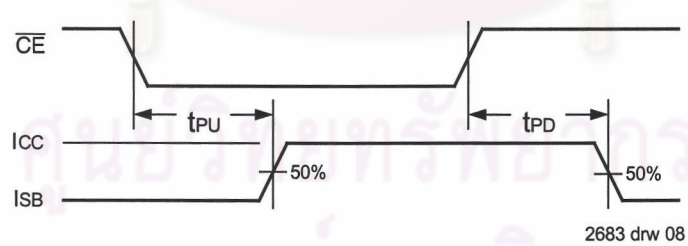
NOTES:
1. Transition is measured ±500mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterazation, but is not production tested.
3. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, and $\overline{SEM}$ = V_{IH}. To access semephore, $\overline{CE}$ = V_{IH} or $\overline{UB}$ & $\overline{LB}$ = V_{IH}, and $\overline{SEM}$ = V_{IL}.
4. 'X' in part number indicates power rating (S or L).
5. Industrial temperature: for other speeds, packages and powers contact your sales office.

Waveform of Read Cycles(5)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$, $\overline{CE}$, $\overline{LB}$, or $\overline{UB}$.
2. Timing depends on which signal is de-asserted first, $\overline{CE}$, $\overline{OE}$, $\overline{LB}$, or $\overline{UB}$.
3. t_{BDD} delay is required only in case where opposite port is completing a write operation to the same address location for simultaneous read operations BUSY has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last t_{ABE}, t_{AOE}, t_{ACE}, t_{AA} or t_{BDD}.
5. $\overline{SEM}$ = V_{IH}.

Timing of Power-Up Power-Down



AC Electrical Characteristics Over the Operating Temperature and Supply Voltage[5,6]

Symbol	Parameter	7025X15 Com'l Only		7025X17 Com'l Only		7025X20 Com'l & Military		7025X25 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE										
t_{WC}	Write Cycle Time	15	—	17	—	20	—	25	—	ns
t_{EW}	Chip Enable to End-of-Write[3]	12	—	12	—	15	—	20	—	ns
t_{AW}	Address Valid to End-of-Write	12	—	12	—	15	—	20	—	ns
t_{AS}	Address Set-up Time[3]	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	12	—	15	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	10	—	10	—	15	—	15	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	10	—	10	—	12	—	15	ns
t_{DH}	Data Hold Time[4]	0	—	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,2]	—	10	—	10	—	12	—	15	ns
t_{OW}	Output Active from End-of-Write[1,2,4]	0	—	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	5	—	ns

2683 tbl 13a

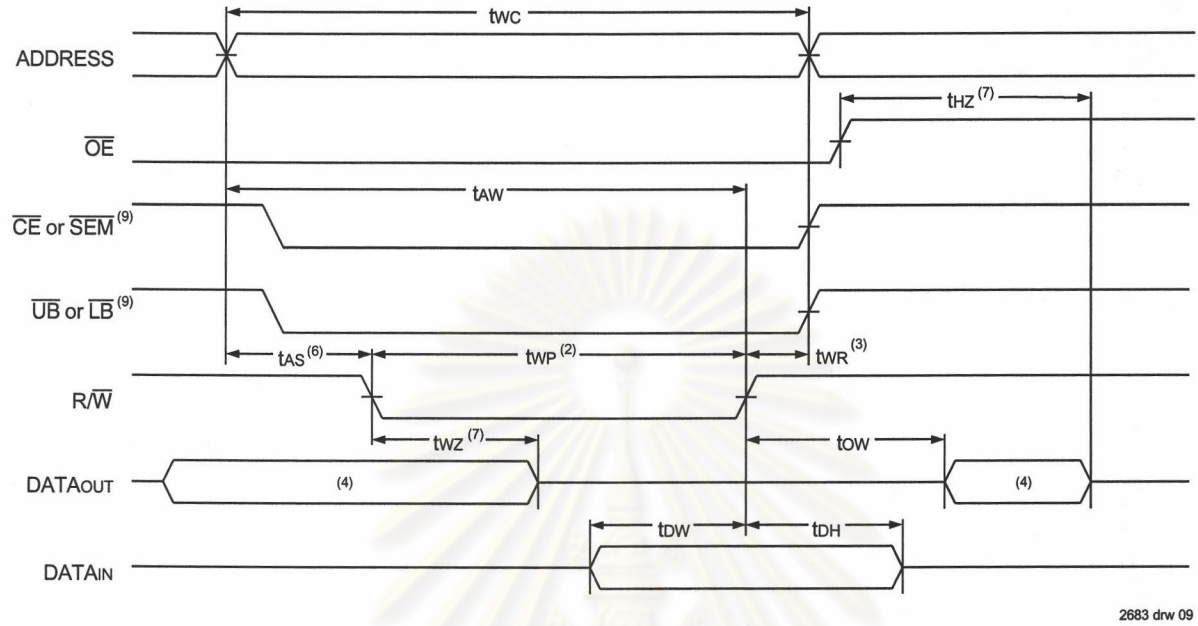
Symbol	Parameter	7025X35 Com'l & Military		7025X55 Com'l, Ind & Military		7025X70 Military Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	35	—	55	—	70	—	ns
t_{EW}	Chip Enable to End-of-Write[3]	30	—	45	—	50	—	ns
t_{AW}	Address Valid to End-of-Write	30	—	45	—	50	—	ns
t_{AS}	Address Set-up Time[3]	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	40	—	50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	30	—	40	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	15	—	25	—	30	ns
t_{DH}	Data Hold Time[4]	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,2]	—	15	—	25	—	30	ns
t_{OW}	Output Active from End-of-Write[1,2,4]	0	—	0	—	0	—	ns
t_{SWRD}	$\overline{SEM}$ Flag Write to Read Time	5	—	5	—	5	—	ns
t_{SPS}	$\overline{SEM}$ Flag Contention Window	5	—	5	—	5	—	ns

2683 tbl 13b

NOTES:

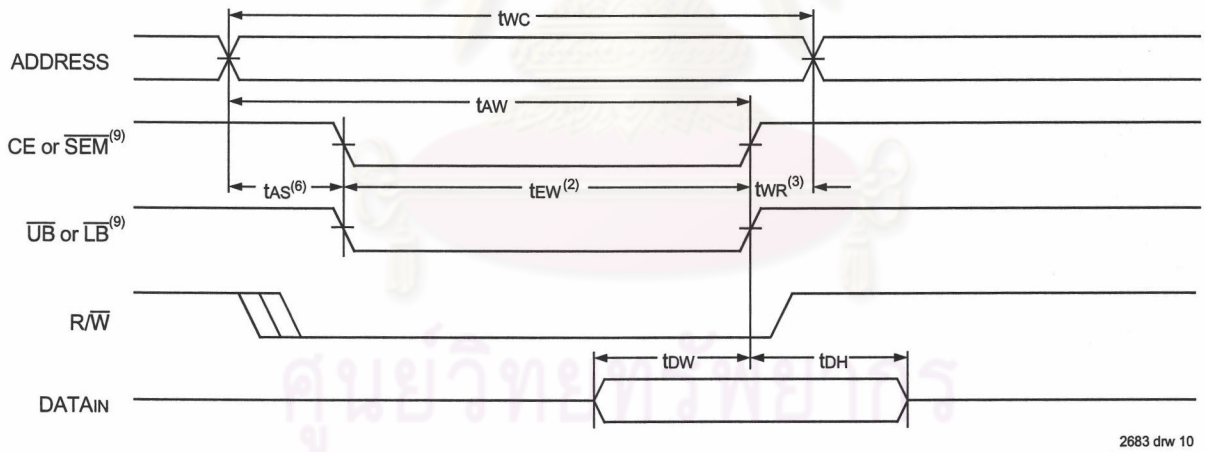
1. Transition is measured ±500mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH} or $\overline{UB}$ & $\overline{LB}$ = V_{IH}, and $\overline{SEM}$ = V_{IL}. Either condition must be valid for the entire t_{EW} time.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
5. 'X' in part number indicates power rating (S or L).
6. Industrial temperature: for other speeds, packages and powers contact your sales office.

Timing Waveform of Write Cycle No. 1, R/$\overline{W}$ Controlled Timing(1,5,8)



2683 drw 09

Timing Waveform of Write Cycle No. 2, $\overline{CE}$, $\overline{UB}$, $\overline{LB}$ Controlled Timing(1,5)

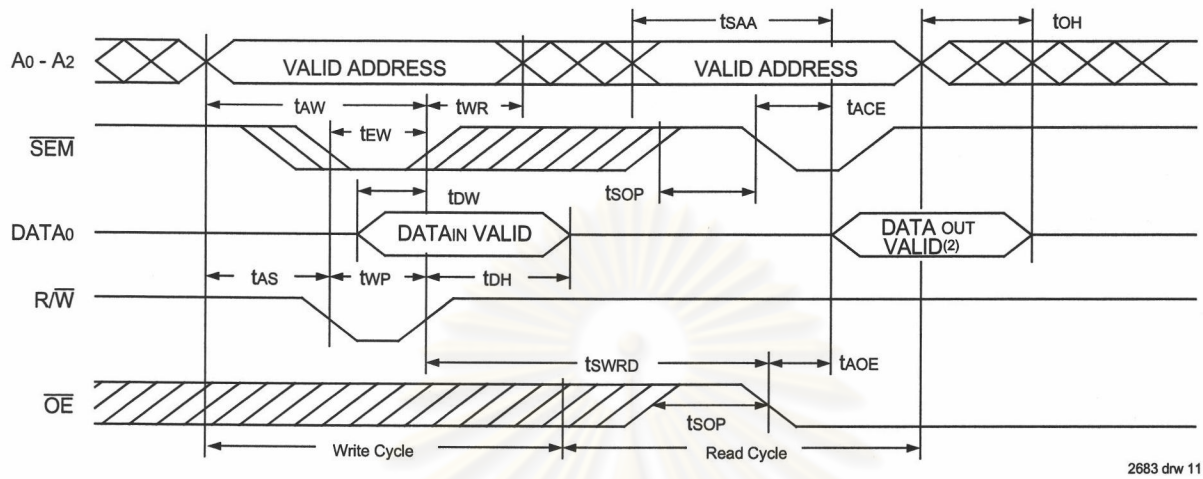


2683 drw 10

NOTES:

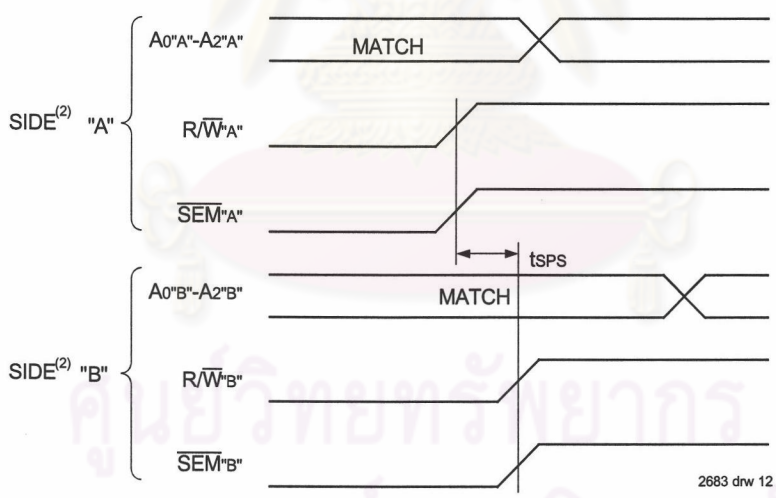
1. R/$\overline{W}$ or $\overline{CE}$ or $\overline{UB}$ & $\overline{LB}$ = VIH during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a $\overline{UB}$ or $\overline{LB}$ = VIL and a $\overline{CE}$ = VIL and a R/$\overline{W}$ = VIL for memory array writing cycle.
3. tWR is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ (or $\overline{SEM}$ or R/$\overline{W}$) going to VIH to the end-of-write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ or $\overline{SEM}$ LOW = VIL transition occurs simultaneously with or after the R/W = VIL transition, the outputs remain in the HIGH impedance state.
6. Timing depends on which enable signal is asserted last, $\overline{CE}$, R/$\overline{W}$, or byte control.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured ±500mV from steady state with Output Test Load (Figure 2).
8. If $\overline{OE}$ = VIL during R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ = VIH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
9. To access RAM, $\overline{CE}$ = VIL, $\overline{UB}$ or $\overline{LB}$ = VIL, and $\overline{SEM}$ = VIH. To access Semaphore, $\overline{CE}$ = VIH or $\overline{UB}$ & $\overline{LB}$ = VIL, and $\overline{SEM}$ = VIL. tEW must be met for either condition.

Timing Waveform of Semaphore Read after Write Timing, Either Side[1]



NOTE:
1. $\overline{CE}$ = VIH or $\overline{UB}$ & $\overline{LB}$ = VIH for the duration of the above timing (both write and read cycle).
2. "DATAOUT VALID" represents all I/O's (I/O0-I/O15) equal to the semaphore value.

Timing Waveform of Semaphore Write Contention[1,3,4]



NOTES:
1. DOR = DOL = VIL, $\overline{CE}_R$ = $\overline{CE}_L$ = VIH, or both $\overline{UB}$ & $\overline{LB}$ = VIH.
2. All timing is the same for left and right port. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
3. This parameter is measured from R/$\overline{W}$"A" or $\overline{SEM}$"A" going HIGH to R/$\overline{W}$"B" or $\overline{SEM}$"B" going HIGH.
4. If tSPS is not satisfied, there is no guarantee which side will obtain the semaphore flag.

AC Electrical Characteristics Over the Operating Temperature Supply Voltage Range[6,7]

Symbol	Parameter	7025X15 Com'l Ony		7025X17 Com'l Only		7025X20 Com'l & Military		7025X25 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{BUSY}$ TIMING ($M/\overline{S}$ = V_{IH})										
t_{BAA}	$\overline{BUSY}$ Access Time from Address Match	—	15	—	17	—	20	—	20	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address Not Matched	—	15	—	17	—	20	—	20	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	15	—	17	—	20	—	20	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	15	—	17	—	17	—	17	ns
t_{APS}	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data[3]	—	18	—	18	—	30	—	30	ns
t_{WH}	Write Hold After $\overline{BUSY}$[5]	12	—	13	—	15	—	17	—	ns
$\overline{BUSY}$ TIMING ($M/\overline{S}$ = V_{IL})										
t_{WB}	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$[5]	12	—	13	—	15	—	17	—	ns
PORT-TO-PORT DELAY TIMING										
t_{WDD}	Write Pulse to Data Delay[1]	—	30	—	30	—	45	—	50	ns
t_{DDD}	Write Data Valid to Read Data Delay[1]	—	25	—	25	—	35	—	35	ns

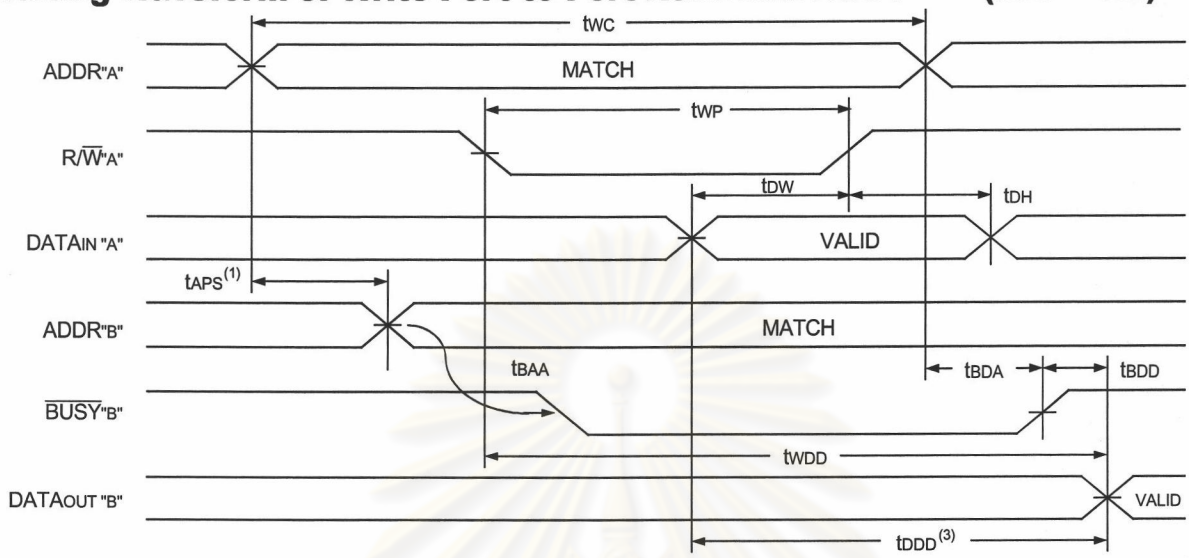
2683 tbl 14a

Symbol	Parameter	7025X35 Com'l & Military		7025X55 Com'l, Ind & Military		7025X70 Military Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{BUSY}$ TIMING ($M/\overline{S}$ = V_{IH})								
t_{BAA}	$\overline{BUSY}$ Access Time from Address Match	—	20	—	45	—	45	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address Not Matched	—	20	—	40	—	40	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable LOW	—	20	—	40	—	40	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable HIGH	—	20	—	35	—	35	ns
t_{APS}	Arbitration Priority Set-up Time[2]	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data[3]	—	35	—	40	—	45	ns
t_{WH}	Write Hold After $\overline{BUSY}$[5]	25	—	25	—	25	—	ns
$\overline{BUSY}$ TIMING ($M/\overline{S}$ = V_{IL})								
t_{WB}	$\overline{BUSY}$ Input to Write[4]	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$[5]	25	—	25	—	25	—	ns
PORT-TO-PORT DELAY TIMING								
t_{WDD}	Write Pulse to Data Delay[1]	—	60	—	80	—	95	ns
t_{DDD}	Write Data Valid to Read Data Delay[1]	—	45	—	65	—	80	ns

2683 tbl 14b

NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write Port-to-Port Read and $\overline{BUSY}$ ($M/\overline{S}$ = V_{IH})".
2. To ensure that the earlier of the two ports wins.
3. t_{BDD} is a calculated parameter and is the greater of 0ns, t_{WDD} – t_{WP} (actual) or t_{DDD} – t_{DW} (actual).
4. To ensure that the write cycle is inhibited on Port "B" during contention with Port "A".
5. To ensure that a write cycle is completed on Port "B" after contention with Port "A".
6. 'X' in part number indicates power rating (S or L).
7. Industrial temperature: for other speeds, packages and powers contact your sales office.

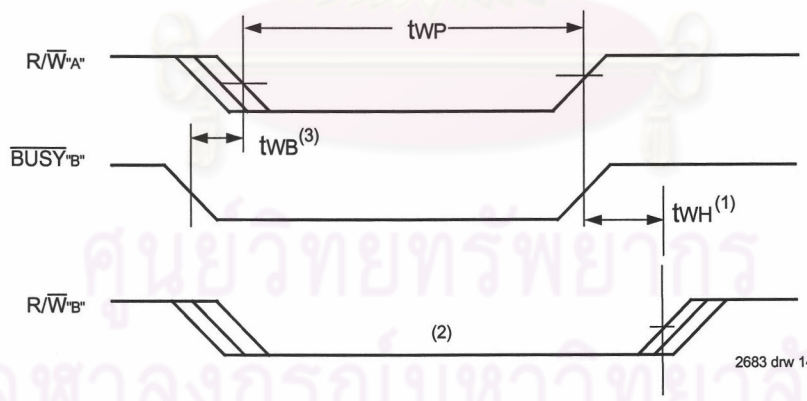
Timing Waveform of Write Port-to-Port Read and $\overline{BUSY}^{(2,4,5)}$ ($M/\overline{S}$ = VIH)



2683 drw 13

NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for $M/\overline{S}$ = VIL (slave).
2. $\overline{CE}_L = \overline{CE}_R$ = VIL.
3. $\overline{OE}$ = VIL for the reading port.
4. If $M/\overline{S}$ = VIL (SLAVE), then $\overline{BUSY}$ is an input. Therefore in this example $\overline{BUSY}_{"A"}$ = VIH and $\overline{BUSY}_{"B"}$ input is shown.
5. All timing is the same for left and right ports. Port "A" may be either the left of right port. Port "B" is the opposite port from Port "A".

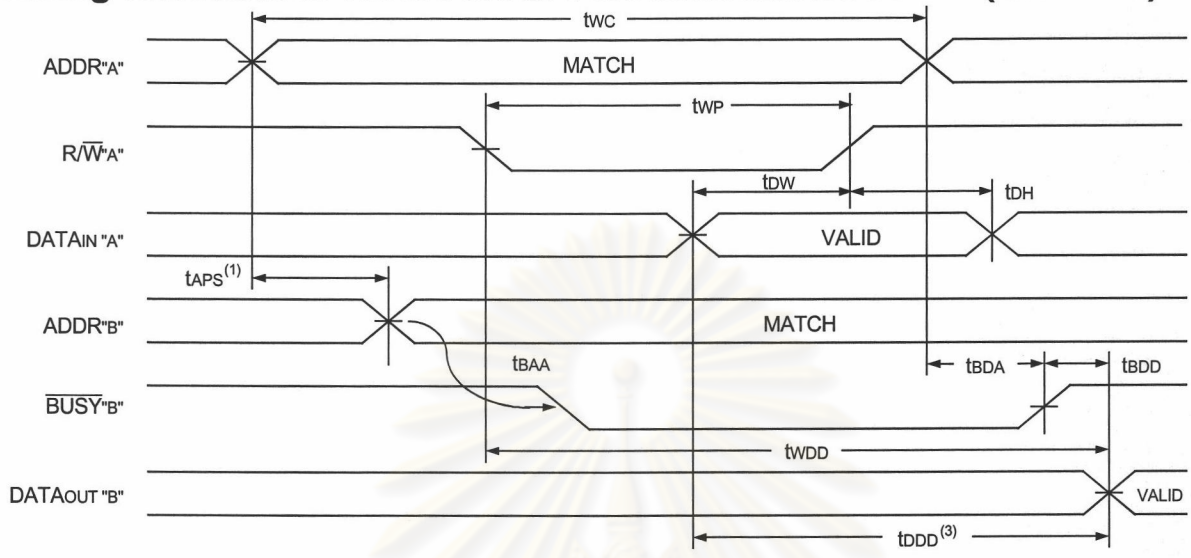
Timing Waveform of Write with $\overline{BUSY}$



2683 drw 14

NOTES:
1. tWH must be met for both $\overline{BUSY}$ input (slave) output master.
2. $\overline{BUSY}$ is asserted on port "B" Blocking $R/\overline{W}_{"B"}$, until $\overline{BUSY}_{"B"}$ goes HIGH.
3. tWB is only for the 'Slave' Version.

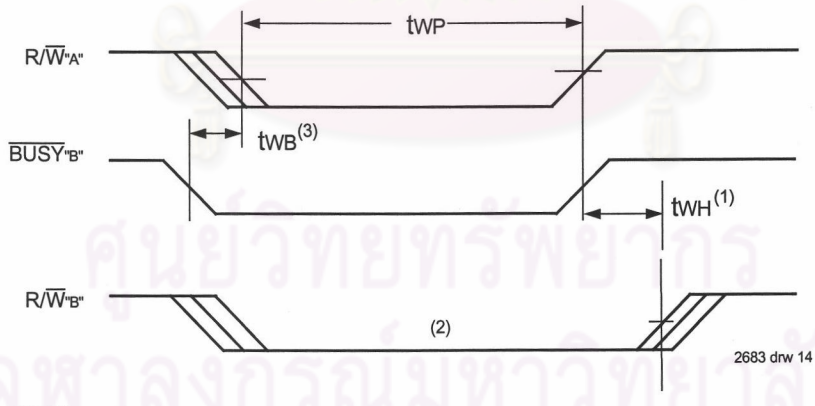
Timing Waveform of Write Port-to-Port Read and $\overline{BUSY}^{(2,4,5)}$ ($M/\overline{S}$ = VIH)



2683 drw 13

NOTES:
1. To ensure that the earlier of the two ports wins. tAPS is ignored for $M/\overline{S}$ = VIL (slave).
2. $\overline{CE}_L = \overline{CE}_R$ = VIL.
3. $\overline{OE}$ = VIL for the reading port.
4. If $M/\overline{S}$ = VIL (SLAVE), then $\overline{BUSY}$ is an input. Therefore in this example $\overline{BUSY}_{"A"}$ = VIH and $\overline{BUSY}_{"B"}$ input is shown.
5. All timing is the same for left and right ports. Port "A" may be either the left of right port. Port "B" is the opposite port from Port "A".

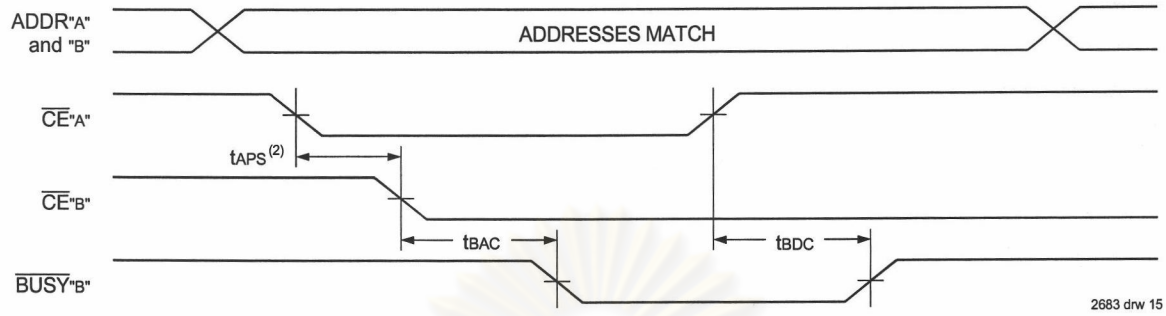
Timing Waveform of Write with $\overline{BUSY}$



2683 drw 14

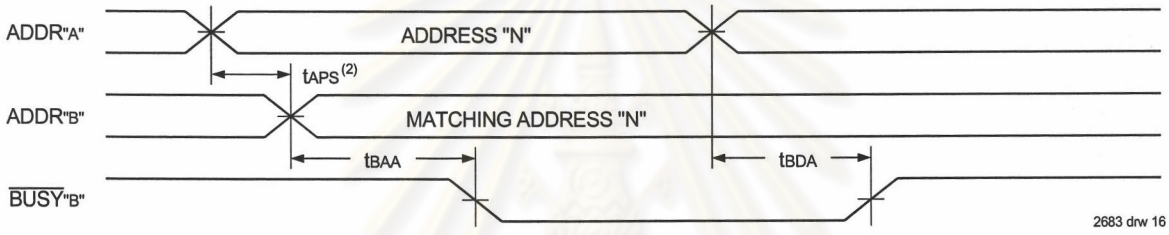
NOTES:
1. tWH must be met for both $\overline{BUSY}$ input (slave) output master.
2. $\overline{BUSY}$ is asserted on port "B" Blocking $R/\overline{W}_{"B"}$, until $\overline{BUSY}_{"B"}$ goes HIGH.
3. tWB is only for the 'Slave' Version.

Waveform of $\overline{BUSY}$ Arbitration Controlled by $\overline{CE}$ Timing(1) (M/$\overline{S}$ = VIH)



2683 drw 15

Waveform of $\overline{BUSY}$ Arbitration Cycle Controlled by Address Match Timing(1) (M/$\overline{S}$ = VIH)



2683 drw 16

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is not satisfied, the $\overline{BUSY}$ signal will be asserted on one side or another but there is no guarantee on which side $\overline{BUSY}$ will be asserted.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(1,2)

		7025X15 Com'l Only		7025X17 Com'l Only		7025X20 Com'l & Military		7025X25 Com'l & Military		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
INTERRUPT TIMING										
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	15	—	15	—	20	—	20	ns
tINR	Interrupt Reset Time	—	15	—	15	—	20	—	20	ns

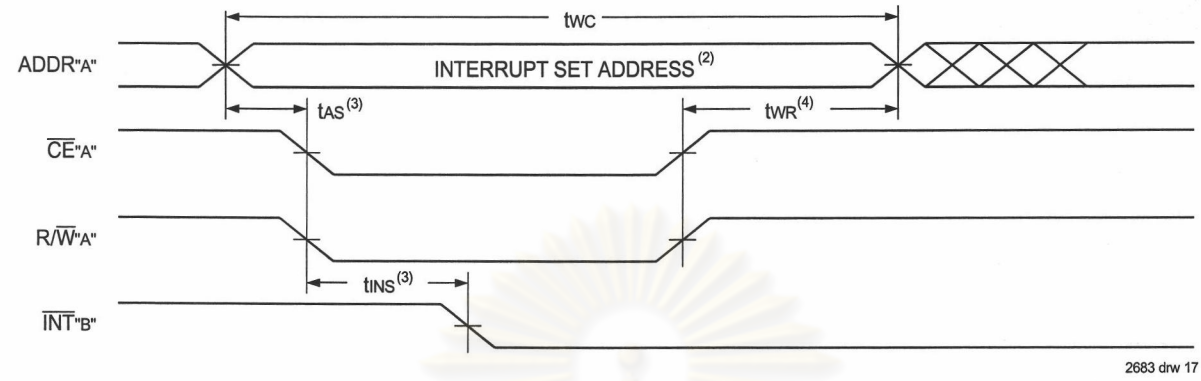
2683 tbl 15a

		7025X35 Com'l & Military		7025X55 Com'l, Ind & Military		7025X70 Military Only		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
INTERRUPT TIMING								
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tINS	Interrupt Set Time	—	25	—	40	—	50	ns
tINR	Interrupt Reset Time	—	25	—	40	—	50	ns

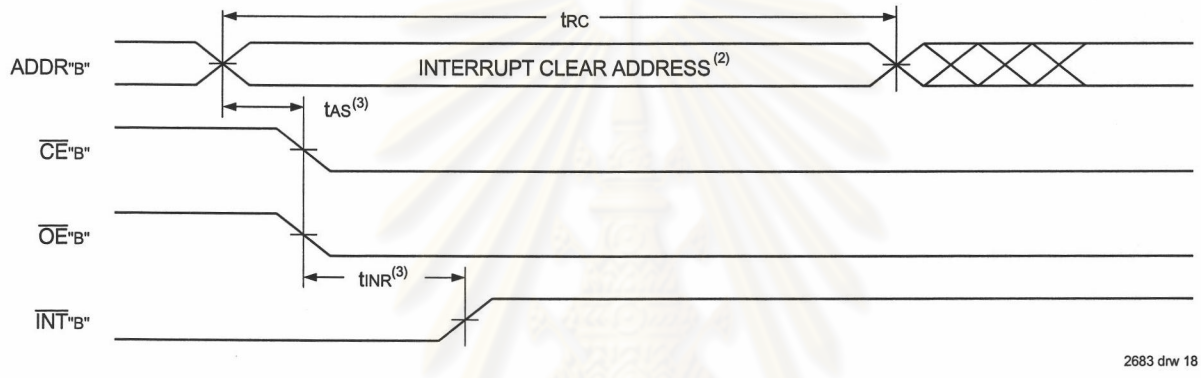
2683 tbl 15b

NOTES:
1. 'X' in part number indicates power rating (S or L).
2. Industrial temperature: for other speeds, packages and powers contact your sales office.

Waveform of Interrupt Timing[1]



2683 drw 17



2683 drw 18

NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt Flag Truth Table.
3. Timing depends on which enable signal ($\overline{CE}$ or $R/\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or $R/\overline{W}$) is de-asserted first.

Truth Tables

Truth Table I — Interrupt Flag[1]

Left Port					Right Port					
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	A_{0L}-A_{12L}	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	A_{0R}-A_{12R}	$\overline{INT}_R$	Function
L	L	X	1FFF	X	X	X	X	X	L[2]	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	1FFF	H[3]	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L[3]	L	L	X	1FFE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	1FFE	H[2]	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

2689 tbl 16

NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R = V_{IH}$.
2. If $\overline{BUSY}_L = V_{IL}$, then no change.
3. If $\overline{BUSY}_R = V_{IL}$, then no change.
4. $\overline{INT}_R$ and $\overline{INT}_L$ must be initialized at power-up.

Truth Table II — Address $\overline{BUSY}$ Arbitration

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{12L} A_{0R}-A_{12R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

2683 tbl 17

NOTES:
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs when the part is configured as a master. $\overline{BUSY}$ are inputs when configured as a slave. $\overline{BUSY}_X$ outputs on the IDT7025 are push pull, not open drain outputs. On slaves the $\overline{BUSY}$ asserted internally inhibits write.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = LOW will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs cannot be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of actual logic level on the pin.

Truth Table III — Example of Semaphore Procurement Sequence(1,2,3)

Functions	D_0 - D_{15} Left	D_0 - D_{15} Right	Status
No Action	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Right Port Writes "0" to Semaphore	0	1	No change. Right side has no write access to semaphore
Left Port Writes "1" to Semaphore	1	0	Right port obtains semaphore token
Left Port Writes "0" to Semaphore	1	0	No change. Left port has no write access to semaphore
Right Port Writes "1" to Semaphore	0	1	Left port obtains semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free
Right Port Writes "0" to Semaphore	1	0	Right port has semaphore token
Right Port Writes "1" to Semaphore	1	1	Semaphore free
Left Port Writes "0" to Semaphore	0	1	Left port has semaphore token
Left Port Writes "1" to Semaphore	1	1	Semaphore free

2683 tbl 18

NOTES:
1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7025.
2. There are eight semaphore flags written to via I/O_0 and read from all I/0's. These eight semaphores are addressed by A_0 - A_2.
3. $\overline{CE}$ = V_{IH}, $\overline{SEM}$ = V_{IL}, to access the semaphores. Refer to the Semaphore Read/Write Truth Table.

Functional Description

The IDT7025 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7025 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ = V_{IH}). When a port is enabled, access to the entire memory array is permitted.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 1FFE (HEX), where a write is defined as the $\overline{CE}_R$ = R/$\overline{W}_R$ = V_{IL} per Truth Table I. The left port clears the interrupt by an address location 1FFE access when $\overline{CE}_L$ = $\overline{OE}_L$ = V_{IL}, R/$\overline{W}_L$ is a "don't care". Likewise, the right port interrupt flag (INT_R) is asserted when the left port writes to memory location 1FFF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must access the memory location 1FFF, The message (16 bits) at 1FFE or 1FFF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 1FFE and 1FFF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table I for the interrupt operation.

Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The $\overline{BUSY}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a $\overline{BUSY}$ indication, the write signal is gated internally to prevent the write from proceeding.

The use of $\overline{BUSY}$ logic is not required or desirable for all applications. In some cases it may be useful to logically OR the $\overline{BUSY}$ outputs together and use any $\overline{BUSY}$ indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of $\overline{BUSY}$ logic is not desirable, the $\overline{BUSY}$ logic can be disabled by placing the part in slave mode with the M/$\overline{S}$ pin. Once in slave mode the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins HIGH. If desired, unintended write operations can be prevented to a port by tying the $\overline{BUSY}$ pin for that port LOW.

The $\overline{BUSY}$ outputs on the IDT 7025 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the $\overline{BUSY}$ indication for the resulting array requires the use of an external AND gate.

Width Expansion with Busy Logic Master/Slave Arrays

When expanding an IDT7025 RAM array in width while using $\overline{BUSY}$ logic, one master part is used to decide which side of the RAM array will receive a $\overline{BUSY}$ indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the $\overline{BUSY}$ signal as a write inhibit signal. Thus on the IDT7025 RAM the $\overline{BUSY}$ pin is an output if the part is used as a master (M/$\overline{S}$ pin = V_{IH}), and the $\overline{BUSY}$ pin is an input if the part used as a slave (M/$\overline{S}$ pin = V_{IL}) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating $\overline{BUSY}$ on one side of the array and another master indicating $\overline{BUSY}$ on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The $\overline{BUSY}$ arbitration, on a master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a $\overline{BUSY}$ flag to be output from the master before the actual write pulse can be initiated with either the R/$\overline{W}$ signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

Semaphores

The IDT7025 is an extremely fast Dual-Port 8K x 16 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer's software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, and both ports are completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from, or written to, at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by $\overline{CE}$, the Dual-Port RAM enable, and $\overline{SEM}$, the semaphore enable. The $\overline{CE}$ and $\overline{SEM}$ pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table I where $\overline{CE}$ and $\overline{SEM}$ are both = V_{IH}.

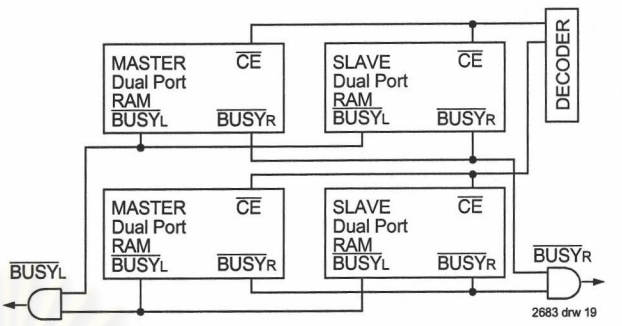


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7025 RAMs.

Systems which can best use the IDT7025 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT7025's hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT7025 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

How the Semaphore Flags Work

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called "Token Passing Allocation." In this method, the state of a semaphore latch is used as a token indicating that shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then verifies its success in setting the latch by reading it. If it was successful, it proceeds to assume control over the shared resource. If it was not successful in setting the latch, it determines that the right side processor has set the latch first, has the token and is using the shared resource. The left processor can then either repeatedly request

that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active LOW. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7025 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a LOW input on the $\overline{SEM}$ pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, $\overline{OE}$, and R/$\overline{W}$) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins $A_0 - A_2$. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin D_0 is used. If a LOW level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Truth Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select ($\overline{SEM}$) and output enable ($\overline{OE}$) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal ($\overline{SEM}$ or $\overline{OE}$) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Truth Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag LOW and the other side HIGH. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay LOW until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Using Semaphores—Some Examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7025's Dual-Port RAM. Say the 8K x 16 RAM was to be divided into two 4K x 16 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 4K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 4K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 4K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 4K blocks of Dual-Port RAM with each other.

The blocks do not have to be any particular size and can even be

variable, depending upon the complexity of the software using the semaphore flags. All eight semaphores could be used to divide the Dual-Port RAM or other shared resources into eight parts. Semaphores can even be assigned different meanings on different sides rather than being given a common meaning as was shown in the example above.

Semaphores are a useful form of arbitration in systems like disk interfaces where the CPU must be locked out of a section of memory during a transfer and the I/O device cannot tolerate any wait states. With the use of semaphores, once the two devices has determined which memory area was "off-limits" to the CPU, both the CPU and the I/O devices could access their assigned portions of memory continuously without any wait states.

Semaphores are also useful in applications where no memory "WAIT" state is available on one or both sides. Once a semaphore handshake has been performed, both processors can access their assigned RAM segments at full speed.

Another application is in the area of complex data structures. In this case, block arbitration is very important. For this application one processor may be responsible for building and updating a data structure. The other processor then reads and interprets that data structure. If the interpreting processor reads an incomplete data structure, a major error condition may exist. Therefore, some sort of arbitration must be used between the two different processors. The building processor arbitrates for the block, locks it and then is able to go in and update the data structure. When the update is completed, the data structure block is released. This allows the interpreting processor to come back and read the complete data structure, thereby guaranteeing a consistent data structure.

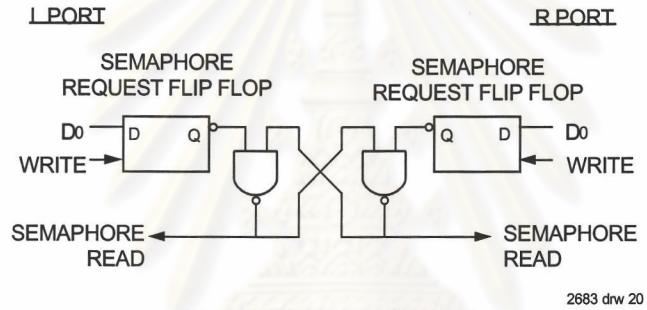
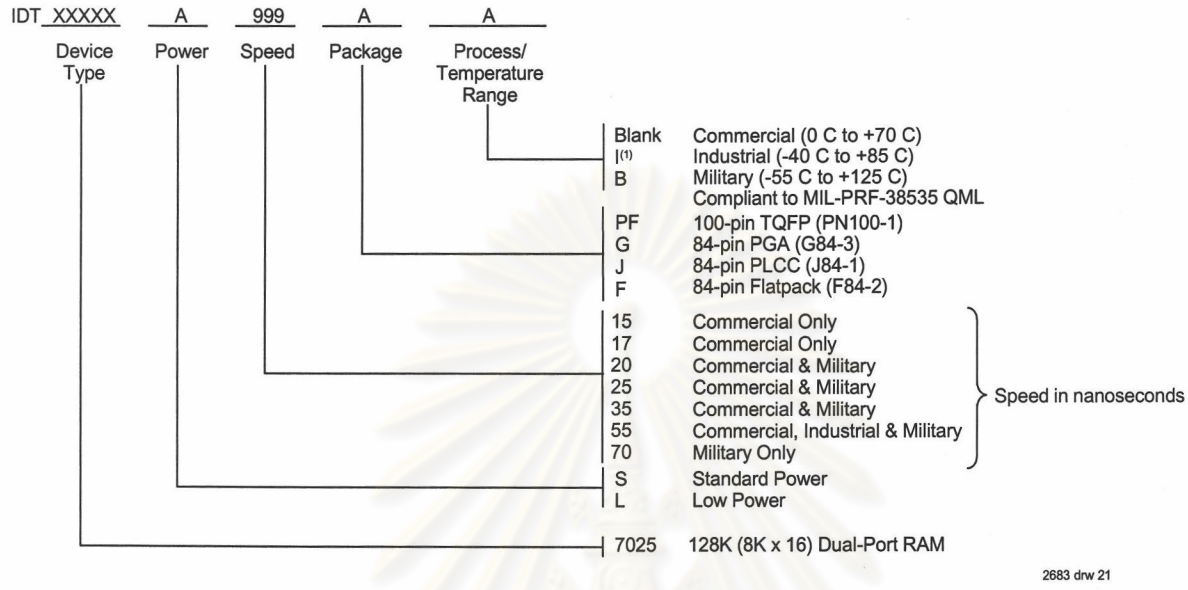


Figure 4. IDT7025 Semaphore Logic

Ordering Information



NOTE:
1. Industrial range is available on selected PLCC packages in standard power. For other speeds, packages and powers contact your sales office.

Datasheet Document History

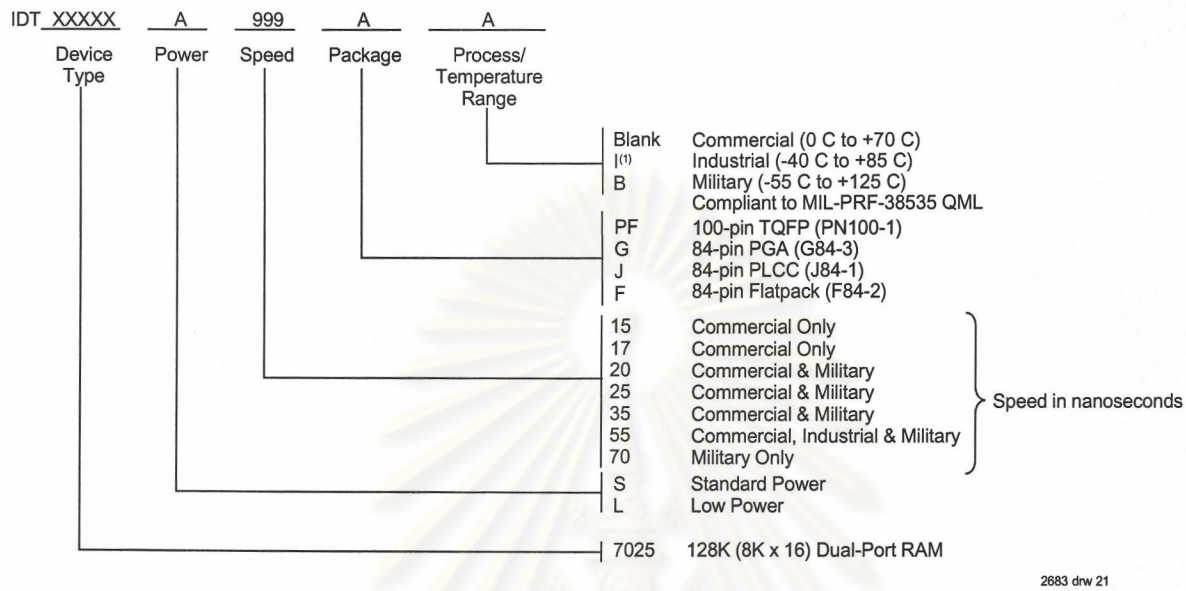
1/13/99: Initiated datasheet document history
Converted to new format
Cosmetic and typographical corrections
Pages 2 and 3 Added additional notes to pin configurations

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
831-754-4613
DualPortHelp@idt.com

Ordering Information



NOTE:
1. Industrial range is available on selected PLCC packages in standard power. For other speeds, packages and powers contact your sales office.

Datasheet Document History

1/13/99: Initiated datasheet document history
Converted to new format
Cosmetic and typographical corrections
Pages 2 and 3 Added additional notes to pin configurations

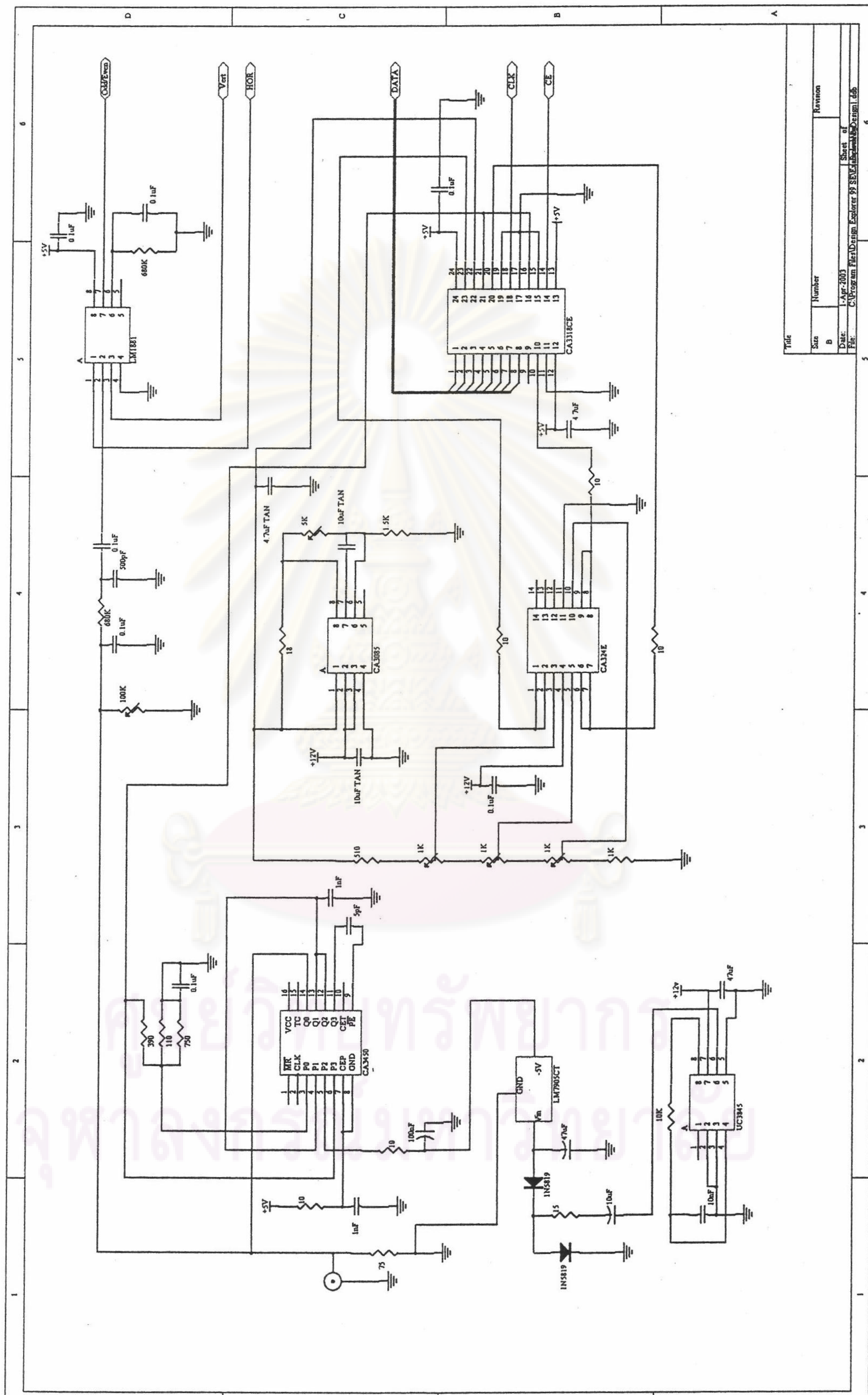
CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

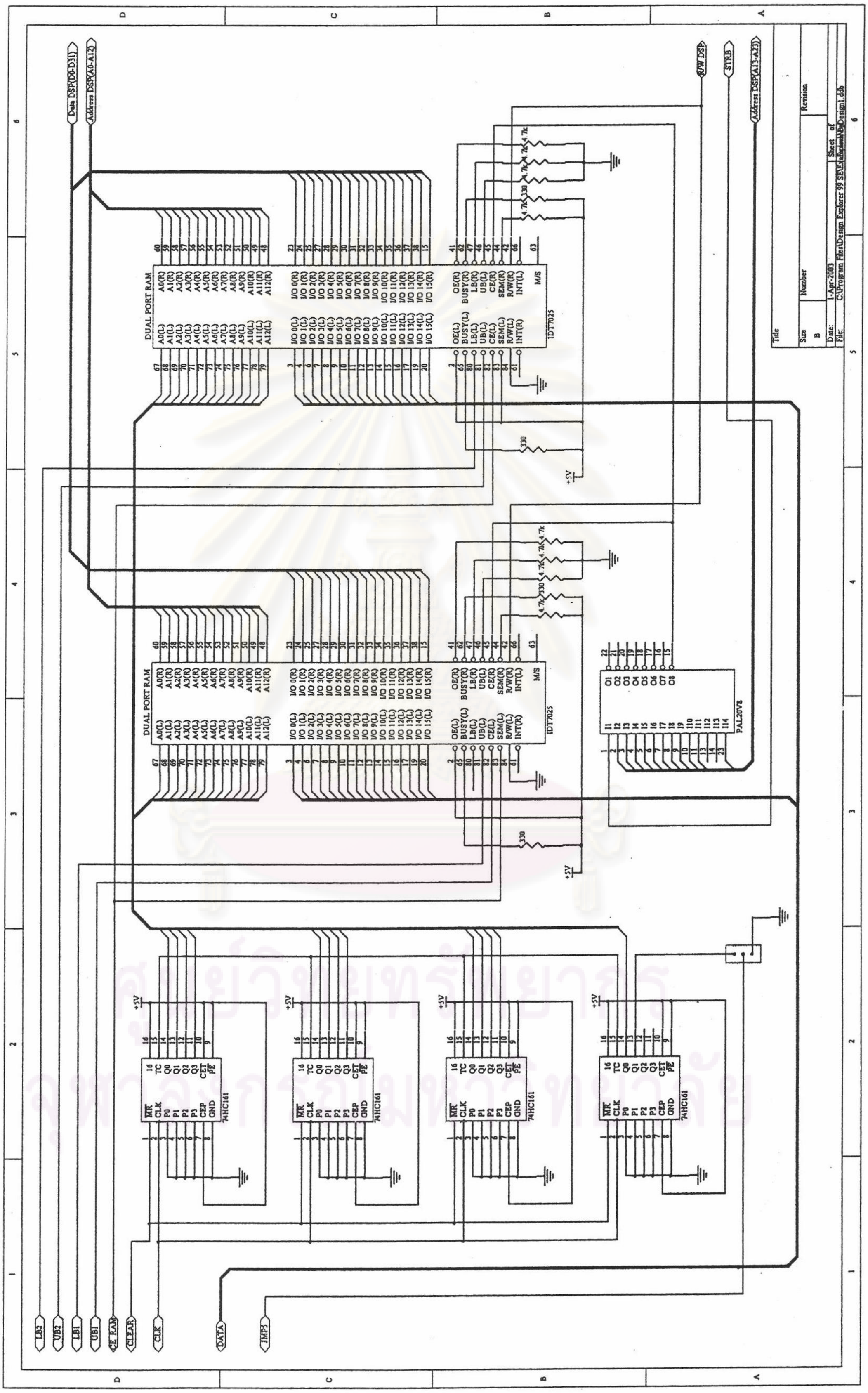
for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

for Tech Support:
831-754-4613
DualPortHelp@idt.com

ภาคผนวก ง

แผนภาพวงจร


Odd/Even
Vert
HOR
DATA
CLK
CE
LM1881
CA3318CE
CA3085
CA324E
CA3450
LM7905CT
UC3845
1N5819
Title
Size
B
Number
Revision
Date:
1-Apr-2003
File:
Sheet of


Data DSP(D0-D31)
Address DSP(A0-A12)
R/W DSP
STRB
Address DSP(A13-A23)
DUAL PORT RAM
IDT7025
DUAL PORT RAM
IDT7025
PAL20V8
74HC161
74HC161
74HC161
74HC161
LB2
UB2
LB1
UB1
CE RAM
CLEAR
CLK
DATA
IMPS

ประวัติผู้เขียนวิทยานิพนธ์

นางสาวภิญญาภัทร์ ศรีกฤษณ์ จบการศึกษาวิทยาศาตรบัณฑิต สาขาฟิสิกส์อุตสาหกรรมและอุปกรณ์การแพทย์ คณะวิทยาศาสตร์ประยุกต์ สถาบันเทคโนโลยีเพระจอมเกล้าพระนครเหนือข้าศึกษาต่อภาควิชานิวเคลียร์เทคโนโลยี คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัยในปีการศึกษา 2542

แบบฟอร์ม Research Mapping

สำหรับงานวิจัยเพื่อทำวิทยานิพนธ์ของนิสิต ระดับบัณฑิตศึกษา จุฬาลงกรณ์มหาวิทยาลัย

---

1. ชื่อ – นามสกุลนิสิต นางสาวกิญญาภัทร์ ศรีกาญจน์
   เลขประจำตัว 4270484921
2. อาจารย์ที่ปรึกษาวิทยานิพนธ์ อ. ดร. ทองอิน
3. ระดับ ☑ ปริญญาโท ☐ ปริญญาเอก สาขาวิชา .....
4. อนุมัติหัวข้อวิทยานิพนธ์เมื่อภาคการศึกษา ☐ ภาคต้น ☑ ภาคปลาย ปีการศึกษา 2543
5. คณะ/หน่วยงานที่รับผิดชอบ

☐ สหสาขาวิชา	☑ วิศวกรรมศาสตร์	☐ อักษรศาสตร์	☐ วิทยาศาสตร์
☐ รัฐศาสตร์	☐ สถาปัตยกรรมศาสตร์	☐ พาณิชยศาสตร์ฯ	☐ ครุศาสตร์
☐ นิเทศศาสตร์	☐ เศรษฐศาสตร์	☐ แพทยศาสตร์	☐ สัตวแพทยศาสตร์
☐ ทันตแพทยศาสตร์	☐ เภสัชศาสตร์	☐ นิติศาสตร์	☐ ศิลปกรรมศาสตร์
☐ พยาบาลศาสตร์	☐ ว.ประชากรศาสตร์	☐ จิตวิทยา	☐ อื่น ๆ ระบุ .....

6. โปรดระบุว่างานวิจัยที่จะจัดทำข้างต้นอยู่ในกลุ่มใด โดยทำเครื่องหมาย ✓ ในช่องแรก และระบุประเด็นหลักการวิจัยใน ช่องที่ 2

☐ **กลุ่มวิจัยเพื่อการพัฒนาด้านเกษตรและอุตสาหกรรมการเกษตร**	**ระบุประเด็นหลักการวิจัย (Main Theme or Key Words)**
..... (1) โครงการวิจัยเกี่ยวกับข้าว	
..... (2) โครงการวิจัยเกี่ยวกับยางพารา	
.....(3) โครงการวิจัยเกี่ยวกับการพัฒนาผลผลิตและผลิตภัณฑ์จากกุ้งกุลาดำ และกุ้งทะเลอื่น ๆ	
..... (4) โครงการวิจัยเกี่ยวกับการพัฒนาผลผลิต และผลิตภัณฑ์จากปลาสวยงามและพรรณไม้น้ำ	
..... (5) โครงการวิจัยเกี่ยวกับไม้ดอกไม้ประดับ	
..... (6) โครงการวิจัยเกี่ยวกับระบบเกษตร	
..... (7) โครงการวิจัยเกี่ยวกับโค สุกร และสัตว์ปีก	
..... (8) โครงการวิจัยเกี่ยวกับการพัฒนาไม้ผล	
..... (9) โครงการวิจัยเกี่ยวกับมันสำปะหลัง	
..... (10) โครงการวิจัยเกี่ยวกับการพัฒนาการใช้ประโยชน์จากไม้สวนป่า	
..... (11) โครงการวิจัยเกี่ยวกับอ้อย น้ำตาล และผลิตภัณฑ์	
..... (12) โครงการวิจัยเกี่ยวกับพัฒนาผลผลิต และผลิตภัณฑ์จากปลาทูน่า	
..... อื่น ๆ ระบุโครงการวิจัยเกี่ยวกับ	

* โปรดกรอกแบบฟอร์มแล้วส่งพร้อมวิทยานิพนธ์ฉบับสมบูรณ์ ที่งานมาตรฐานการศึกษา บัณฑิตวิทยาลัย

☑ กลุ่มวิจัยเพื่อการพัฒนาด้านวิทยาศาสตร์ เทคโนโลยี และอุตสาหกรรม	ระบุประเด็นหลักการวิจัย (Main Theme or Key Words)
..... (13) โครงการวิจัยเกี่ยวกับอุตสาหกรรมอาหารเพื่อการส่งเสริม	
..... (14) โครงการวิจัยเกี่ยวกับเทคโนโลยีสนับสนุนอุตสาหกรรมการผลิต	
..... (15) โครงการวิจัยเกี่ยวกับพลังงานทดแทนและการใช้พลังงานอย่างมีประสิทธิภาพ	
..... (16) โครงการวิจัยเกี่ยวกั เทคโนโลยีสะอาดและเทคโนโลยีบำบัดของเสีย	
..✓.. (17) โครงการวิจัยเกี่ยวกับการพัฒนาคอมพิวเตอร์ซอฟต์แวร์และฮาร์ดแวร์	RADIOGRAPHIC IMAGE / DPS TECHNIQUE
..... (18) โครงการวิจัยเกี่ยวกับนโยบายการพัฒนาอุตสาหกรรมไทย	
..... อื่น ๆ ระบุโครงการวิจัยเกี่ยวกับ	

☐ กลุ่มวิจัยเพื่อการพัฒนาด้านสุขภาพ	ระบุประเด็นหลักการวิจัย
.....(19) โครงการวิจัยด้านอุบัติเหตุและภยันตราย	
.....(20) โครงการวิจัยเกี่ยวกับสมรรถนะของมนุษย์	
.....(21) โครงการวิจัยเกี่ยวกับการกระจายอำนาจระบบบริการสุขภาพ	
..... (22) โครงการวิจัยเกี่ยวกับสมุนไพร	
.....(23) โครงการวิจัยเกี่ยวกับโรคเอดส์	
..... (24) โครงการวิจัยเกี่ยวกับโรคติดเชื้อ	
..... (25).โครงการวิจัยเกี่ยวกับโรคไม่ติดเชื้อ	
.....(26) โครงการวิจัยเกี่ยวกับชุดวินิจฉัยโรค	
.....(27) โครงการวิจัยเกี่ยวกับอุตสาหกรรมยาภายในประเทศ	
.....(28) โครงการวิจัยเกี่ยวกับภูมิปัญญาท้องถิ่นด้านสุขภาพ	
..... อื่น ๆ ระบุโครงการวิจัยเกี่ยวกับ	

☐ กลุ่มวิจัยเพื่อการพัฒนาด้านพัฒนาสังคม และวัฒนธรรม	ระบุประเด็นหลักการวิจัย
.....(29) โครงการวิจัยเกี่ยวกับสำนึกไทยและวินัยในวิถีชีวิตไทย	
.....(30) โครงการวิจัยเกี่ยวกับการจัดการทรัพยากรธรรมชาติของประเทศ	
.....(31) โครงการวิจัยเพื่อพัฒนาอุตสาหกรรมบริการด้านการท่องเที่ยว	
.....(32) โครงการวิจัยเกี่ยวกับผลกระทบจากกระแสโลกาภิวัตน์ต่อสังคมไทย	
.....(33) โครงการวิจัยเรื่องการบริหารจัดการในการป้องกันและแก้ไขวิกฤตยาเสพติดในประเทศไทย	
.....(34) โครงการวิจัยเกี่ยวกับแรงงานของประเทศ	
..... อื่น ๆ ระบุโครงการวิจัยเกี่ยวกับ	

(ลงนาม).....
อาจารย์ที่ปรึกษาวิทยานิพนธ์
...../...../.....

(ลงนาม) .....
นิสิตผู้ทำวิทยานิพนธ์
...../...../.....