Chapter 5

Building the pulse programmer unit

In the previous chapter, the GPIB interface contained in both the pulse programmer and the pulse shaping unit has been mentioned. In this chapter description this GPIB interface and the main circuit of the pulse programmer will be given. Since the GPIB system is a complicated system, so single chip microcomputer is used to control this system and to control the information storing in the pulse programmer or the pulse shaping unit.

The GPIB interface

Fig.5-1 shows the circuit of the GPIB interface, containing the microcomputer IC5 (8035 microcomputer that is in MCS-48) which is used to control other parts of the pulse programmer by passing IC8 (8255 I/O ports) and to communicate with the computer by passing the tri-state buffers IC3 and IC4 - (74LS245). These tri-state buffers will be active once the pulse programmer is turned on. When the pulse programmer is turned off they will be in tri-state or high impedance, and will not disturbed the GPIB system. This GPIB interface is only designed for the listener (see types of GPIB devices in appendix A). The 8035 microcomputer has two I/O ports. Since the GPIB system requires 16 lines - DIO$_{1-8}$, SRQ, IFC, DAV, ATN, EOI, NRFD, REN and NDAC - and the main circuit of the pulse programmer requires 21 lines to control its system, so it must expand I/O ports by using 8255 general purpose programmable I/O. Each device in the GPIB system has its own particular address, which is represented by a number 0-30. This number can be set by the DIP switch, a 5 pins behind each device. Each device must have different address from the others. In the other word, one address is used for one device. So not more than 30 devices can be connected to the GPIB system. IC1 and IC2 are used for searching the assigned address as soon as the pulse programmer is turned on or is

Fig.B-1 The circuit of the GPIB section of PPI1 and PPI2.

initialized with the GPSCLR or GPACLR command (see the GPIB commands in appendix A). The software that control the 8035 microcomputer contains in IC7, 2716 ROM. IC6 is used for separating 8 bits data bus and 8 bits address bus.

The software that control the GPIB interface and the main circuit of the pulse programmer will be considered in chapter 7.

The main circuit of the pulse programmer

In the previous chapter, the structure of the pulse programmer has been presented. In this section the details of the pulse programmer will be presented. The main circuit of the pulse programmer is shown in Fig.5-2. On the left of this circuit, it is connected with the GPIB interface. The first box on the top-left of the circuit is a 8 to 24 bit latch, that is active during the time of information-storing.

The information storing of the pulse programmer

When the pulse programmer is turned on, the GPIB interface and the other parts of the pulse programmer will be initialized. The 8 to 24 bit latch will be activated - $\overline{LE1}$, $\overline{LE2}$, $\overline{LE3}$ and $\overline{OE1}$ are low. The external clock from clock pin can pass through to the 16 bits binary counter - CPEN is high, but the 16 bit binary counter is disabled by its low $\overline{CE}$. The three memories (IC29, IC30 and IC31) are in the write state - $\overline{W}/R$ is low and $\overline{OE2}$ is high. D1 (data ready) is not lighted because $\overline{LED1}$ is high. The manual trigger switch (SW1) or external trigger is disabled - REN is low and start is high. The address generator consists of a down binary counter, a up binary counter, 11 bit latch, AND gates (IC32A, IC32B, IC32D), inverter (IC14E) and buffer (IC20F). It is reset address to zero by taking $\overline{RES}$ to low for a moment when INC and EOD are high. While the informations are sent to the pulse programmer, the GPIB interface is controlling the 8 to 24 latch to latch data every three bytes on Q0 - Q23. Then it increases one address by taking positive pulse on INC pin. The first and the second of three bytes data are stored in IC29
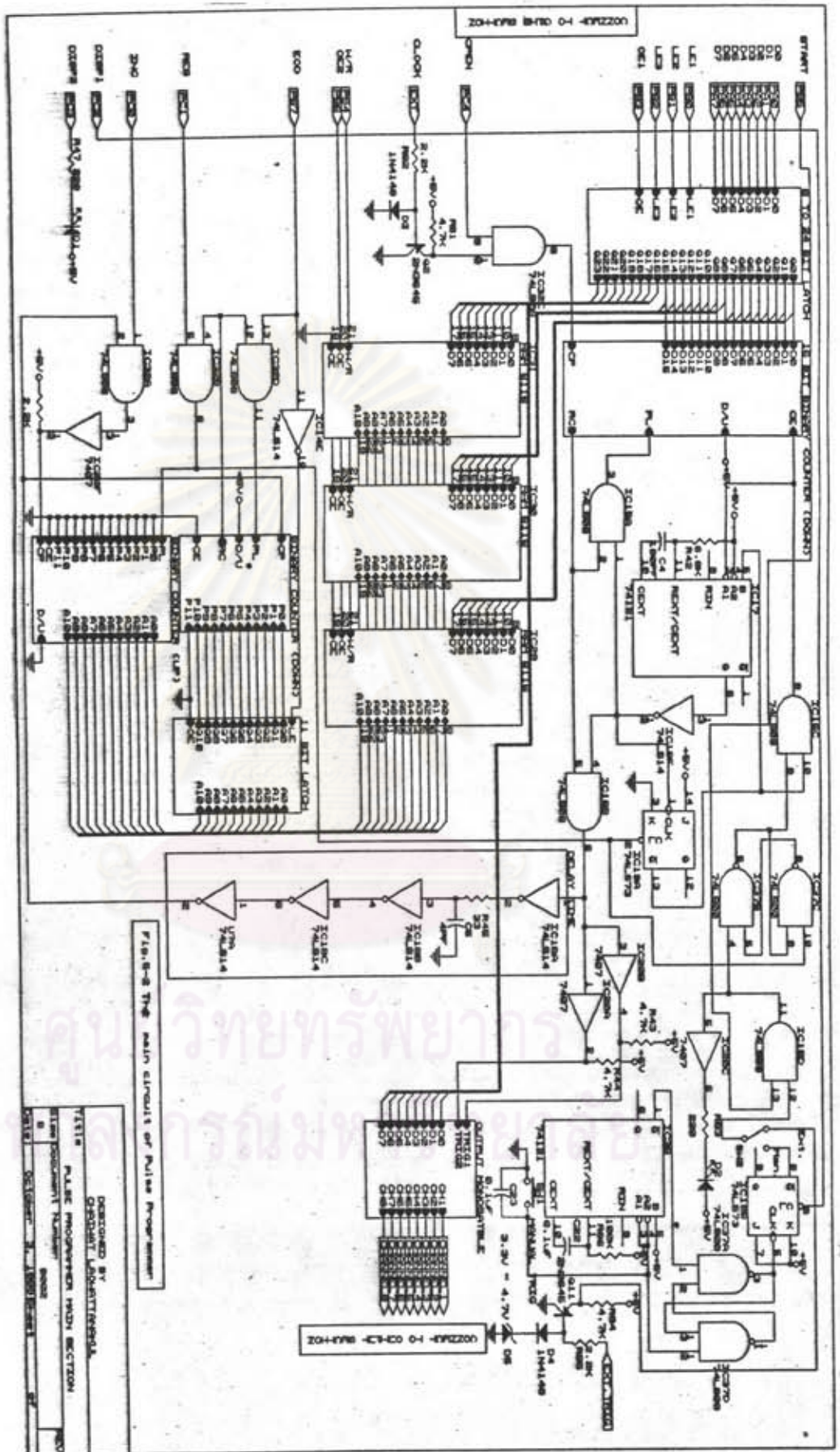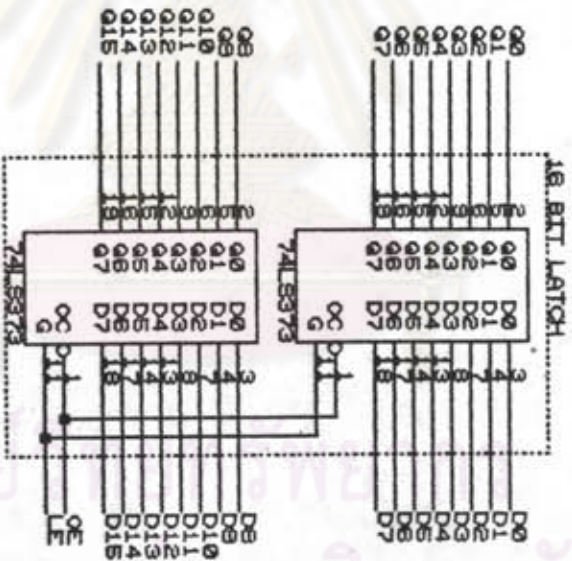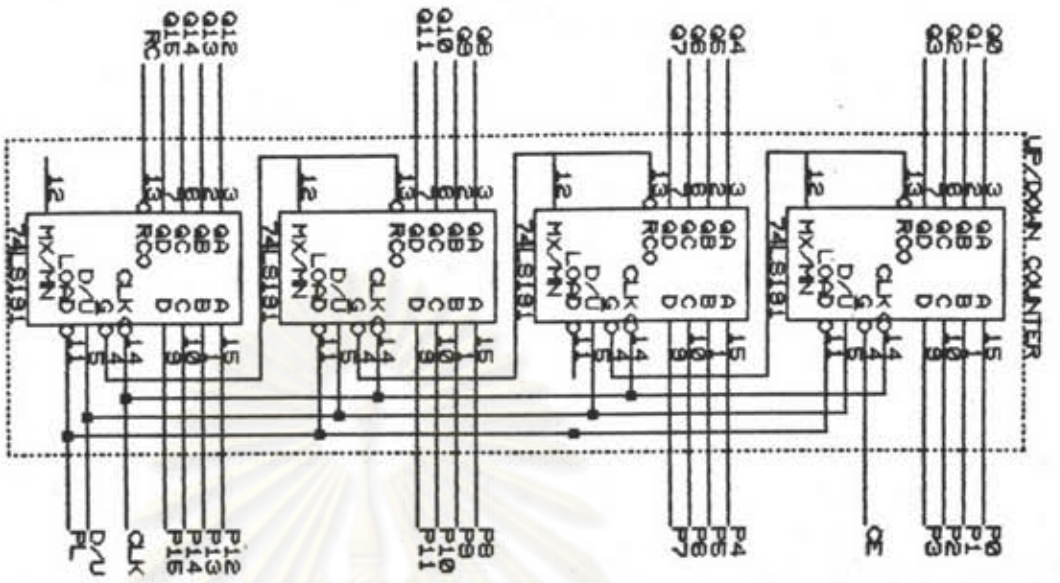
Fig.8-2 The main circuit of Pulse Programmer.

Fig.5-3 The circuits of binary counter (up/down) and 16-bit latch

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BINARY COUNTER (UP/DOWN) AND 16-BIT LATCH
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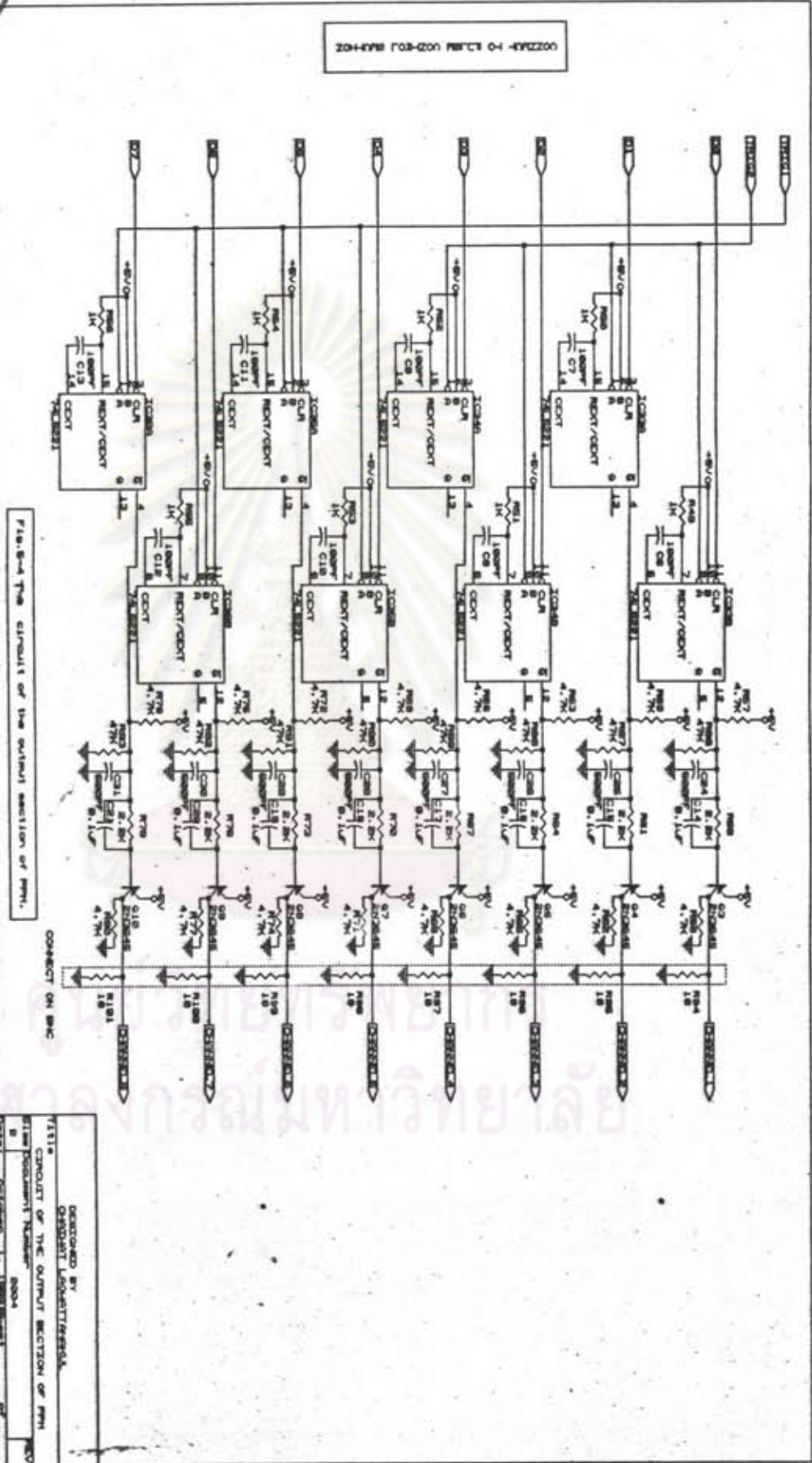
Fig.8-4 The circuit of the output section of PPH.

and IC30 for the low and the high order time, respectively. The third is stored in IC31 for the channels. It will repeat until receiving an ending code, the 3-byte zero. This ending code will be stored in IC29, IC30 and IC31 also. The GPIB interface will control the 8 to 24 bit latch to disable ($\overline{LE1}$, $\overline{LE2}$, $\overline{LE3}$ and $\overline{OE1}$ are high). It controls three memories (IC29, IC30 and IC31) to read state (W/R is high and $\overline{OE2}$ is low) after latching the last address of the address bus in the 11 bit latch. It resets binary count (up) to zero and loads binary count (down) with the last address from the 11 bit latch. D1 (data ready) is also lighted because the GPIB interface controls $\overline{LED1}$ to be low. At this time the GPIB interface is waiting the GPIB commands - such as gpsclr, gpaclr, gpsloc,..., etc. (see the GPIB commands in appendix A). If the GPIB command is the trigger command (gptrg), then the GPIB interface will generate the negative pulse on 'START' pin. This signal will be executed the pulse programmer.

The executing process of the pulse programmer

The negative pulse on 'START' pin is ANDed with signal, normally high, on $\overline{Q}$ of IC19B. This negative pulse can pass to the monostable 74121 (IC17). Then it will generate the negative pulse to flip the output $\overline{Q}$ of flipflop 74LS73 (IC19) to be low and to be ANDed by IC16A with signal, normally high, on RC pin of 16 bit binary counter (down). Consequently, the value on all data bus is loaded in the 16 bit binary counter (down). Since the output $\overline{Q}$ of flipflop 74LS73 (IC19) is low so $\overline{CE}$ pin of 16 bit binary counter (down) is low also. Then 16 bit binary counter (down) will begin count down. As the negative pulse from 74121 (IC17) is ANDed by IC16B with signal on RC pin of the 16 bit binary counter (down), the result is the negative pulse again, that is sent into two parts of this circuit. The first part is the output monostable will generate the trigger pulses on each channel depend upon the data bus of 6116 RAM (IC29). If some bits of channel bus are high and the negative pulse arrives at the output monostable then the related channels will release the trigger pulses. In the other word, if D0 is high and the negative pulse arrives at the output monostable then channel1

will release the trigger pulse. Similarly, if D7 is high and the negative pulse arrives at the output monostable then channel8 will release the trigger pulse. The second part is the address generator consists of binary counter (up), binary counter (down), 11 bit latch include a few AND gates, one buffer and one inverter. The receive negative pulse will be delayed a little time before increasing one address to binary counter (up) and decreasing one address to binary counter (down). This process will occur after the 16 bit binary counter (down) loads the value from the data bus because of the delay time. Consequently, the new value of the next address will be released on the data bus during the 16 bit binary counter (down) is counting the old value down. If the 16 bit binary counter (down) count the old value down until it is zero, then the negative pulse will released on the RC pin. This negative pulse will be sent to load the new value from the data bus by ANDing with the output of 74121 (IC17), normally high. It will be sent to the output monostable for generating the trigger pulses and will be sent to increase one address at the address generator also. This process will repeat until the binary counter (down) count the maximum address to zero. Then its RC pin will have the negative pulse. This negative pulse will be sent to clear the flipflop 74LS73 (IC19A). A $\overline{CE}$ pin of the 16 bit binary counter (down) goes to be high again. Since there is no signal from the 16 bit binary counter (down) so the 16 bit binary counter (down) will stop counting and the other parts will stop too. The RS flipflop (IC37B and IC37C) is used for 'rerun' mode. The JK flipflop (IC19B) is used for controlling the manual trigger button on the front panel key operation. The RS flipflop (IC37A and IC37D) and monostable 74121 (IC38) are used for eliminating the transient signal from SW1 when it is pressed. The LED2 is used for indication the execute state of the pulse programmer - 'rerun' mode or 'single run' mode.
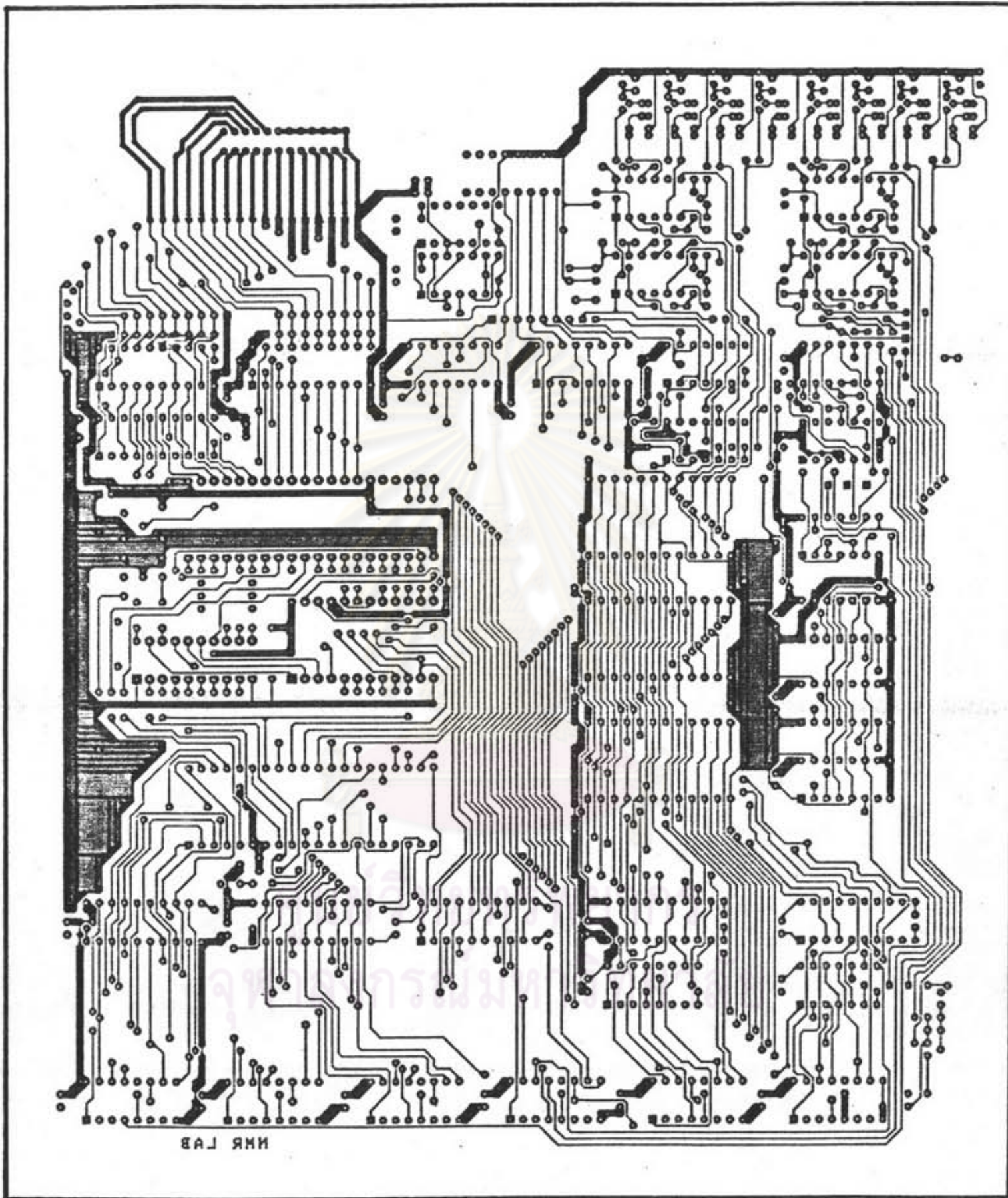
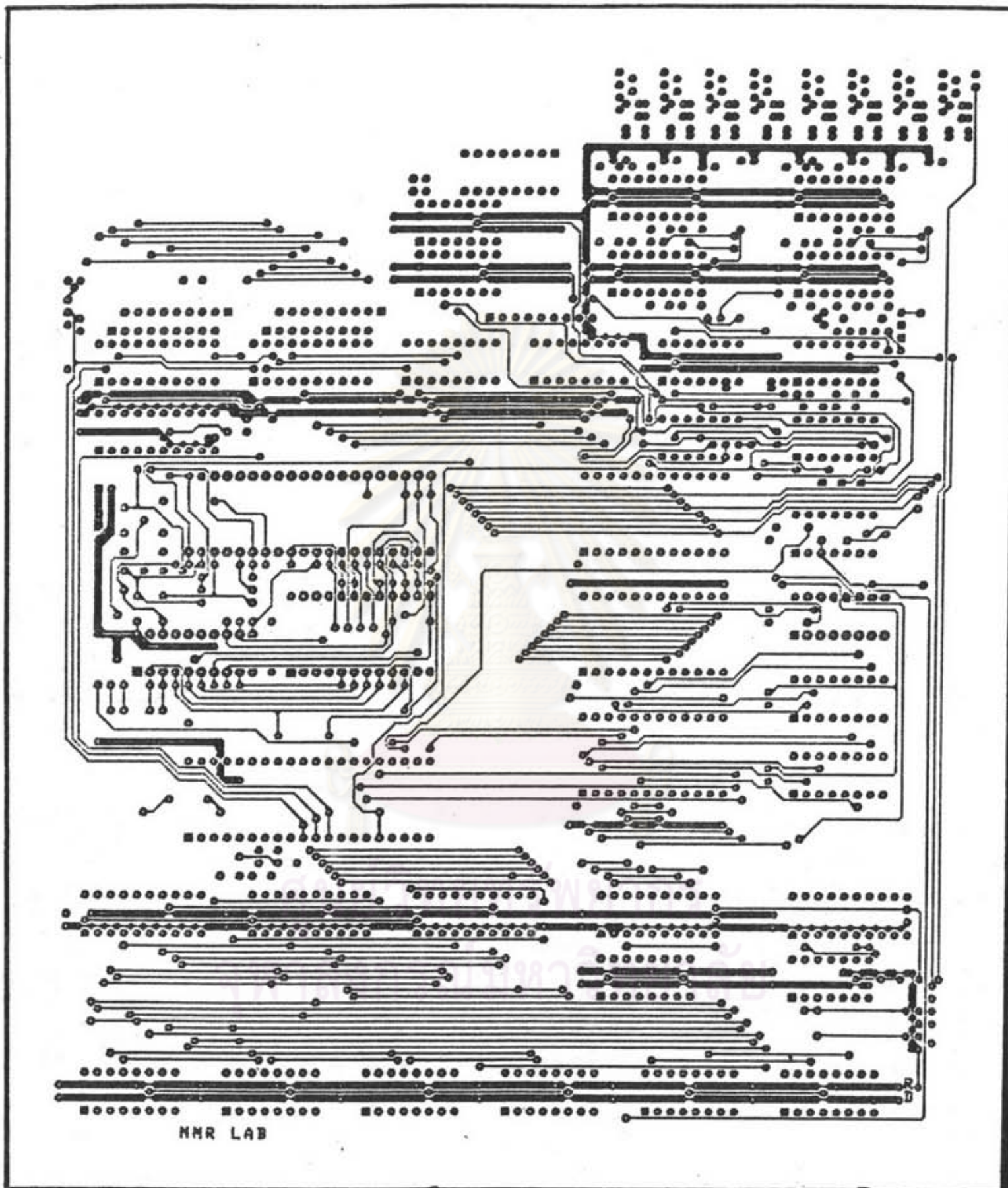Fig.5-5(a) The mirror of the solder side of the printed circuit board for PPM.

Fig.5-5(b) The component side of the printed circuit board for PPM.
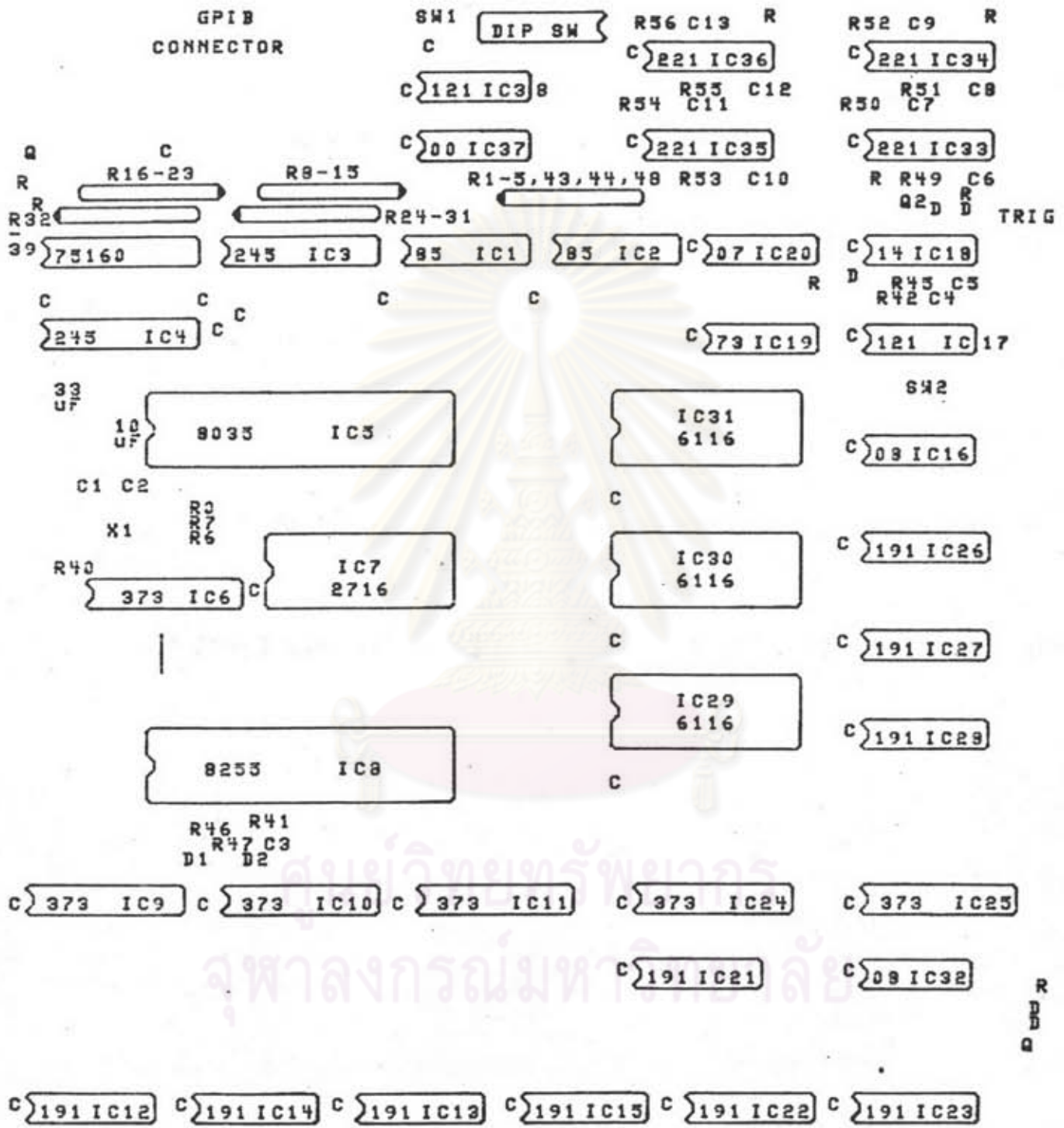
Fig.5-6 The component layout of PPM.
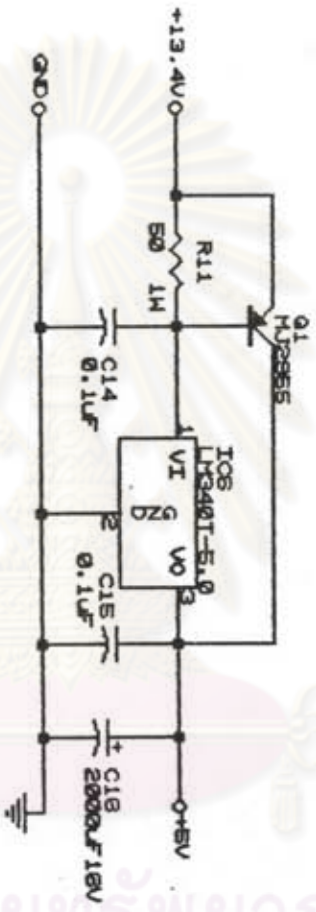
Fig.5-7 The circuit of regulator for PPM and PSP

+13.4V

GND

R11
50
1W

Q1
MJ2955

IC6
LM340T-5.0
VI G VO

C14
0.1uF

C15
0.1uF

C16
2000uF 16V

+5V

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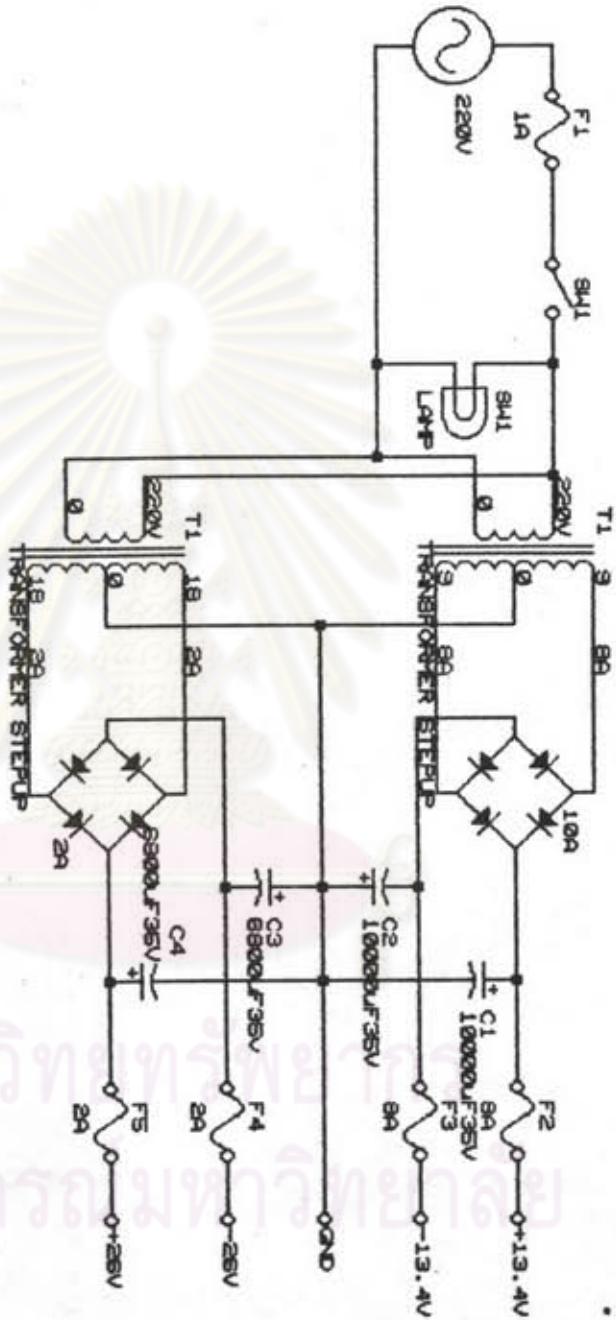Date: October 1, 1989 Sheet   of

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Fig.5-6 The Power Supply for PPM and PSP

POWER SUPPLY FOR PPM AND PSP

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POWER SUPPLY FOR PPM AND PSP

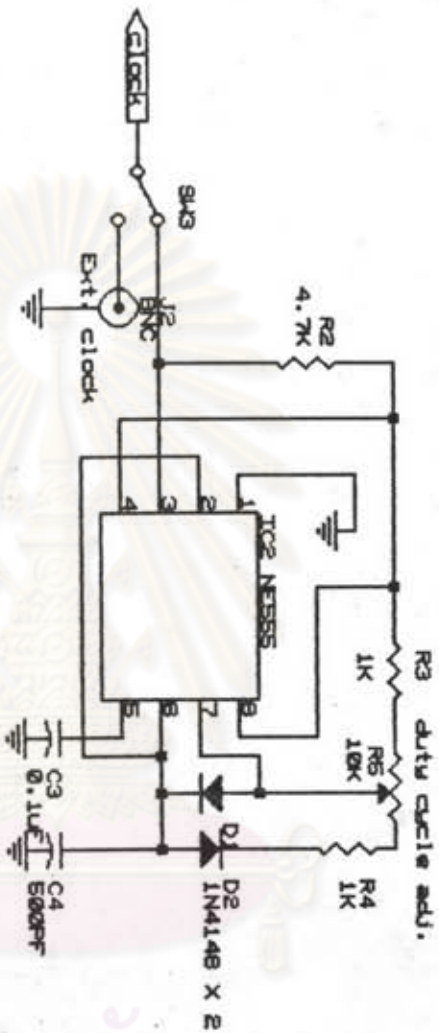Size Document Number
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Fig.5-8 The circuit of internal clock for PPM and PSP.

Title
INTERNAL CLOCK FOR PPM AND PSP

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Power Supply for the pulse programmer

Since the most elements of the pulse programmer is ICs TTL, so power supply of the pulse programmer is +5VDC. The pulse programmer circuit requires current at least 0.8 A. The power supply circuit of the pulse programmer is shown in Fig.5-7. It contains only the regulator, without transformer and rectifier. This transformer and rectifier are shown in Fig.5-8; they are separated in the another box. They are used for suppling to the pulse shaping circuit also.

Internal clock

The internal clock is used for the pulse programmer and the pulse shaping. It consists of IC 555. Its circuit is shown in Fig.5-9. It generates the square wave that has the duty cycle 50% at frequency about 128.5 KHz. Since its circuits use IC 555 so its generated frequency is not very precise, but can be used for NMR imaging.