

บรรณานุกรม

ภาษาไทย

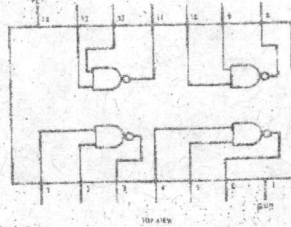
สมควร บูรมินเนนทร์, คร. ๒๕๑๓ Computer System เล่ม ๑, ๒ ศูนย์คอมพิวเตอร์
บัณฑิตวิทยาลัย จุฬาลงกรณ์มหาวิทยาลัย กรุงเทพฯ.

REFERENCES

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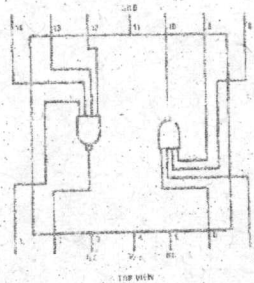
การเชื่อมต่อ ก.

Connection Diagrams ของ IC ที่ใช้



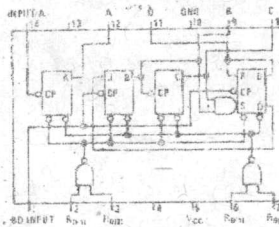
DM5400/DM7400(SN5400/SN7400)

quadruple 2-input NAND gate



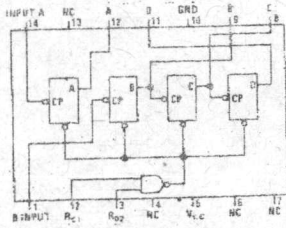
DM5420/DM7420(SN5420/SN7420)

dual 4-input NAND gate

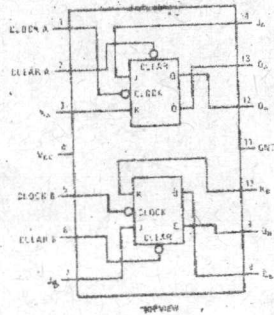


DM5490/DM7490(SN5490/SN7490)

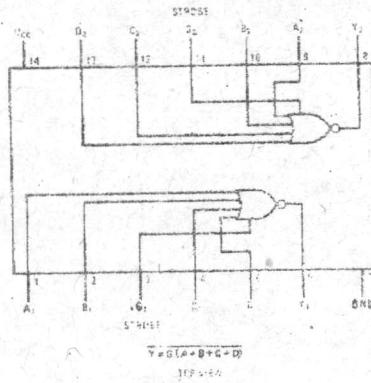
decade counter

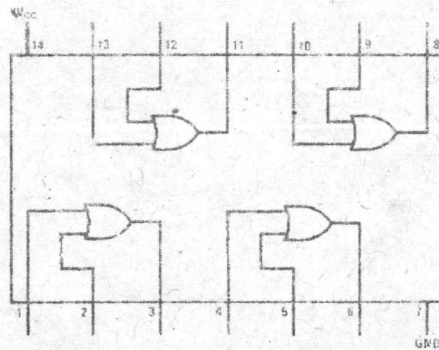


DM5493/ DM7493(SN5493/SN7493)
4 - bit binary counter



DM5473 / DM7473(SN5473/SN7473)
dual JK master/slave flip flop

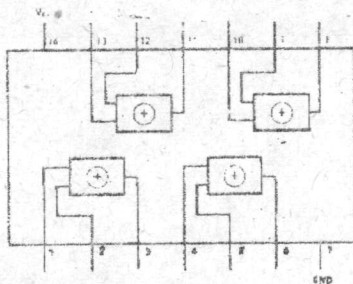




TOP VIEW

DM5432/DM7432(SN5432/SN7432)

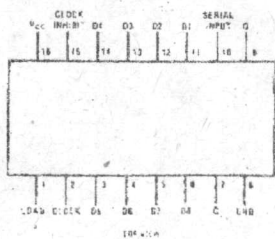
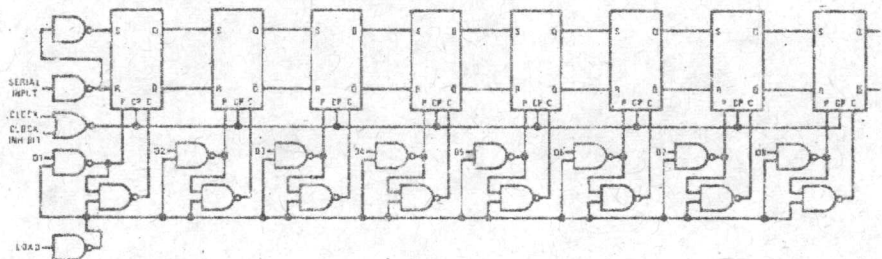
quad 2-input OR gate



TOP VIEW

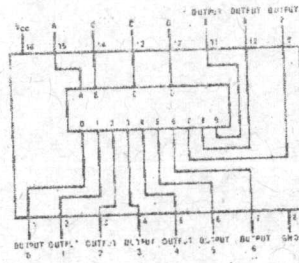
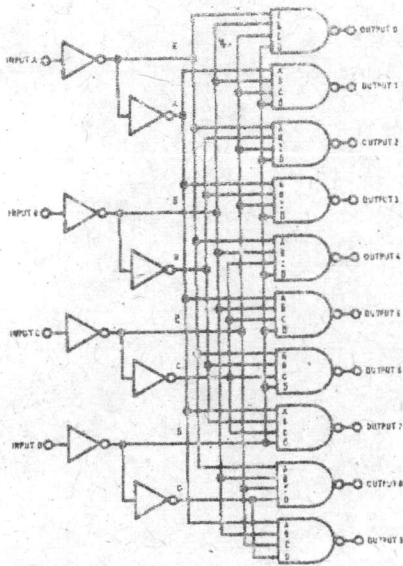
DM5486/DM7486(SN5486/SN7486)

quad EXCLUSIVE-OR gate



DM7590/DM8590(SN54165/SN74165)

8-bit parallel-in serial-out shift register



INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

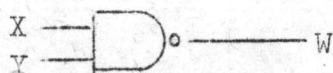
DM5442/DM7442 (SN5442/SN7442)

BCD-to-decimal decoder

ภาคผนวก ข.

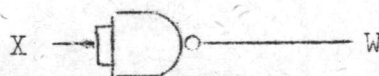
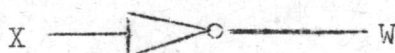
การทอวงจรและ Truth Table ของลอจิกที่ใช้

NAND Gate



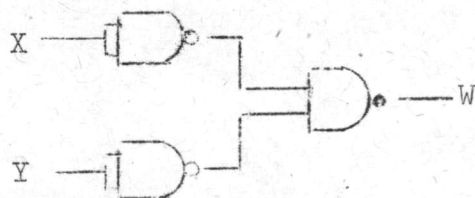
X	Y	W
L	L	H
L	H	H
H	L	H
H	H	L

Inverter (NOT Gate)



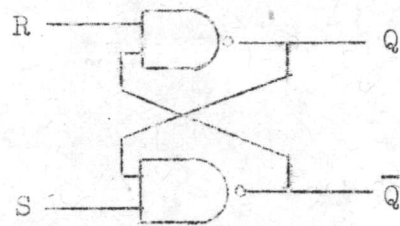
X	W
L	H
H	L

OR Gate



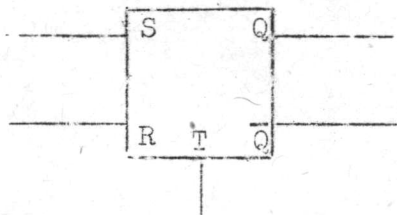
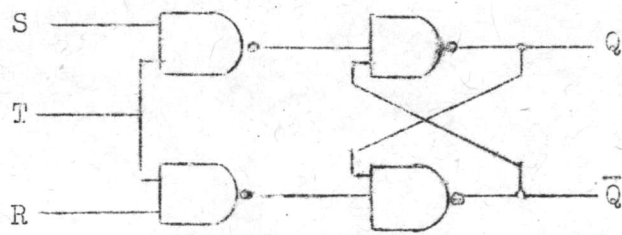
X	Y	W
L	L	L
L	H	H
H	L	H
H	H	H

RS Flip Flop



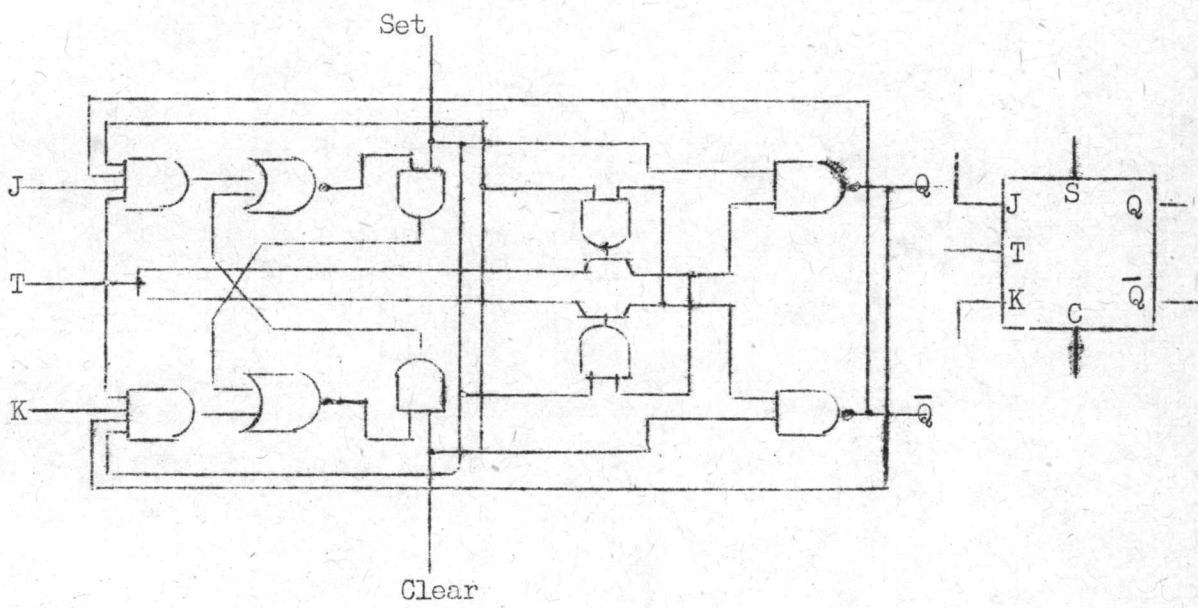
R	S	Q	\bar{Q}
L	L	H	H
L	H	H	L
H	L	L	H
H	H	Q	\bar{Q}

RST Flip Flop



R	S	T = 1	
		Q	\bar{Q}
L	L	Q	\bar{Q}
L	H	H	L
H	L	L	H
H	H	L	L

JK Flip Flop

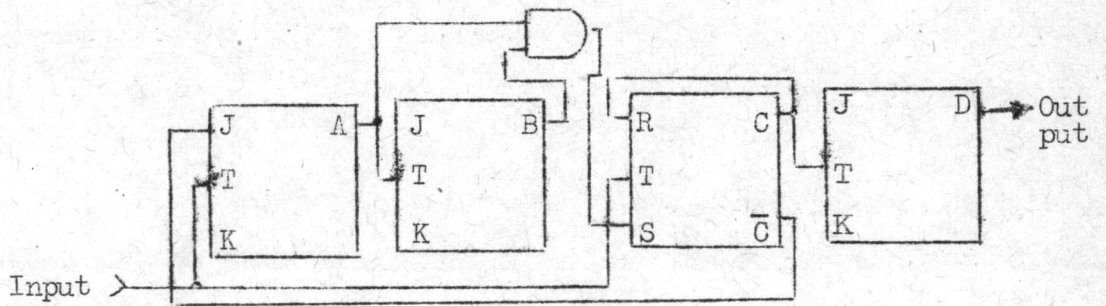


J	K	After Clk	
		Q	\bar{Q}
L	L	Q	\bar{Q}
L	H	L	H
H	L	H	L
H	H	\bar{Q}	Q

S	C	Q	\bar{Q}
L	L	?	?
L	H	0	1
H	L	1	0
H	H	Q	\bar{Q}

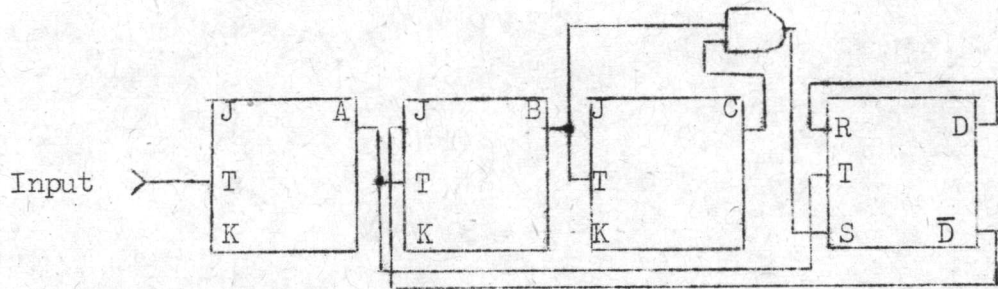
Divide-by-ten Counter

เมื่อมี Clock ทาง Input 10 Clock จึงจะทำให้ทาง Output มี Clock เกิดขึ้น 1 Clock



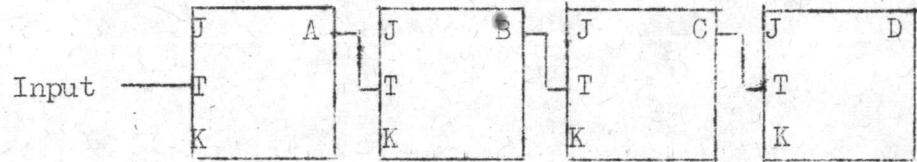
Clock	D	C	B	A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

BCD Decode Counter



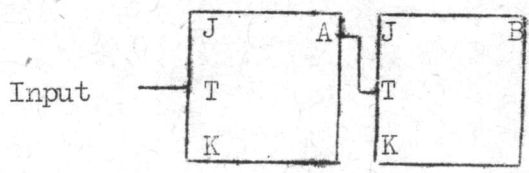
Count	D	C	B	A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

4-bit Binary Counter



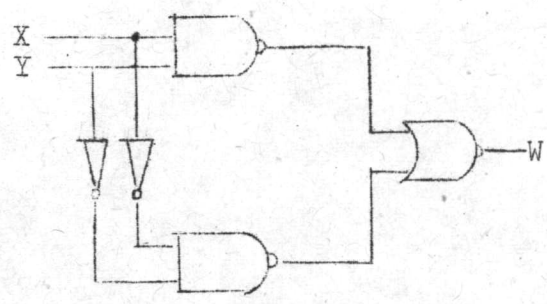
Count	D	C	B	A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

2-bit Binary Counter

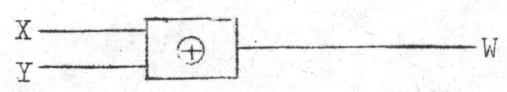
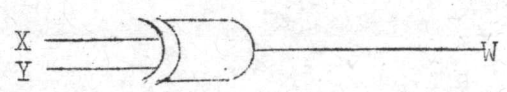


Count	B	A
0	L	L
1	L	H
2	H	L
3	H	H

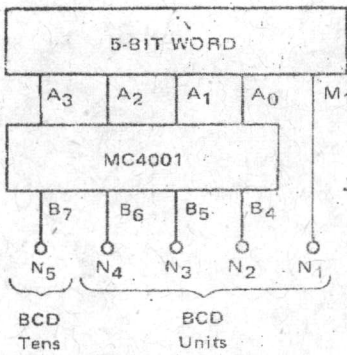
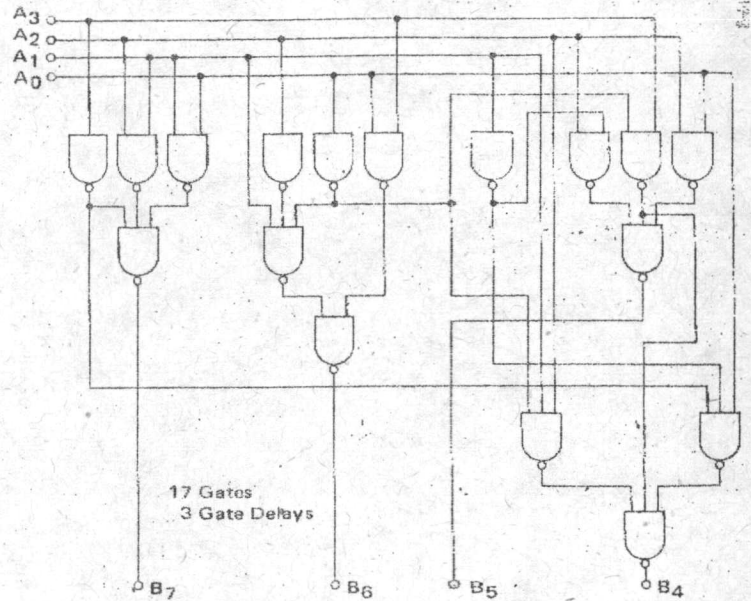
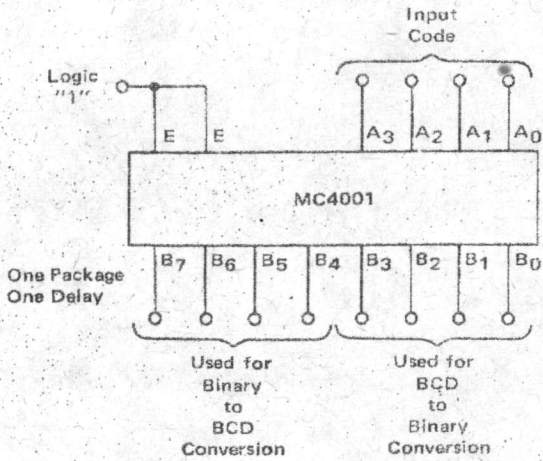
Exclusive - OR Gate



X	Y	W
0	0	0
0	1	1
1	0	1
1	1	0



ROM Binary/BCD Converter



Decimal Number	Binary Number					Tens Digit BCD Number				Units Digit BCD Number			
	M ₅	M ₄	M ₃	M ₂	M ₁	N ₈	N ₇	N ₆	N ₅	N ₄	N ₃	N ₂	N ₁
0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	0	0	1
2	0	0	0	1	0	0	0	0	0	0	0	1	0
3	0	0	0	1	1	0	0	0	0	0	0	1	1
4	0	0	1	0	0	0	0	0	0	0	1	0	0
5	0	0	1	0	1	0	0	0	0	0	1	0	1
6	0	0	1	1	0	0	0	0	0	0	1	1	0
7	0	0	1	1	1	0	0	0	0	0	1	1	1
8	0	1	0	0	0	0	0	0	0	1	0	0	0
9	0	1	0	0	1	0	0	0	0	1	0	0	1
10	0	1	0	1	0	0	0	0	1	0	0	0	0
11	0	1	0	1	1	0	0	0	1	0	0	0	1
12	0	1	1	0	0	0	0	0	1	0	0	1	0
13	0	1	1	0	1	0	0	0	1	0	0	1	1
14	0	1	1	1	0	0	0	0	1	0	1	0	0
15	0	1	1	1	1	0	0	0	1	0	1	0	1
16	1	0	0	0	0	0	0	0	1	0	1	1	0
17	1	0	0	0	1	0	0	0	1	0	1	1	1
18	1	0	0	1	0	0	0	0	1	1	0	0	0
19	1	0	0	1	1	0	0	0	1	1	0	0	1

Decimal Value of 5-Bit Word	MC4001													
	Address				Output									
	A ₃	A ₂	A ₁	A ₀	B ₇	B ₆	B ₅	B ₄						
0	0	0	0	0	0	0	0	0	0					
1	0	0	0	0	0	0	0	0	0					
2	0	0	0	0	1	0	0	0	0					
3	0	0	0	0	1	0	0	0	1					
4	0	0	0	1	0	0	0	0	1					
5	0	0	0	1	0	0	0	0	1					
6	0	0	0	1	1	0	0	0	1					
7	0	0	0	1	1	0	0	0	1					
8	0	1	0	0	0	0	0	1	0					
9	0	1	0	0	0	0	0	1	0					
10	0	1	0	1	1	0	0	0	0					
11	0	1	0	1	1	0	0	0	1					
12	0	1	1	0	0	1	0	0	0					
13	0	1	1	0	1	0	0	0	1					
14	0	1	1	1	1	0	0	1	0					
15	0	1	1	1	1	1	0	1	0					
16	1	0	0	0	0	1	0	1	1					
17	1	0	0	0	1	0	1	1	1					
18	1	0	0	1	1	1	1	0	0					
19	1	0	0	1	1	1	1	0	0					



ประวัติการศึกษา

นายภูดเกียรติ กรีพานิช จบการศึกษาระดับปริญญาตรี วิทยาศาสตรบัณฑิต (สาขาบริหาร) จากมหาวิทยาลัยมหิดล พ.ศ. ๒๕๑๐ ปัจจุบันรับราชการในตำแหน่ง วิทยากรโท สำนักนโยบายและแผน กรุงเทพมหานคร.

