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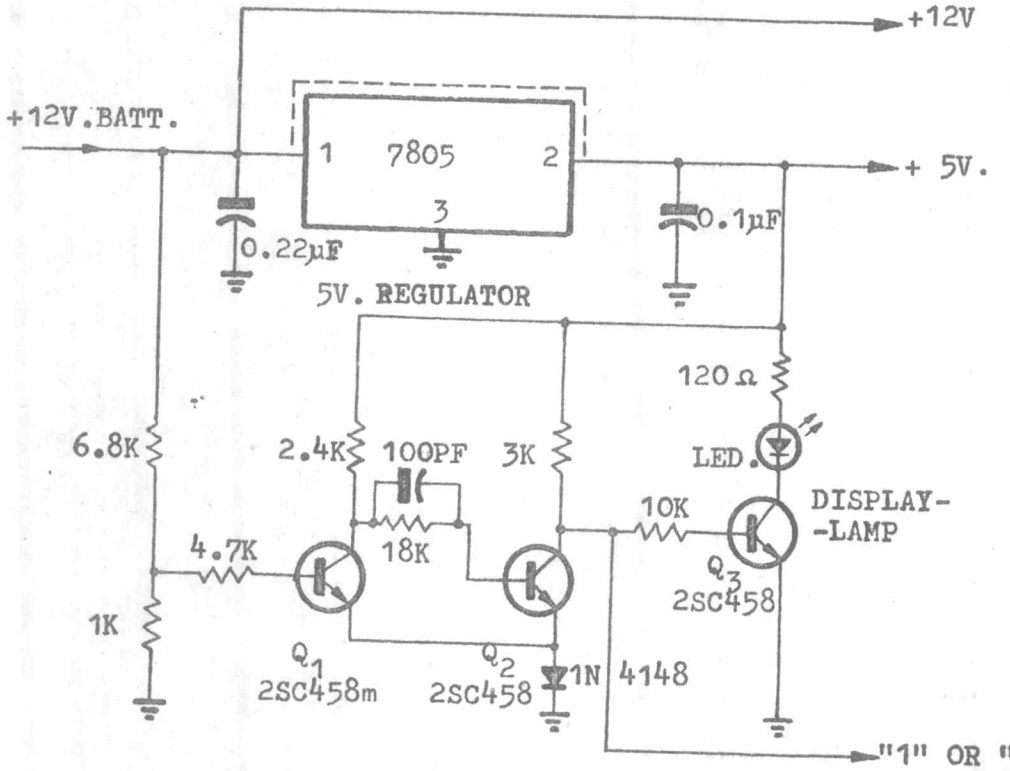
ภาคผนวก

ภาคผนวก ก.

วงจร Power Supply และวงจร Power Failure Decoder



POWER SUPPLY FAILURE DECODER

ภาคผนวก ข.

วงจร เครื่องพิมพ์ดีดโทรทัศน์ (๘)

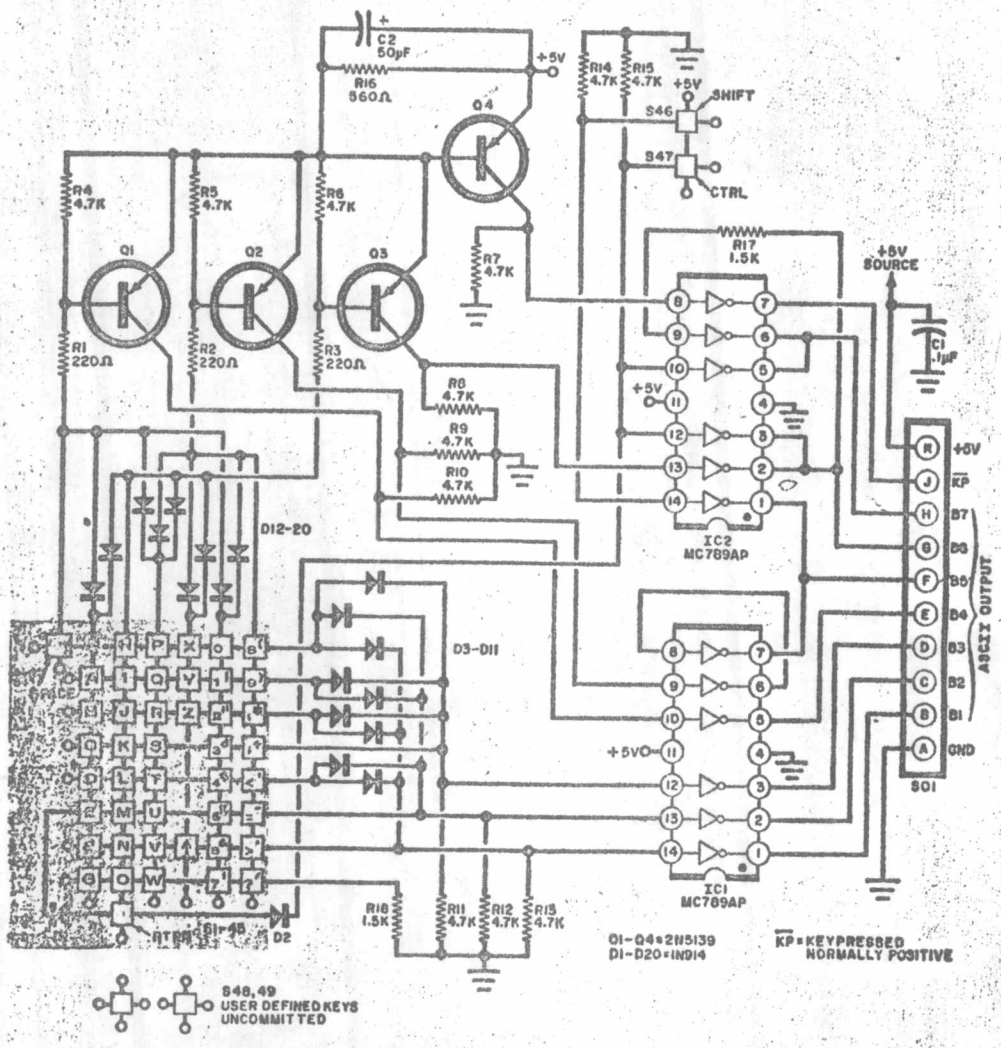


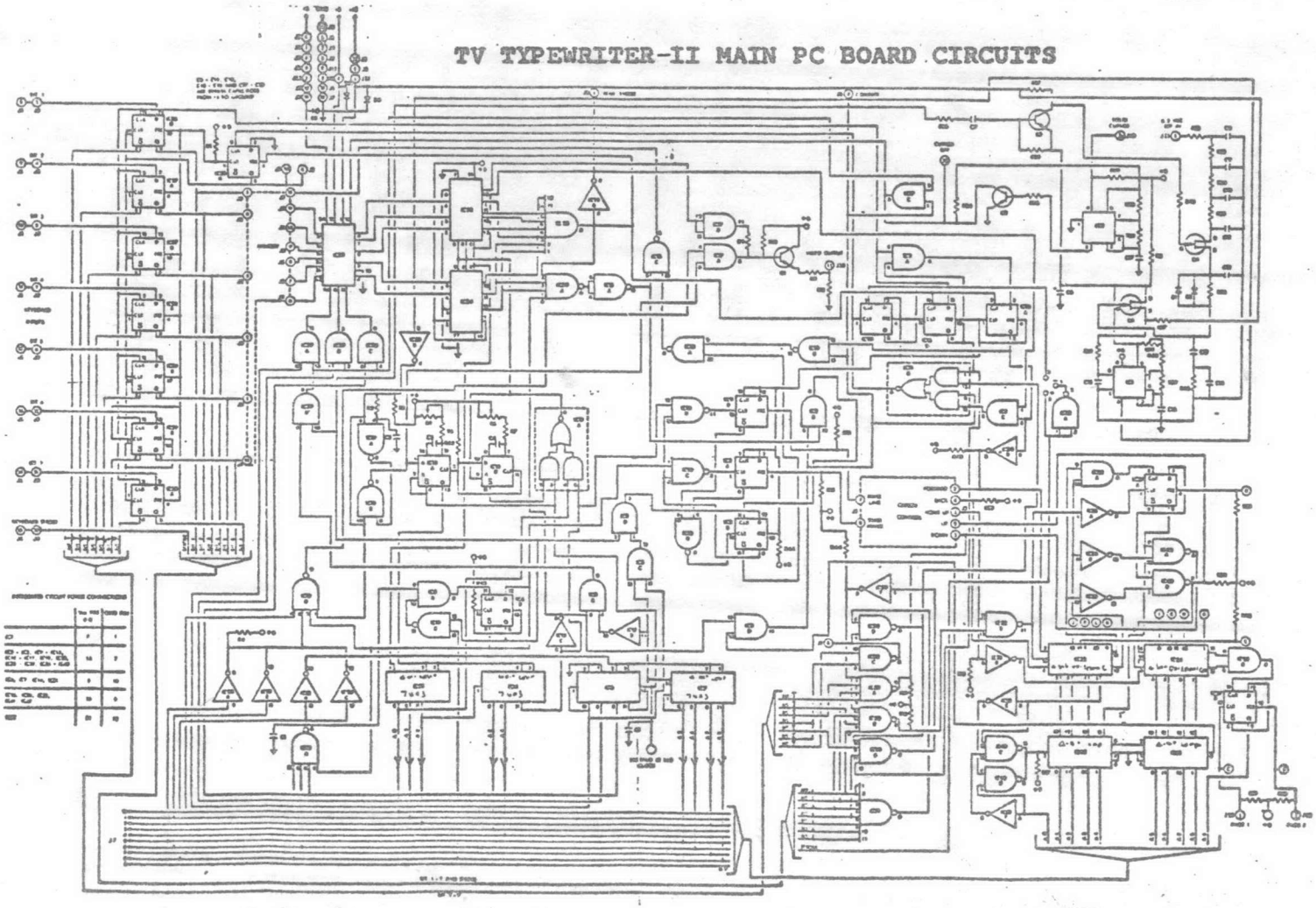
Fig. 1. The 48 keys are arranged in a 6-by-8 matrix as shown in block at lower left. The encoder, Q1 through Q4 and IC1 and IC2, provides the proper output.

PARTS LIST

C1—0.1-μF, 10-volt disc ceramic capacitor
C2—50-μF, 10-volt electrolytic capacitor
D1-D20—1N914 diode
IC1,IC2—MC789AP hex inverter (no substitute)
Q1-Q4—2N5139 transistor
R1-R3—220-ohm, ¼-watt resistor
R4-R15—4700-ohm, ¼-watt resistor
R16—560-ohm, ¼-watt resistor
R17,R18—1500-ohm, ¼-watt resistor
S1-S49—Keyswitches (Mechanical Enterprises LFW-CT)
SO1—Socket (Molex 09-52-3103)
Misc.—Keytops (two-shot molded) (shift and return are 1½ width); spacebar with equalizer and #2-56 mounting hardware; pc board (see text); #6 mounting hardware; solder; etc.

Note—The following are available from Southwest Technical Products, 219 W. Rhapsody, San Antonio, TX 78216: actual-size pc foil patterns and component installation diagram free on request; pc board, etched and drilled #Kb at $17.50; complete kit of all parts #KBC at $39.50 plus postage for 3 lb.

TV TYPEWRITER-II MAIN PC BOARD CIRCUITS



Parts List - TV Typewriter II Main Board

Integrated Circuits

IC1, IC8	NE555 timer
IC2, IC4, IC9, IC16, IC27	7474 dual "D" flip flop
IC36, IC37, IC38, IC39	7408 quad AND gate
IC3, IC5, IC28, IC29	7490 decade counter
IC6	7493 4 bit binary counter
IC7, IC14, IC21	7400 quad NAND gate
IC10, IC15	7451 dual AND-OR-INVERT gate
IC11	7404 hex inverter
IC12, IC33	7420 dual NAND gate
IC13, IC26	7409 quad AND gate (open collector)
IC17	74123 dual one shot
IC18	74132 quad schmitt NAND gate
IC19, IC32	7405 hex inverter (open collector)
IC20	2513 ASCII character generator
IC22	7495 4 bit shift register
IC23, IC24	7430 8 input NAND gate
IC25, IC31	7422 dual NAND gate (open collector)
IC30	74193 4 bit up/down counter
IC34, IC35	7403 quad NAND gate (open collector)
IC40	7485 4 bit comparator
IC41, IC42	

Resistors

R1, R2, R3, R9, R10, R13-R23, R26, R29, R42 - R48, R50	1K ohm 1/4 watt resistor
R4	20K ohm trimmer resistor
R5	5.6K ohm 1/4 watt resistor
R6	5K ohm trimmer resistor
R7	4.7K ohm 1/4 watt resistor
R8	100 ohm 1/4 watt resistor
R11	47 ohm 1/4 watt resistor
R12	100 ohm 1/4 watt resistor
R24, R25, R28, R30, R31	4.7K ohm 1/4 watt esistor
R27, R32-R35, R37	10K ohm 1/4 watt resistor
R36, R49	2.2M ohm 1/4 watt resistor
R38	50K ohm trimmer resistor
R39, R41	33K ohm 1/4 watt resistor
R40	220K ohm 1/4 watt resistor
R41	33K ohm 1/4 watt resistor

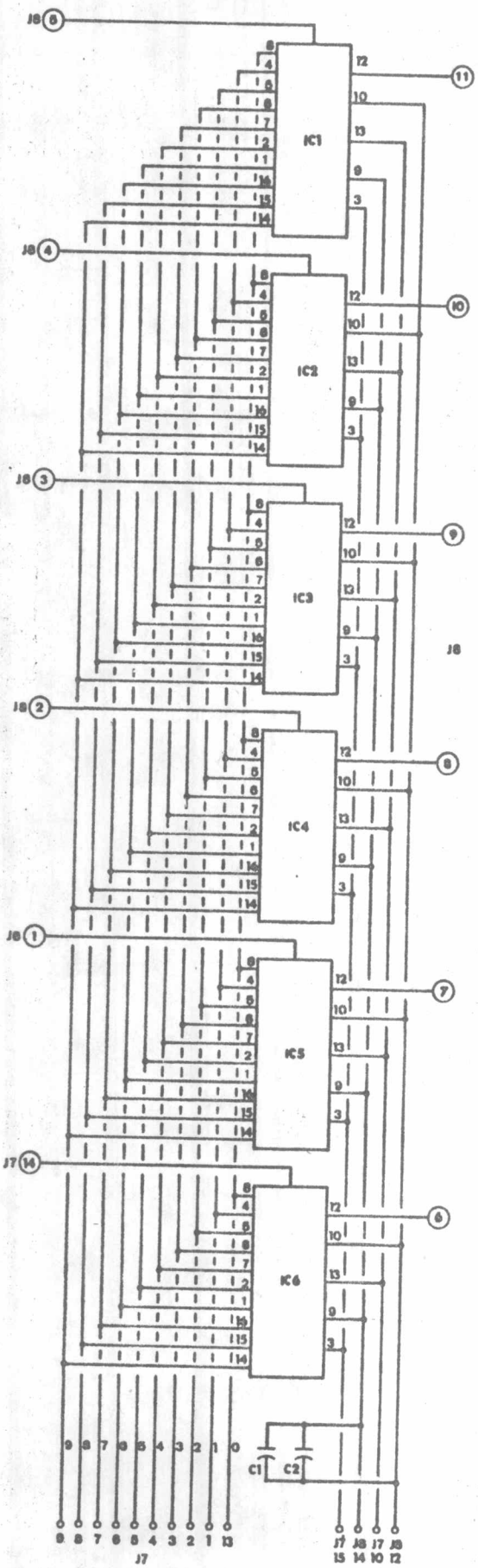
Capacitors

C1, C5	470 pfd capacitor
C2, C7, C14	0.01 mfd capacitor
C3	0.0033 mfd disc capacitor
C4	39 pfd capacitor
C6, C34	100 mfd @ 16 VDC electrolytic capacitor
C8, C9, C10, C11, C15, C18 - C24, C27 - C33	0.1 mfd mylar capacitor
C12	0.1 mfd (cermaic disc capacitor)
C13	0.047 mfd capacitor
C16	0.22 mfd mylar capacitor
C17	0.001 mfd capacitor
	33 mfd @ 25 VDC electrolytic capacitor

Transistors and Diodes

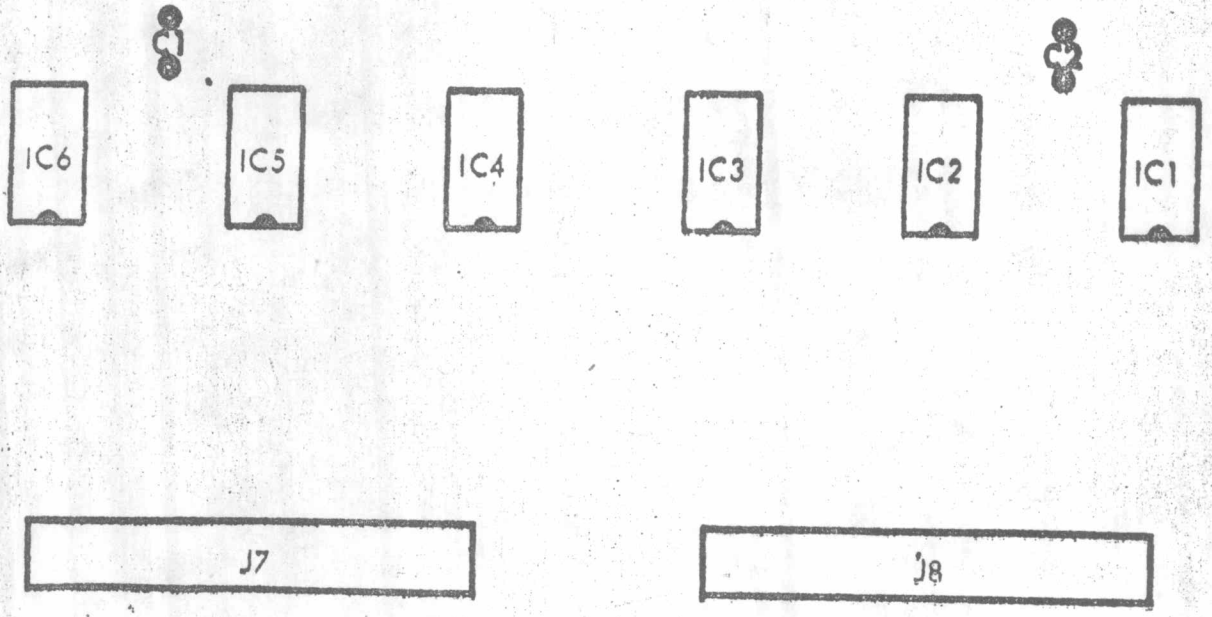
Q1, Q2	2N5129 silicon transistor
Q3	2N5139 silicon transistor
Q4, Q5	TIS58 field effect transistor
D1, D2	1N914 silicon diode
D3 - D5	1N5060 silicon diode

TV TYPEWRITER II - Memory Board Schematic

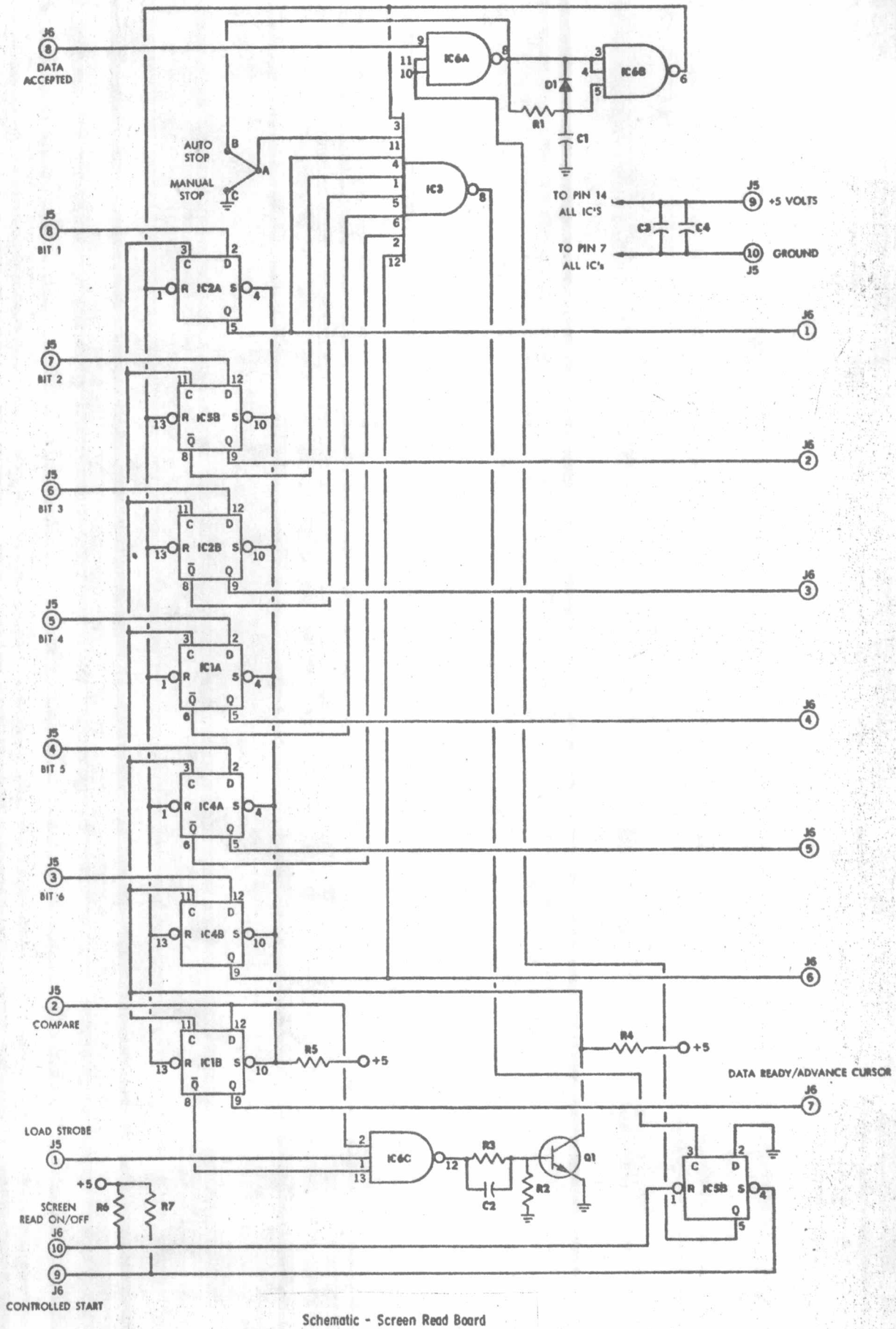


Parts List - TV Typewriter II Memory Board

IC1 - IC6	2102 1024 bit static RAM
C1, C2	0.1 mfd capacitor



Component Layout CT-1024 Memory Board



Schematic - Screen Read Board

Parts List - Screen Read Board

Resistors

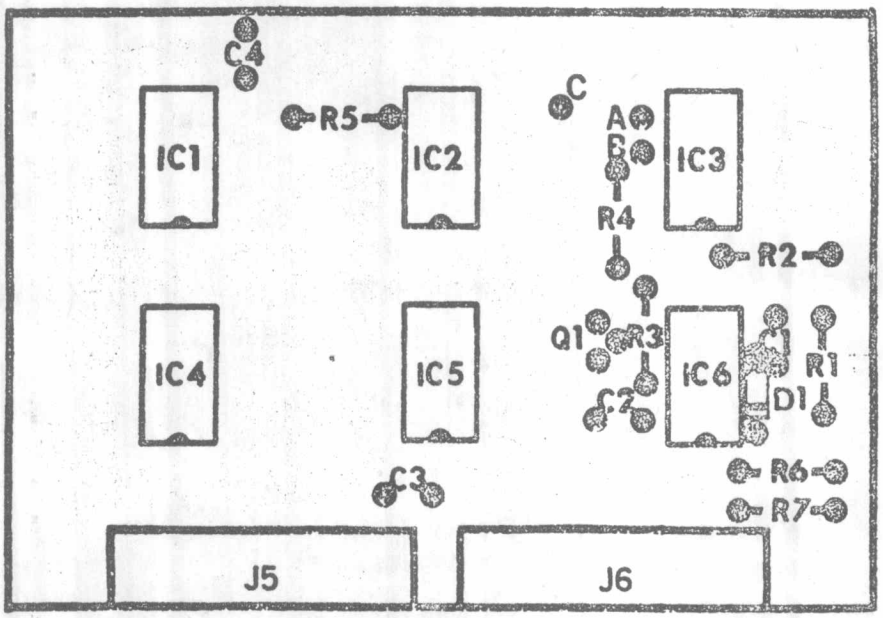
R1, R3-R7	1K ohm 1/4 watt resistor
R2	4.7K ohm 1/4 watt resistor

Capacitors

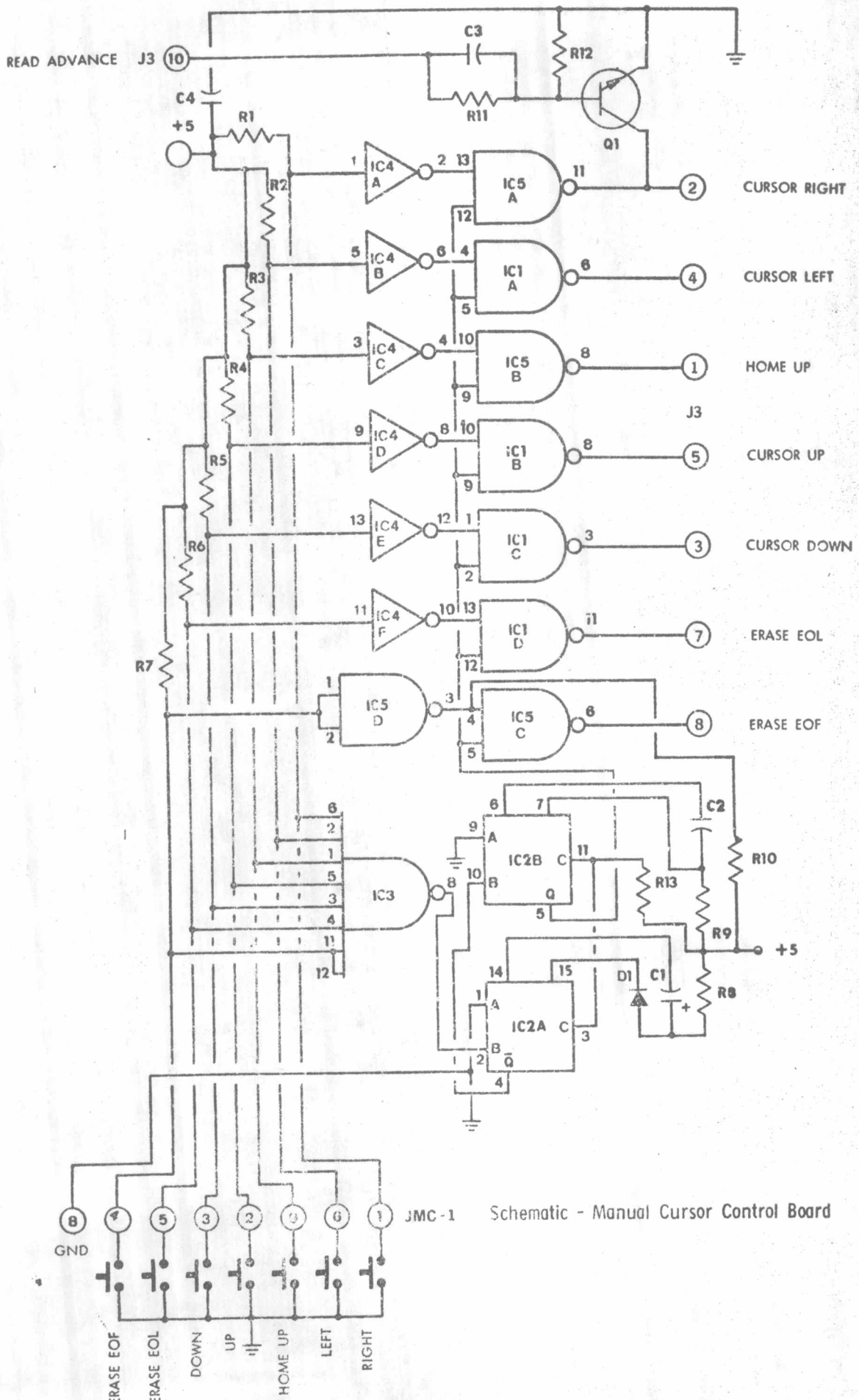
C1	100 pfd polystyrene capacitor
C2	1000 pfd polystyrene capacitor
C3, C4	0.1 mfd capacitor

Semiconductors

D1	1N914 silicon diode
Q1	2N5129 transistor
IC1, IC2, IC4, IC5	7474 dual D flipflop
IC3	7430 eight input NAND gate
IC6	7410 triple 3 - input NAND gate



PC Top Layout - Screen Read Board



Schematic - Manual Cursor Control Board

Parts List - Manual Cursor Board

Resistors

R1 - R7, R10, R12, R13	1K ohm 1/4 watt resistor
R8	5.6K ohm " " "
R9	5.6K ohm " " "
R11	2.2K ohm " " "

Capacitors

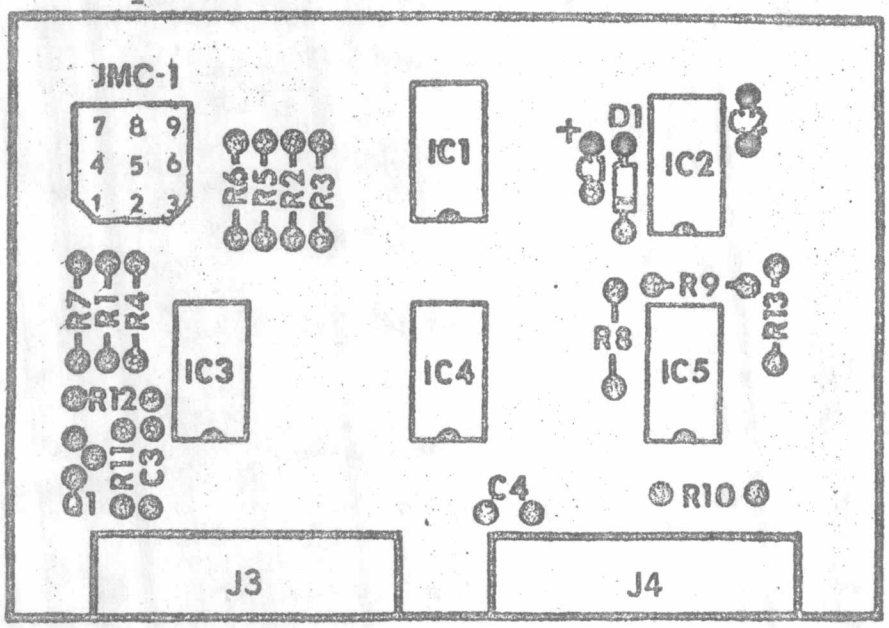
C1	33 mfd @6 VDC electrolytic capacitor
C2, C3	100 pfd polystyrene capacitor
C4	0.1 mfd capacitor

Semiconductors

D1	1N914 silicon diode or equiv.
IC1, IC5	7403 quad NAND gate (open collector)
IC2	74123 dual one shot
IC3	7430 8 input NAND gate
IC4	7404 hex inverter
Q1	2N5129

หมายเหตุ C_1 ใช้ 33 µF 25V แทน

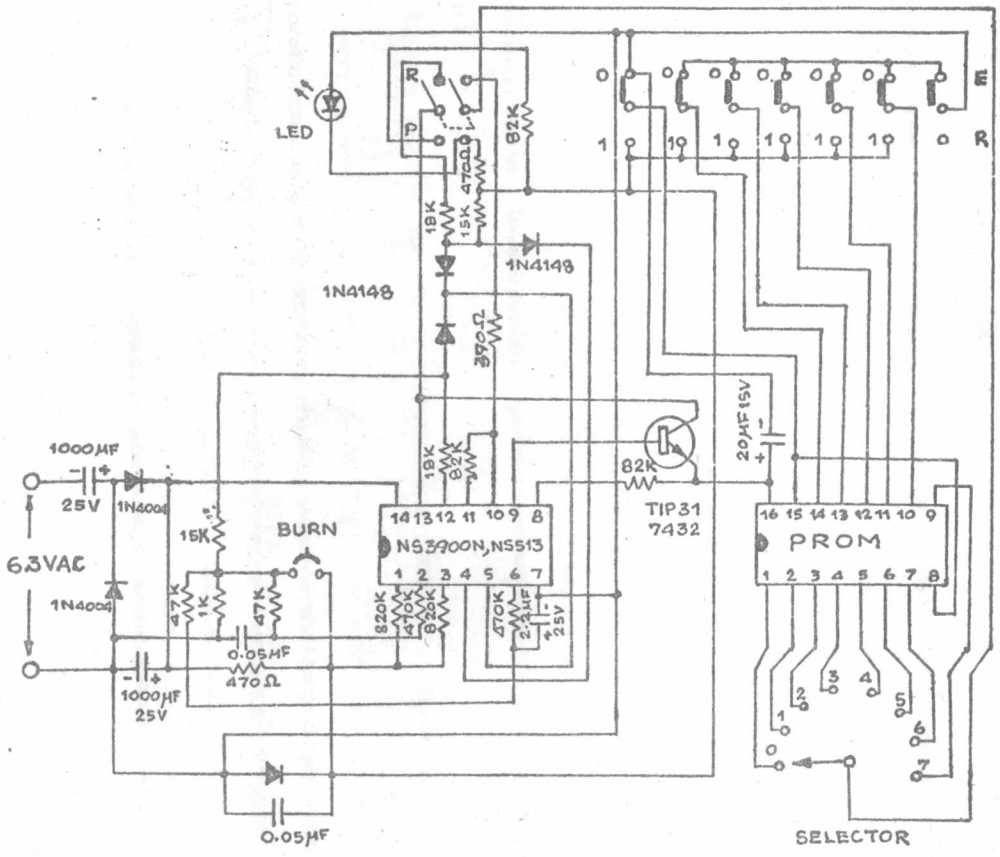
D_1 ใช้ 1N4148 แทน

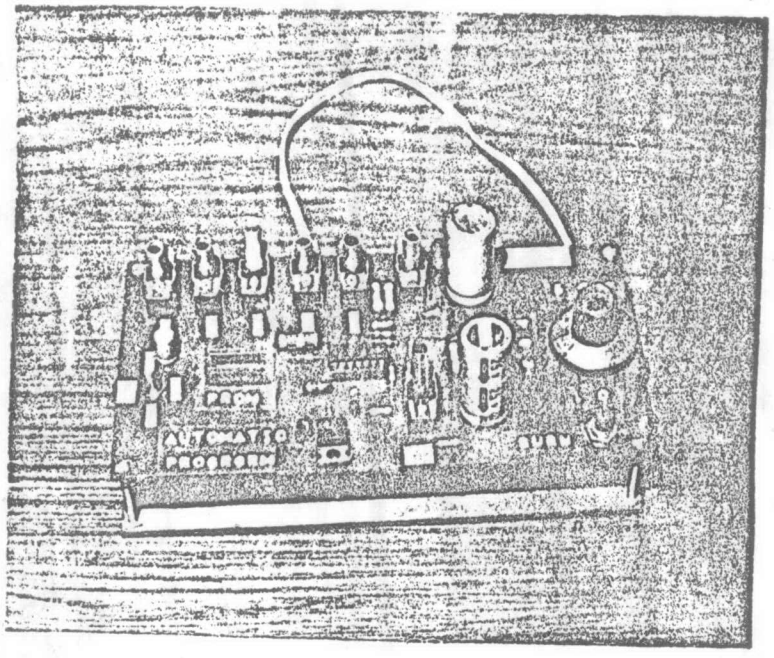


PC Top Layout - Manual Cursor Board

ภาคผนวก ค.

วงจรสำหรับโปรแกรม ไอ.ซี.แบบ PROM



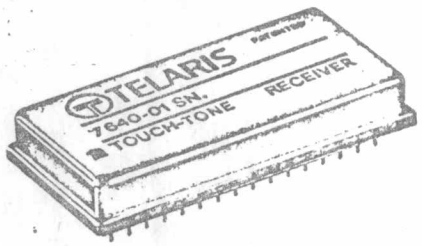


เครื่องโปรแกรม ไอ.ซี. แบบ PROM

ภาคผนวก ง.

MFP. Encoder

TELARIS
Telecommunications, Inc.



Model 7640-01

Touch-Tone Receiver*

The 7640 is a sub-system that converts analog touch-tone signals into digital logic level outputs for use in communications and data systems. Contained within a 32 pin dual-in-line package, the 7640 combines a multi-layer thick film hybrid design with a P-MOS LSI digital tone detector. The whole package occupies less than a ½ cubic inch and requires only the addition of an external crystal for operation.

Touch-tone input signals may be balanced or single ended in a range of −26 to +6 dBM. D.C. blocking capacitors are provided and the balanced input impedance is 86K ohms. Operates from single 10 to 14 volt supply. Outputs are MOS compatible.

DESCRIPTION

Telaris Model 7640 is a Touch-Tone Receiver designed for general telephone office and PBX use. It combines Telaris thick film hybrid circuits with the Collins CRC8030 digital DTMF detector to achieve an immunity to talk-off that is superior to any touch-tone receiver available.

The 7640 is a complete sub-system comprised of a balanced input buffer amplifier, a dial tone reject filter, high and low group band separation filters, level comparators, two limiters, a supply divider, and the digital P-MOS DTMF detector. It requires only an external 3.58MHz crystal to operate, has a 32 dB dynamic range, operates from a single power supply, and is MOS compatible. The line bridging input is balanced, DC blocked, and of high impedance. The output is pin selected to either a "modified" hexadecimal binary or 2-of-8 code format. Three signal to noise ranges may be pin programmed and the detection of the special function frequency (1633Hz) may be inhibited when desired.

* Touch-Tone is a registered mark of AT&T

OPERATION

A unity gain input amplifier buffers the filters providing a balanced input with common mode noise rejection of 60dB. D.C. blocking capacitors with a 50 WVDC rating provide the interface to the line. Single ended operation is achieved by connecting pin 4 to ground.
The first filter section is a high pass configuration with an Fc of 680Hz. This filter attenuates precise dial tone signals of 350 and 440Hz along with other frequencies below 680Hz. Band separation is accomplished with a lowpass and a highpass filter pair. Their outputs feed limiters which set the input sensitivity of the receiver. The threshold limiter function is accomplished by comparing the output of the filter with a fixed reference. The reference is a voltage divider connected between (+)VS and (+)VS − (−)VS/2. The limiter output provides a squared signal with a voltage swing from the negative supply rail to within −1V of the positive supply rail to operate the digital detectors.
The 7640's DTMF Detector employs a digital matched filter based on a unique autocorrelation algorithm. Detection of valid signals takes 22 to 39mS depending on the accuracy of the frequencies presented and the relative incidence of interference (absence of correlation). If correlation is not achieved in the time programmed the output is inhibited until the input has cleared and the process repeated. The device ignores the first few sine waves of the Touch-Tone sender. The signal is then analyzed several times by the digital range filter prior to being accepted as valid. A strobe output provides a momentary indication that valid data is present at the data lines. For improved signal recognition on noisy circuits the strobe output may be ignored.
Once a digit is valid the 7640 ignores any change in signal frequency until either the high or low group signal disappears for more than 12mS. When this occurs the unit is reset internally and ready to accept a new digit.
Interruptions of either one or both of the signal frequencies for less than 12mS are bridged and the data line outputs are undisturbed.

DIGITAL INPUTS

Bin Select

Operation is such that when the 2-of-8 output format is allowed (the BIN SELECT, pin #17, is left open) the strobe and data lines, pins 22 through 30, display data with negative true logic. But when the binary output format is selected (BIN SELECT, pin #17, is held Lo) the STROBE and data lines, pins 22 through 26, display data with positive true logic.

Output Hold

This input may be held low to latch the data line output registers when data is received. See Fig. 6 for output hold operation timing.

RxMute

While this input is held low, the detector is inhibited from analyzing input signals. Operation of RxMUTE in combination with the OUTPUT HOLD is a master reset on device outputs. If the OUTPUT HOLD LINE is enabled, the data lines will not reset. See Fig. 6 for inhibit operation timing.

Silence Reset

This output pulses low when silence is detected. This occurs 9mS after the interruption of signal on either the high or low group limiter outputs (pins #10 and #13) or about 20mS after the loss of signal at the receivers input. Refer to Fig. 6

Auxiliary Clock

This output may be used as a time base for the operation of ancilliary systems such as a dial pulse converter. The output frequency is 32KHz ± 0.1%.

Performance Specifications, Model 7640-01 Touch-Tone Receiver

PARAMETER	CONDITION	MIN	TYPICAL	MAX	UNITS
Input Level, High	Each Tone Freq. Comp.	+6		+8	dBm
Input Level, Low	Each Tone Freq. Comp.	−28		−26	dBm
Input Impedance	Balanced		86		k ohm
Input Impedance	Unbalanced		43		k ohm
Dial Tone Rejection	Note 1	36			dB
Twist	Hi/Lo grp. Lo/Hi grp			12	db
Guard Time, Long Strobe	Note 2			39	mS
Guard Time, Short Strobe	Note 2			33	mS
Fault Time	Note 3		20	25	mS
In Band Tone Rejection	Note 4		17		dB
Invalid Tone Reject Limit	Tones Pulsed	−3.5		+3.5	%
Tone Pair Duration, Invalid				20	mS
60 and 120 Hz Rejection		40			dB
Common Mode Rejection	Balanced Input	40	60		dB
Signal to Noise Ratio	3kHz White Noise, Long Strobe		18		dB
Signal to Noise Ratio	3kHz White Noise, Short Strobe		22		dB
Signal to Noise Ratio	3kHz White Noise, No Strobe		14		dB
Talk-Off (Speech Simulations)	Long Strobe, Note 5		2	10	HITS
D.C. Input Blocking Voltage	Pin 1 or 4 to ground			50	Volts
Operating Voltage	(+)Vs — (−)Vs	10	12	14	Volts
Operating Current			50		mA
Operating Temperature		0		+70	C
Storage Temperature		−30		+85	C
Input Clock (Crystal)		−.005%	3.579545	+.005%	MHz
Output Level, Logic "1"	1 Source = 2.0 mA	(+)VS − 0.4			Volts
Output Level, Logic "0"	1 Sink + 25 μA			−VS +0.3	Volts
Output Rise or Fall Time	10% to 90% of total (w/30pFload)			4	μS
Detected Frequencies, Lo Group			697		Hz
			770		Hz
			852		Hz
			941		Hz
		−3.2%	1209	+3.3%	Hz
Detected Frequencies, High Group			1336		Hz
			1477		Hz
			1633		Hz
Strobe Duration, Long		10		17000	μS
Strobe Duration, Short		10		8000	μS
Interdigit Interval		25			mS
Data Rate	Long Strobe			15	PPS

Notes:

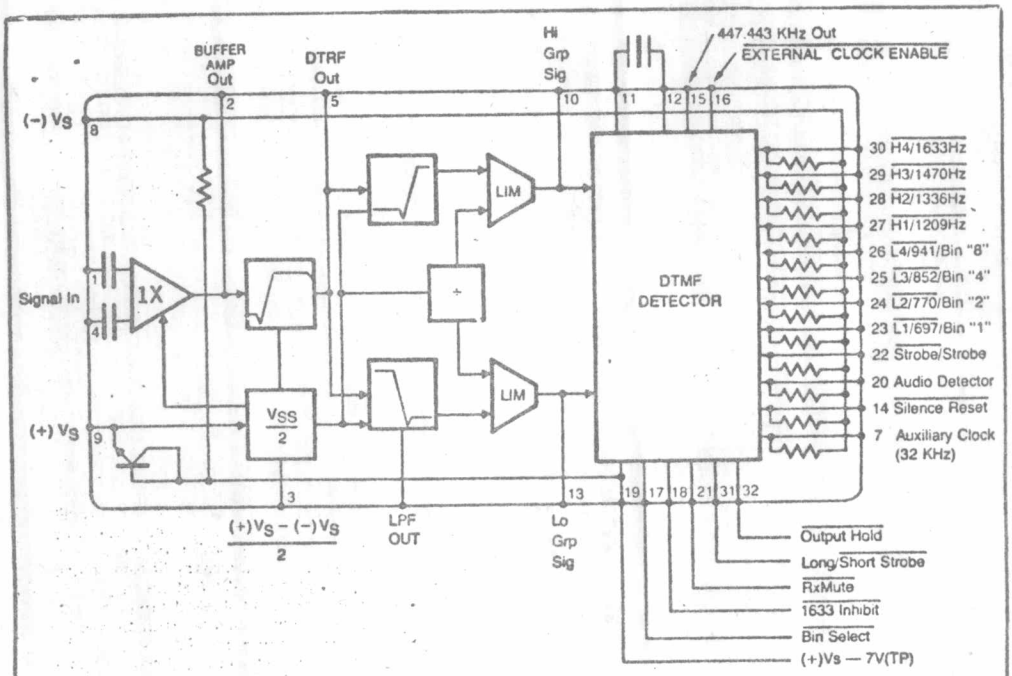
1. Precise dial tone (350-440 Hz) present at −10 dBm.
2. Guard time is defined as the receiver response time to a tone input pulse. (See strobe control option)
3. Fault time is the time a tone pulse may be interrupted without the receiver output reseting.
4. Third frequency is 1700 Hz 4000 Hz and −1 dB with respect to high group tone.
5. Based on Mitel test tape (CM 7290). Equivalent to 100 hrs exposure to speed signals. Long Strobe selected.

Timing. Refer to the timing diagram Fig 6

t SP	Silence Period	9.4	10	10.6	ms
t R	Silence Pulsewidth	1.0	1.1	1.2	ms
t DA1	Data Acquisition Time Long Strobe	22		39	ms
t DA2	Data Acquisition Time Short Strobe	25		33	ms
t H	Output Hold Set-Up Time	10			μS
t INH	Chip Inhibit Pulsewidth	2			μS
t S1	Long Strobe Pulsewidth	10		17000	μS
t S2	Short Strobe Pulsewidth	10		8000	μS
t AUD	Audio Det. Time	1.5	5	8	ms

Timing of digital outputs shown are referenced to detector inputs (pins 10 and 13), not receiver input.

Fig. 2



7640 BLOCK DIAGRAM

Fig. 1

Strobe Control

Normal operation, with pin #31 left open (long strobe) allows the 7640 to analyze and qualify the input signal for a maximum of 39mS. The duration of the strobe pulse (pin #22) will range from a minimum of 10μS to a maximum of 17mS depending on the difficulty experienced achieving correlatable data. This yields a signal to noise performance of 18dB. If correlation is not achieved in 39mS no STROBE pulse will occur.
Talk-off immunity may be improved by holding the STROBE CONTROL, pin #31, low (short strobe). This reduces the period allowed for an incoming signal to be analyzed and qualified to maximum of 33mS. The duration of the STROBE pulse then ranges from 10μS to a maximum of 8mS. If correlation is not achieved in 33mS no STROBE pulse will occur. A signal to noise performance of 22dB results.
If the STROBE line is ignored, a signal to noise performance of 14 dB results.

Clock

Clock inputs, pins #11 and #12, are connected to a 3.57954MHz parallel resonant crystal. The lead length for this connection must be kept short. As an alternative an external oscillator operating at a frequency of 447.443kHz can be used, in which case pin #12 becomes the 447.443kHz input and pin #16 is held low. Pin #11 is then left open. In this way a master unit can supply the clock for several slaves.

1633 Inhibit

Normal operation processes the special function signal frequency of 1633Hz. If not required, detection of 1633Hz may be inhibited by holding pin 18 low.

Digital Outputs

All the output devices of the DTMF detector have pull down resistors (10k ohm ± 20%) tied to the negative supply. This includes all eight data lines (pins 23 through 30), the STROBE LINE (pin 22), and the AUXILIARY CLOCK (pin 7), SILENCE RESET (pin 14), and the AUDIO DETECT (pin 20). These outputs are directly compatible with MOS logic families.

Data Lines

The decoded outputs are displayed on the data lines (pins #23 through #30) in either the 2-of-8 or binary format. Refer to the truth table, figure 4.

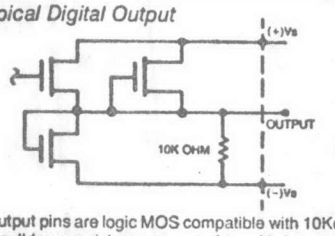
Strobe

The strobe line (pin #22) output indicates when the output data are valid. Refer to the timing diagram, figure 6.

Audio Detect

The AUDIO DETECT line (pin #20) output indicates when signal energy in the band above 680 and below 1680Hz is present following a detection delay ranging from 5 to 8mS and bridging a tone absence of 10 to 12mS. Refer to Fig. 6

7640 Typical Digital Output



All data output pins are logic MOS compatible with 10Kohms (± 20%) pulldown resistors connected to −Vs internally.

Fig. 3

7640 Touch-Tone Receiver Truth Table

Touch-Tone Symbol	Input Signal Frequency	Binary Outputs PIN 28 BIN 8	PIN 25 BIN 4	PIN 24 BIN 2	PIN 23 BIN 1	PIN 22 STROBE
1	697 & 1209	0	0	0	1	1
2	697 & 1336	0	0	1	0	1
3	697 & 1477	0	0	1	1	1
4	770 & 1209	0	1	0	0	1
5	770 & 1336	0	1	0	1	1
6	770 & 1477	0	1	1	0	1
7	852 & 1209	0	1	1	1	1
8	852 & 1336	1	0	0	0	1
9	852 & 1477	1	0	0	1	1
0	941 & 1336	1	0	1	0	1
*	941 & 1209	1	0	1	1	1
#	941 & 1477	1	1	0	0	1
A	697 & 1633	1	1	0	1	1
B	770 & 1633	1	1	1	0	1
C	852 & 1633	1	1	1	1	1
D	941 & 1633	0	0	0	0	1

Touch-Tone Symbol	Input Signal Frequency	2 of 8 Outputs PIN 23 L1	PIN 24 L2	PIN 25 L3	PIN 26 L4	PIN 27 H1	PIN 28 H2	PIN 29 H3	PIN 30 H4	PIN 22 STROBE
1	697 & 1209	0	1	1	1	0	1	1	1	0
2	697 & 1336	0	1	1	1	1	0	1	1	0
3	697 & 1477	0	1	1	1	1	1	0	1	0
4	770 & 1209	1	0	1	1	0	1	1	1	0
5	770 & 1336	1	0	1	1	1	0	1	1	0
6	770 & 1477	1	0	1	1	1	1	0	1	0
7	852 & 1209	1	1	0	1	0	1	1	1	0
8	852 & 1336	1	1	0	1	1	0	1	1	0
9	852 & 1477	1	1	0	1	1	1	0	1	0
0	941 & 1336	1	1	1	0	1	0	1	1	0
*	941 & 1209	1	1	1	0	0	1	1	1	0
#	941 & 1477	1	1	1	0	1	1	0	1	0
A	697 & 1633	0	1	1	1	1	1	1	0	0
B	770 & 1633	1	0	1	1	1	1	1	0	0
C	852 & 1633	1	1	0	1	1	1	1	0	0
D	941 & 1633	1	1	1	0	1	1	1	0	0

1 = HIGH LEVEL
0 = LOW LEVEL

Fig. 4

7640 Pin Assignments

Package Viewed from Top

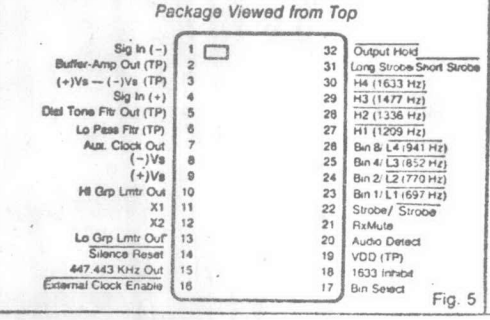
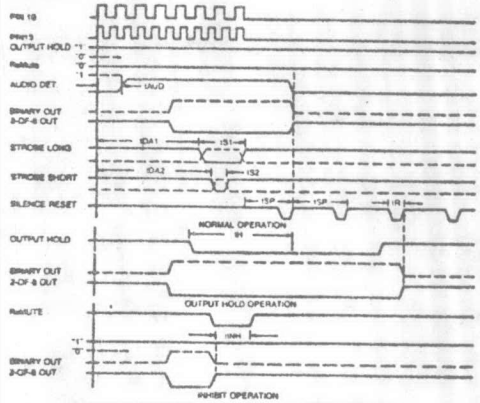


Fig. 5

7640 Timing Diagram



Timing			
tSP	Silence Period	tINH	Chip Inhibit Pulsewidth
tR	Silence Pulsewidth	tS1	Strobe Pulsewidth Option 1
tDA1	Data Acquisition Time Option 1	tS2	Strobe Pulsewidth Option 2
tDA2	Data Acquisition Time Option 2	tAUD	Audio Det. Time
tH	Output Hold Set-up Time		

Fig. 6

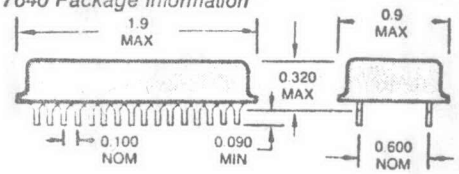
Operating Mode Selection

Function/Pin	16	17	18	21	31	32
External Clock Enable	O	X	X	X	X	X
Binary Output	X	O	X	X	X	X
1633 Inhibit	X	X	O	X	X	X
RxMute	X	X	X	O	X	X
Strobe Control (Short)	X	X	X	X	O	X
Output Hold	X	X	X	X	X	O

O = Low Level X = Don't Care

Fig. 7

7640 Package Information



32 Pin Dual In-Line Package (dimensions in inches)

Mechanical Characteristics

Substrate .... Metallized, 96% Alumina
Cover ..... Gold Flashed, Brass
Pins ..... Tinned Kovar
LEAD TEMPERATURE (during soldering)
At distance 1.6 ± 1/32 inch from case for
10 seconds max. ..... 200°C

Recommended Sources

M-TRON CTS
ELECTRO DYNAMICS NDK

Crystal Specifications

Frequency .... 3.57954 MHz
Tolerance ..... ± .005%
TA ..... 25°C
CL ..... 18 pfd

Fig. 8

TELARIS Telecommunications, Inc.

TELARIS, TELECOMMUNICATIONS, INC. • 2772 MAIN STREET • IRVINE, CALIFORNIA 92714 • (714) 754-7566 • TELEX: 681410

4-78 — 2M

Printed in USA

AY-5-9800 Series

Dual Tone Multi-Frequency Receivers

FEATURES

- No tuning required, inherent discrimination better than ± 0.1%.
- Digitally defined bandwidths with no inherent voltage or temperature drift.
- Acquisition time typically 25 ms. (tone inputs to common output)
- Frequency correlation provides good S/N performance.
- Inter-tone separation checked for correct IDP period.
- Many programmable features provide wide applications.
- High reliability and low cost using P-channel process.
- On-chip analog amplifiers for analog preprocessing.
- Interfaces directly with the AY-5-9100 for M.F.—Strowger converters. (AY-5-9801/9805).
- Handshaking facility to interface directly with CP1600 microprocessor.
- Three-State code outputs.

AY-5-9800 SERIES

Part Number*	Output Code	On-Chip OP Amps	Pins
AY-5-9801/9821	4-Bit	Yes	28
AY-5-9802/9822	1 of 16	Yes	40
AY-5-9803/9823	2 of 8	Yes	40
AY-5-9804/9824	Binary	Yes	28
AY-5-9805/9825	4-Bit	No	24
AY-5-9806/9826	1 of 16	No	40
AY-5-9807/9827	2 of 8	No	24
AY-5-9808/9828	Binary	No	24

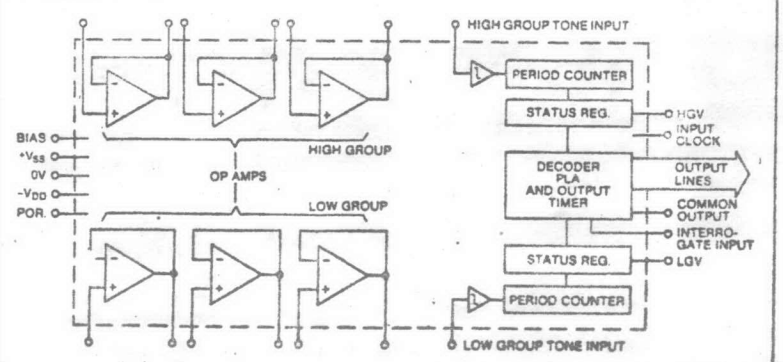
*Part numbers AY-5-9801 through 9808 are supplied in ceramic packages. Part numbers AY-5-9821 through 9828 are supplied in plastic packages.

PROGRAMMABLE OPTIONS

These options can all be provided by a single layer mask change.

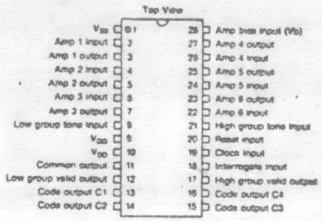
- Programmable center frequencies
- Programmable accuracies
- Variable "Acquire" criteria (1 out of 5 to 5 out of 5)
  Variable "Release" criteria (1 out of 5 to 5 out of 5)
- Normally arranged for 2 of 8 detection, but can be reprogrammed for single tone (1 of 8) detection.
- Common output can be delayed by 1-32 ms after tones are detected valid.
  Note: IDP period = common delay + common width.
- Common output pulse can be programmed from 1-31 mS.
- Output code can be any 4 bit code in 24/28 lead DIP or any 16-bit code in 40 lead DIP (e.g. 2 of 7, 1 of 12 etc.)

BLOCK DIAGRAM

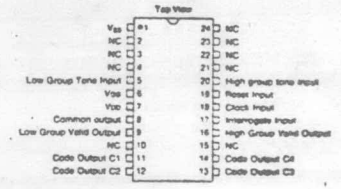


PIN CONFIGURATIONS

28 LEAD DUAL IN LINE
AY-5-9801/9821
AY-5-9804/9824

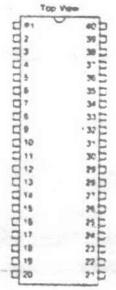


24 LEAD DUAL IN LINE
AY-5-9805/9825
AY-5-9808/9828



40 LEAD DUAL IN LINE
AY-5-9802/9822

40 LEAD DUAL IN LINE
AY-5-9806/9826
Not yet defined



40 LEAD DUAL IN LINE
AY-5-9803/9823
Not yet defined

24 LEAD DUAL IN LINE
AY-5-9807/9827
Not yet defined

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

Voltage on any pin with respect to V_{SS} ..... -20V to +0.3V
Storage Temperature Range ..... -65°C to +150°C
Ambient operating temperature ..... -25°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied — operating ranges are specified below.

Standard Conditions (unless otherwise noted)

V_{SS} = 0V
V_{DD} = -8.5 ±0.5V
V_{GG} = -17V ±1V
Clock frequency = 1 MHz
Operating Temperature (T_A) = +25°C

Characteristics	Min	Typ	Max	Units	Conditions
Clock					
Logic '0' level	+0.3	—	-1.0	V	
Logic '1' level	-6.5	-8.5	-18	V	
Frequency (see NOTE below)	0.01	1.0	1.1	MHz	
Rise Time	10	—	50	ns	
Fall Time	10	—	50	ns	
Width	450	500	550	ns	
Capacitance	—	—	20	pF	
Leakage	—	—	10	µA	
Logic Inputs					
Logic '0' level	+0.3	—	-1.0	V	
Logic '1' level	-3.7	-5	-18	V	
Capacitance	—	—	10	pF	
Leakage	—	—	10	µA	
Logic Outputs					
(i) Code outputs					
Logic '0' output current	1	—	—	mA	V_O = -1V
Logic '1' output current	480	—	—	µA	V_O = -5V
(ii) Common output					
Logic '0' output current	1	—	—	mA	V_O = -1V
Logic '1' output current	620	—	—	µA	V_O = -5V
Pulse delay	1	—	31	ms	
Pulse width	1	32	32	ms	
(iii) Group valid outputs (HGV & LGV)					
Logic '0' output current	500	—	—	µA	V_O = -1V (External pull-down resistors to V_{DD} required).
Signal Input	.5	—	2	V	Peak to peak sine wave
"Handshake" Routine					
(See Fig. 1 for timing diagram). T1, T2	—	—	2.5	µs	
Pull-down resistor (to V_{DD})	50	160	500	KΩ	
Power-on Reset					
Pull-down resistor (to V_{DD})	50	150	500	KΩ	
Pulse Width	10	—	—	µs	
Amplifiers					
Open loop gain	—	500	—	—	F_{in} = 1KHz
Open loop bandwidth	—	1	—	MHz	
Output impedance	—	—	8	KΩ	F_{in} = 1KHz
Power Dissipation	—	—	350	mW	V_{DD} = -9V V_{GG} = -18V

NOTE: Any deviation from the nominal 1MHz clock frequency will result in a corresponding deviation of the frequency detection bands. Other frequencies than 1MHz clock can be preprogrammed in, but circuit characteristics will be modified.

The AY-5-9600 series circuits are fabricated in P channel MTNS process thus minimizing cost and providing high reliability. The basic chip block diagram is shown on the previous page. For analog preprocessing six amplifiers and two source followers are included on-chip, external components being used to determine the filter characteristics. The major functions are mask programmable thus giving a flexible system at a low cost.

The tone pair is separated into two individual tones using the analog circuitry, the separated tones being applied to the Schmidt triggers to square incoming signals which are then processed by the digital circuitry. The high and low group logic is similar; only the decode values for frequency recognition are different. The incoming signal is divided by two or three to eliminate the effects of changing mark/space ratio and its period counted by a timer which is clocked by the accurate 1MHz clock. If the period value is within encoded limits, the result is stored. Five cycles of incoming signal are stored and a decision is made with this information as to whether the tone is valid. A programmable logic array scans the five cycle store for both a "Acquire" criteria and "Release" criteria. If the "Acquire" criteria is exceeded (e.g. 4 out of 5), and the "Release" criteria is not reached (e.g. less than 2 out of 5), the frequency is deemed to be valid. If both high and low frequencies are detected, a time-out timer is started. This timer is mask programmable and will normally require 25ms of valid tone pair signal. Once this period has elapsed the Common Output pulses high, again for a preprogrammed period. After this pulse, the system will not respond again until an IDP of a preprogrammed duration occurs, after which a new input tone pair can be applied.

The Code Outputs and Common Output can be configured for a wide variety of systems. A typical device, AY-5-9601/9621, provides four Three-State Code outputs suitable for microprocessor controlled systems and direct interfacing to the AY-5-9100 for DTMF-Strowger converters. A handshaking interface is provided using the Interrogate input thus allowing very simple microprocessor interfacing. The outputs will directly drive low power TTL, CMOS or MOS and, being Three-State, can be bussed in large systems.

Input Clock — The recommended clock frequency is 1MHz which will then give a frequency detect range of 620—3400Hz with a discrimination of ± 1µs. The discrimination of 1633Hz using a 1MHz clock will be better than ± 0.1%. Any deviation of the 1MHz clock will result in a proportional deviation of the tone recognition bands.

Power-On-Reset—An external power-on reset is required which is used to reset all counters, etc. An on-chip resistor pulls this input to V_{DD}. a 0.1µF capacitor connected from the P.O.R. input to V_{SS} will provide automatic power-on-reset. This input can be used as a chip select putting all Three-State outputs into their high impedance state when held high.

Input Amplifiers—Input amplifiers are suitable for use in band-pass and general buffer amplifiers. They have an open loop gain of approximately 250 and are trimmed by a single 'Bias Input'.

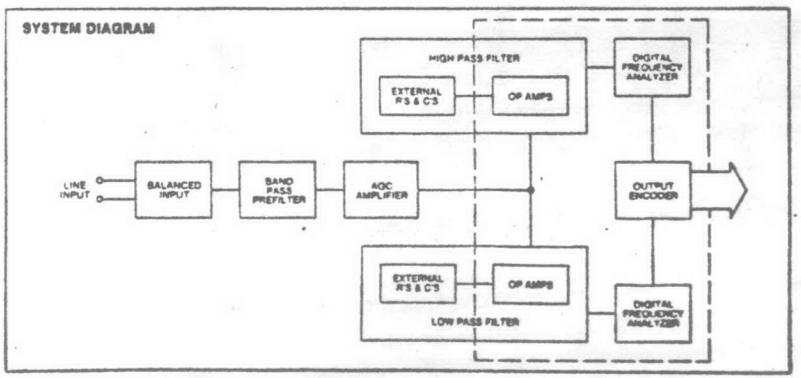
Period Counters—The input frequency is interrogated by the period counter. Each counter has eight values decoded, these representing F1 low limit, F1 high limit, etc. Once a positive going edge is detected, the period counter is started and if the next positive going edge occurs during a time slot decode, the circuit deems the tone to be valid and a bistable indicating the tone decoded is set. Special logic is incorporated to prevent the counter from being continuously triggered in the presence of noise.

Status Word Register—The Status Word Register is a five bit register which is filled with 1's for an in-band signal but filled with 0's for out-of-band signals. With the data in this register a decision is performed which sets a bistable (Acquires the signal) or resets a bistable (Releases the signal). Thus by changing the preprogrammed acceptance standard, a direct trade-off between S/N ratio and stimulation rate can be obtained for different systems.

Output Logic—Two outputs, HGV and LGV, indicate the current state of the correlator for each group. A valid high group frequency, if present for longer than the correlation time, will cause the HGV (high group valid) output to go low. Similarly with the LGV (low group valid) output. Once both high and low group tones have been detected valid, a preprogrammed timer is started. If the tone pair is still valid after the timer has counted out, the Common Output goes high for a preprogrammed period and the Code Outputs present the programmed outputs corresponding to the tone pair input.

If the Interrogate input is used for handshaking, the Code Outputs are only presented after the Interrogate input goes high; the interrogate input going low removes both the Codes and the Common Output.

SYSTEM DIAGRAM



OUTPUT CODE CHART

Input Tone Pair		Normal Digit Representation	AY-5-9801/9821 AY-5-9805/9825 Output Code*				AY-5-9802/9822 AY-5-9806/9826 Output Code	AY-5-9803/9823 AY-5-9807/9827 Output Code	AY-5-9804/9824 AY-5-9808/9828 Output Code**			
Low Group (Hz)	High Group (Hz)	C1	C1	C2	C3	C4	1 of 16	2 of 8	C1	C2	C3	C4
697	1209	1	1	1	1	1	C1	C1,C5	1	1	1	0
697	1336	2	1	1	1	0	C2	C1,C8	1	1	0	1
697	1477	3	1	1	0	1	C3	C1,C7	1	1	0	0
697	1633	— A	0	0	0	1	C4	C1,C8	0	0	0	1
770	1209	4	1	0	1	1	C5	C2,C5	1	0	1	1
770	1336	5	1	0	1	0	C6	C2,C6	1	0	1	0
770	1477	6	1	0	0	1	C7	C2,C7	1	0	0	1
770	1633	— B	0	0	1	0	C8	C2,C8	0	0	1	0
852	1209	7	0	1	1	1	C9	C3,C5	1	0	0	0
852	1336	8	0	1	1	0	C10	C3,C6	0	1	1	1
852	1477	9	0	1	0	1	C11	C3,C7	0	1	1	0
852	1633	— C	0	1	0	0	C12	C3,C8	0	0	1	1
941	1209	*	0	0	1	1	C13	C4,C5	0	1	0	0
941	1336	0	1	1	0	0	C14	C4,C6	0	1	0	1
941	1477	#	0	0	0	0	C15	C4,C7	0	0	0	0
941	1633	— D	1	0	0	0	C16	C4,C8	1	1	1	1

*Compatible with AY-5-9100 **Compatible with AY-5-9120

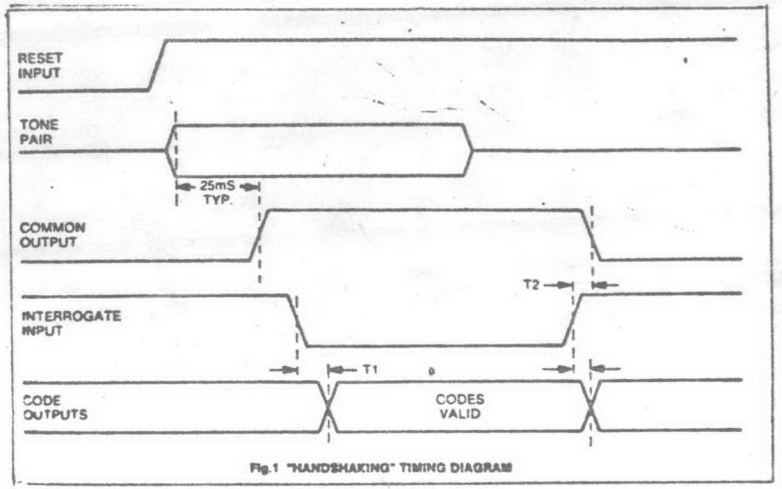


Fig.1 "HANDSHAKING" TIMING DIAGRAM

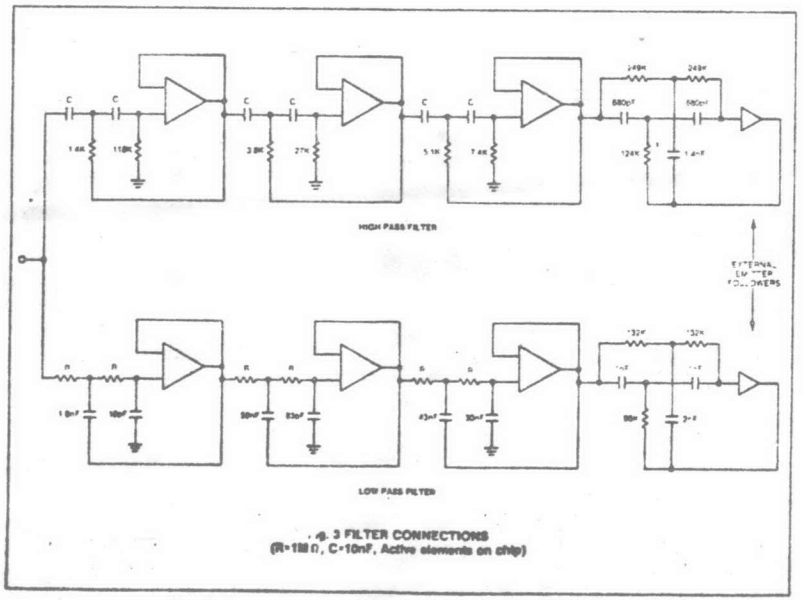
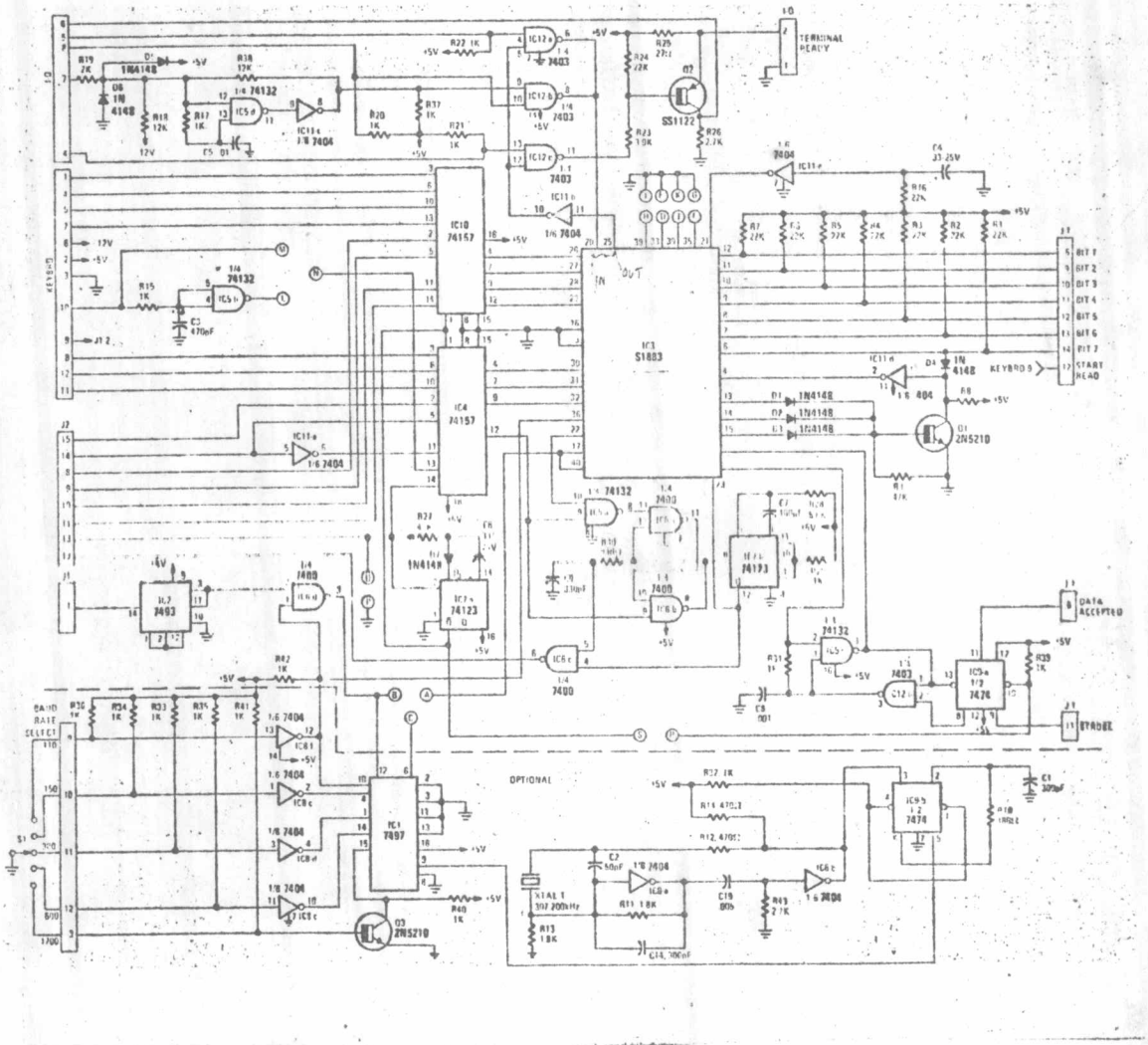


Fig. 3 FILTER CONNECTIONS
(R=1MΩ, C=10nF, Active elements on chip)

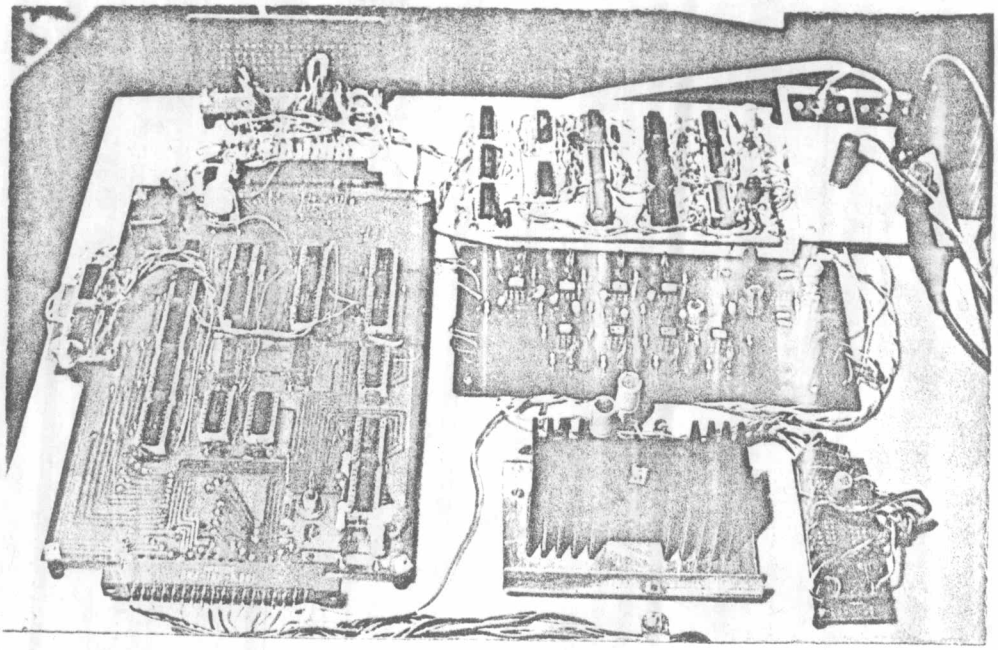
ภาคผนวก จ.

วงจร Serial Interface ที่ใช้กับเครื่องพิมพ์ดีด-โทรทัศน์

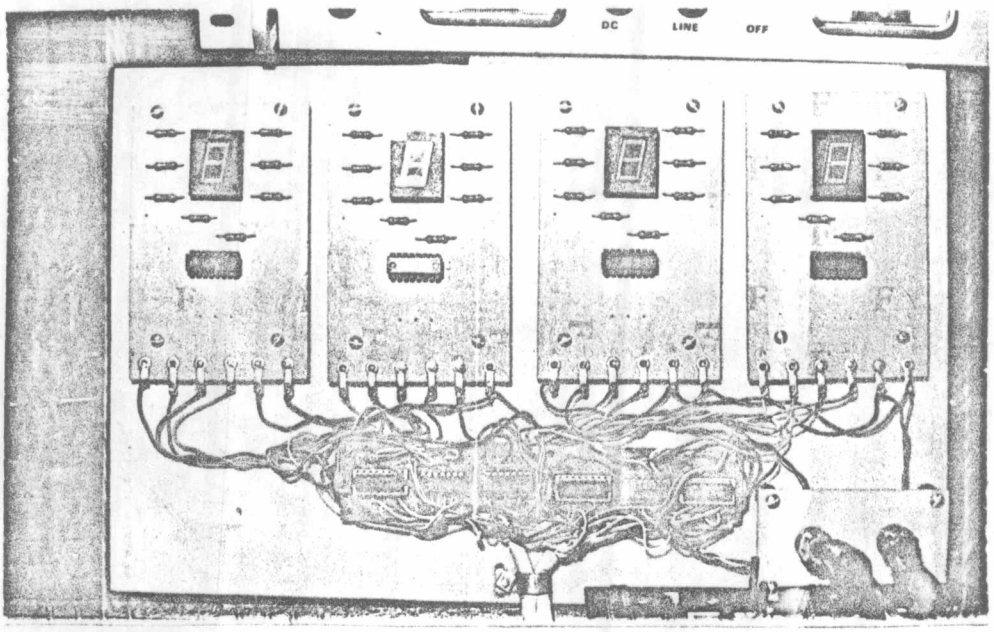


ภาคผนวก ฉ.

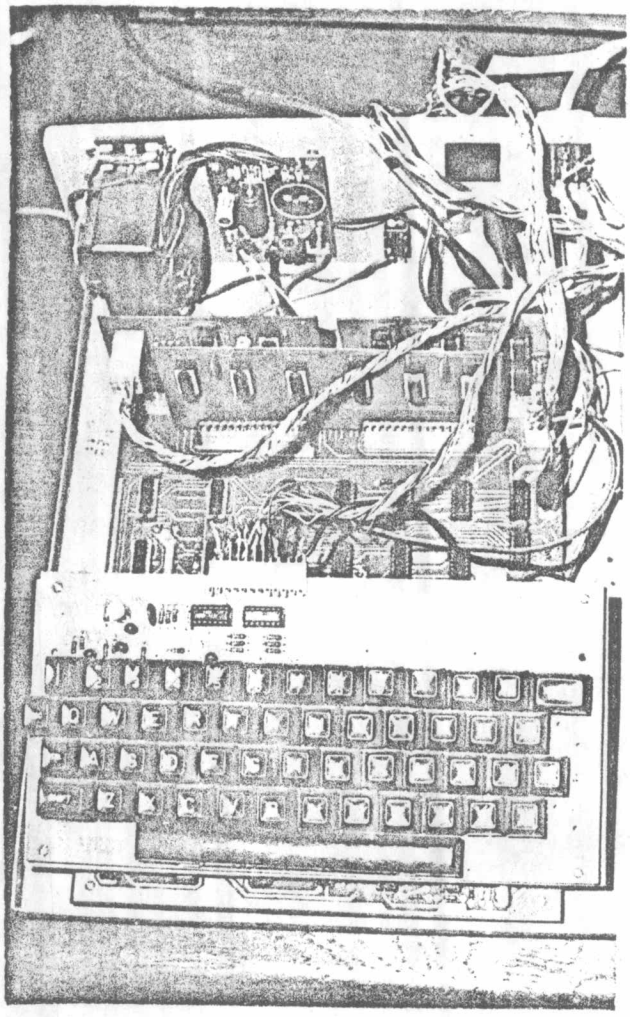
เครื่องมือและอุปกรณ์ที่วิจัย



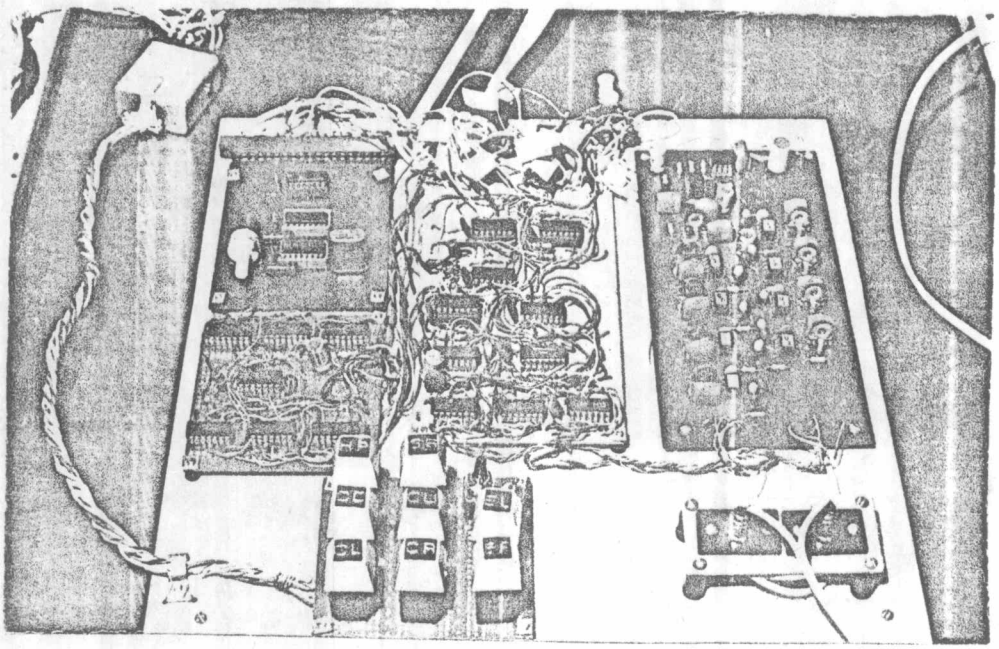
เครื่องรับที่สถานีตรวจวัดปริมาณน้ำฝน



เครื่องแสดงข้อมูลปริมาณน้ำฝนที่วัดได้



เครื่องพิมพ์ดีดโทรทัศน์ที่ใช้ในงานวิจัย



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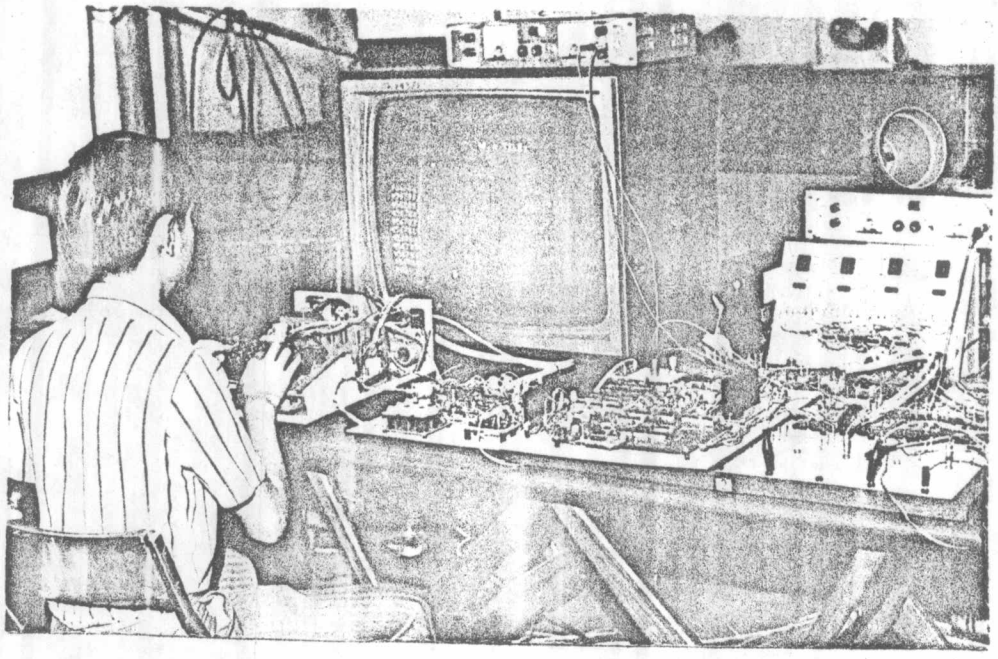
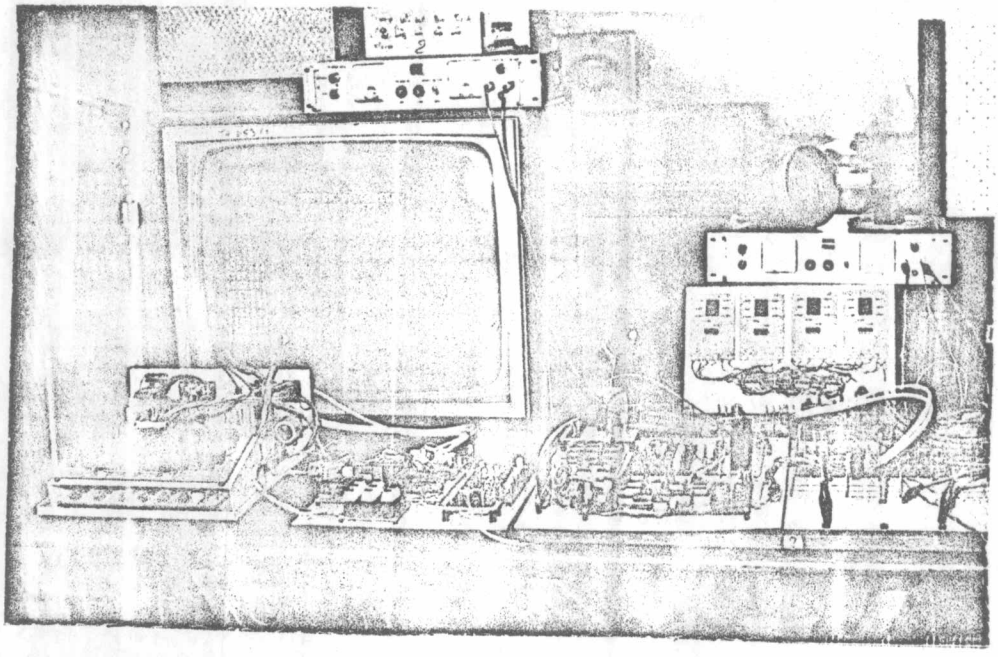


การทดสอบเครื่องมือตรวจวัดปริมาณน้ำฝนทางโทรมาตร



เครื่องมือตรวจวัดปริมาณน้ำฝนทางโทรมาตร

ประวัติการศึกษา

นายมนตรี พรหมเพ็ชร สำเร็จการศึกษาวิศวกรรมศาสตร์บัณฑิต สาขาวิชาไฟฟ้า แขนงวิชาไฟฟ้าสื่อสาร จากสถาบันเทคโนโลยีพระจอมเกล้า วิทยาเขตนนทบุรี เมื่อ ปี พ.ศ. ๒๕๑๖ ปัจจุบันเป็นอาจารย์ประจำแผนกวิชาช่างวิทยุและโทรคมนาคม วิทยาลัยเทคโนโลยีและอาชีวศึกษา วิทยาเขตเทเวศร์ กระทรวงศึกษาธิการ

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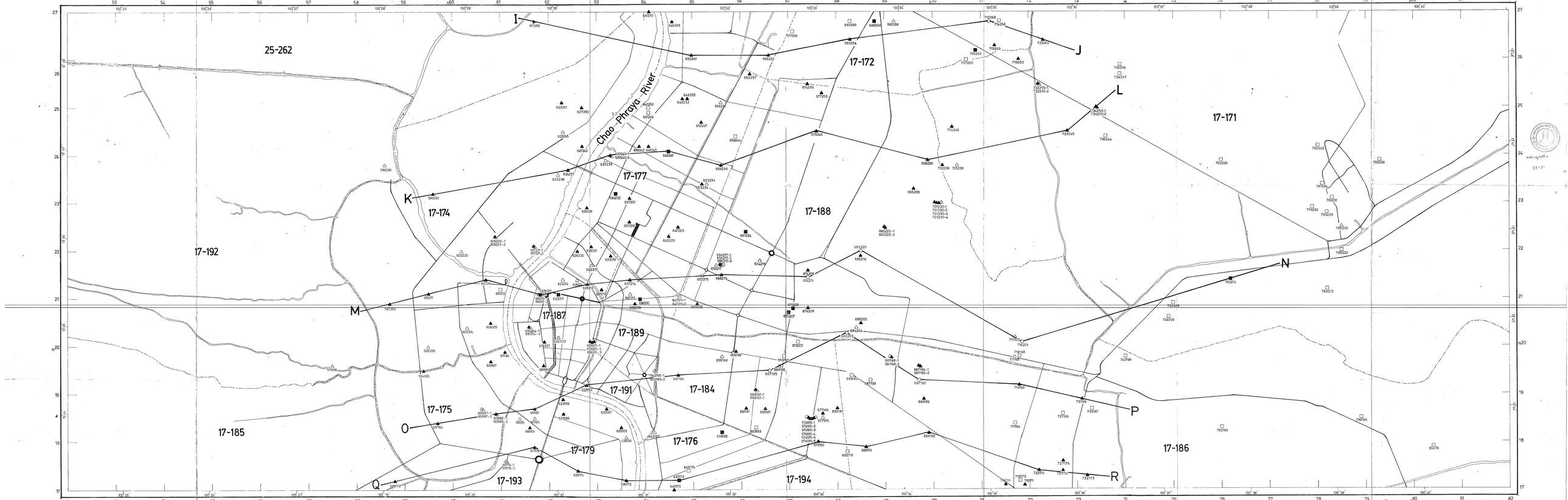

PLATE 1-B WELL LOCATION MAP IN THE MIDDLE PART OF BANGKOK METROPOLIS