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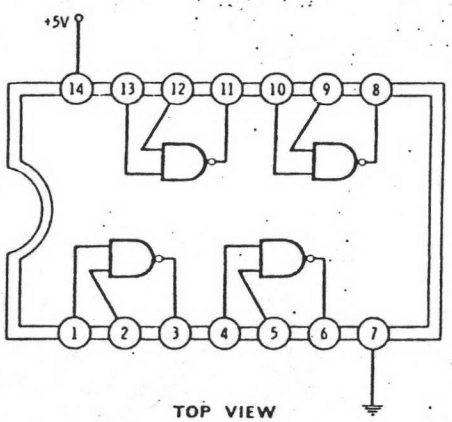
ภาคผนวก ก.

Electrical data of Digital Integated Circuits.

QUAD 2-INPUT NAND GATE

7400



TOP VIEW

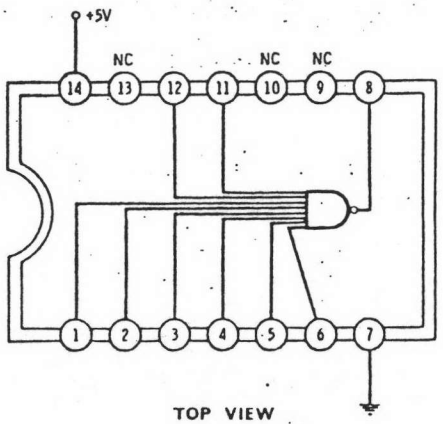
All four positive-logic NAND gates may be used independently. On any one gate, when *either* input is *low* the output is driven *high*. If *both* inputs are *high* the output is *low*.

Propagation delay ..... 10 nanoseconds average

Current per package ..... 12 milliamperes average

8-INPUT NAND GATE

7430



TOP VIEW

There is only a single gate per package. *Any* input-*low* condition drives the output *high*. When *all* inputs are *high* the output is *low*.

Propagation delay ..... 10 nanoseconds typical

Current per package ..... 2 milliamperes average

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '00, '04, '10, '20, '30			SERIES 54H SERIES 74H 'H00, 'H04, 'H10, 'H20, 'H30			SERIES 54L SERIES 74L 'L00, 'L04, 'L10, 'L20, 'L30			SERIES 54LS SERIES 74LS 'LS00, 'LS04, 'LS10, 'LS20, 'LS30			SERIES 54S SERIES 74S 'S00, 'S04, 'S10, 'S20, 'S30, 'S133			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−400			−500			−100			−400			−1000	μA
	74 Family			−400			−500			−200			−400			−1000	
Low-level output current, I_{OL}	54 Family			16			20			2			4			20	mA
	74 Family			16			20			3.6			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS‡			SERIES 54 SERIES 74 '00, '04, '10, '20, '30			SERIES 54H SERIES 74H 'H00, 'H04, 'H10, 'H20, 'H30			SERIES 54L SERIES 74L 'L00, 'L04, 'L10, 'L20, 'L30			SERIES 54LS SERIES 74LS 'LS00, 'LS04, 'LS10, 'LS20, 'LS30			SERIES 54S SERIES 74S 'S00, 'S04, 'S10, 'S20, 'S30, 'S133			UNIT
						MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IH}	High-level input voltage	1, 2				2			2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2			54 Family			0.8			0.8			0.7			0.7			0.8	V
					74 Family			0.8			0.8			0.7			0.8			0.8	
V_I	Input clamp voltage	3	V_{CC} = MIN, I_I = §					−1.5			−1.5						1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OH} = MAX		54 Family	2.4	3.4		2.4	3.5		2.4	3.3		2.5	3.4		2.5	3.4		V
					74 Family	2.4	3.4		2.4	3.5		2.4	3.2		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX		54 Family		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
					74 Family		0.2	0.4		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V					1			1			0.1			0.1			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX		V_{IH} = 2.4 V			40			50			10							μA
					V_{IH} = 2.7 V												20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX	V_{IL} = 0.3 V										−0.18							mA
				V_{IL} = 0.4 V	LS30												−0.4				
					Others			−1.6			−2						−0.36				
				V_{IL} = 0.5 V																−2	
I_{OS}	Short-circuit output current¶	6	V_{CC} = MAX		54 Family	−20		−55	−40		−100	−3		−15	−6		−40	−40		−100	mA
					74 Family	−18		−55	−40		−100	−3		−15	−5		−42	−40		−100	
I_{CC}	Supply current	7	V_{CC} = MAX			See table on next page															mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for SN54'/SN74', −8 mA for SN54H'/SN74H', and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.
¶Not more than one output should be shorted at a time, and for SN54H'/SN74H' and SN54S'/SN74S', duration of short-circuit should not exceed 1 second.
*The input clamp voltage specification is effective for Series 54/74 and 54H/74H parts date-coded 7332 or higher.

POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

supply current[¶]

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'00	4	8	12	22	2
'04	6	12	18	33	2
'10	3	6	9	16.5	2
'20	2	4	6	11	2
'30	1	2	3	6	2
'H00	10	16.8	26	40	4.5
'H04	16	26	40	58	4.5
'H10	7.5	12.6	19.5	30	4.5
'H20	5	8.4	13	[illegible]	4.5
'H30	2.5	4.2	6.5	[illegible]	4.5
'L00	0.44	0.8	1.16	2.04	0.20
'L04	0.66	1.2	1.74	3.06	0.20
'L10	0.33	0.6	0.87	1.53	0.20
'L20	0.22	0.4	0.58	1.02	0.20
SN54L30	0.11	0.33	0.29	0.51	0.20
SN74L30	0.11	0.2	0.29	0.51	0.20
'LS00	0.8	1.6	2.4	4.4	0.4
'LS04	1.2	2.4	3.6	6.6	0.4
'LS10	0.6	1.2	1.8	3.3	0.4
'LS20	0.4	0.8	1.2	2.2	0.4
'LS30	0.35	0.5	0.6	1.1	0.48
'S00	10	16	20	36	3.75
'S04	15	24	30	54	3.75
'S10	7.5	12	15	27	3.75
'S20	5	8	10	18	3.75
'S30	3	5	5.5	10	4.25
'S133	3	5	5.5	10	4.25

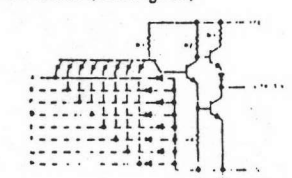
[¶] Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS[#]	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'00, '10	C_L = 15 pF, R_L = 400 Ω		11	22		7	15
'04, '20			12	22		8	15
'30			13	22		8	15
'H00	C_L = 25 pF, R_L = 280 Ω		5.9	10		6.2	10
'H04			6	10		6.5	10
'H10			5.9	10		6.3	10
'H20			6	10		7	10
'H30			6.8	10		8.9	12
'L00, 'L04, 'L10, L20	C_L = 50 pF, R_L = 4 kΩ		15	60		31	60
'L30			35	60		70	100
'LS00, 'LS04 'LS10, 'LS20	C_L = 15 pF, R_L = 2 kΩ		9	20		10	20
'LS30			9	20		25	35
'S00, 'S04	C_L = 15 pF, R_L = 280 Ω	2	3	4.5	2	3	5
'S10, 'S20	C_L = 50 pF, R_L = 280 Ω		4.5			5	
'S30, 'S133	C_L = 15 pF, R_L = 280 Ω	2	4	6	2	4.5	7
	C_L = 50 pF, R_L = 280 Ω		5.5			6.5	

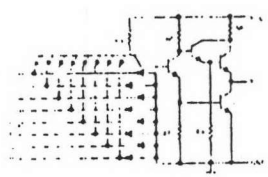
[#] Load circuits and voltage waveforms are shown on pages 148 and 149.

schematics (each gate)

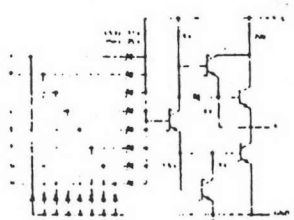


CIRCUIT	R1	R2	R3	R4
'00, '04, '10, '20, '30	4 k	1.6 k	130	1 k
'L00, 'L04, 'L10, 'L20, 'L30	40 k	20 k	500	12 k

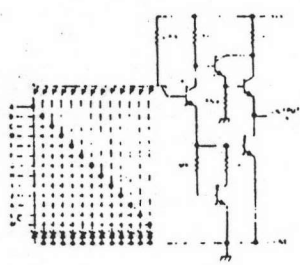
'00, '04, '10, '20, '30
'L00, 'L04, 'L10, 'L20, 'L30, CIRCUITS
Input clamp diodes not on SN54L', SN74L' circuits.



'H00, 'H04, 'H10, 'H20, 'H30 CIRCUITS



'LS00, 'LS04, 'LS10, 'LS20, 'LS30 CIRCUITS



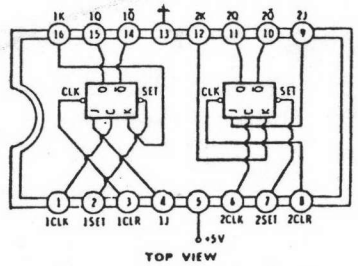
'S00, 'S04, 'S10, 'S20, 'S30, 'S133 CIRCUITS

Resistor values shown are nominal and in ohms.

ภาคผนวก ก.(ต่อ)

7476

DUAL JK LEVEL-TRIGGERED FLIP-FLOP (With Preset and Preclear)



TOP VIEW

Contains two independent level-clocked JK flip-flops. Note the unusual supply connections.

This is a clocked logic block and is covered in detail in Chapter 5. There are two outputs: Q, and its complement $\overline{Q}$.

Under certain input conditions, Q and $\overline{Q}$ can change whenever the Clock input goes to a low level. The Q and $\overline{Q}$ outputs do not change for a change in the J and K inputs; the only time they can change is as the input clock goes to a low level.

If J and K are grounded, the clock does *nothing*. If J and K are made positive, the clock changes the output states on Q and $\overline{Q}$, or *binarily divides*. If J is high and K is low, clocking makes Q high and $\overline{Q}$ low. If J is low and K is high, clocking makes Q low and $\overline{Q}$ high.

Information on the J and K inputs can be changed only once immediately after clocking. Further changes can bring about invalid operation (see Chapter 5). The clock must be conditioned to drop very rapidly per desired operation.

The Clear and Set inputs should be left, or tied positive for normal operation. If the Clear input is grounded, the flip-flop *immediately* goes into the state with Q low and $\overline{Q}$ high. If the Set input is grounded, the flip-flop *immediately* goes into the state with Q high and $\overline{Q}$ low. Set and Clear should *never* be simultaneously grounded, or a disallowed state will result.

Maximum toggle frequency ..... 20 megahertz

Current per package ..... 20 milliamperes

recommended operating conditions

		SERIES 54/74	'70			'72, '73, '76, '107			'74			'109			'110			'111			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−400			−400			−400			−800			−800			−800	μA
Low-level output current, I_{OL}					16			16			16			16			16			16	mA
Pulse width, t_w	Clock high		20			20			30			20			25			25			ns
	Clock low		30			47			37			20			25			25			
	Preset or clear low		25			25			30			20			25			25			
Input setup time, t_{setup}			20↑			0↑			20↑			10↑			20↑			0↑			ns
Input hold time, t_{hold}			5↑			0↓			5↑			6↑			5↑			30↑			ns
Operating free-air temperature, T_A		Series 54	−55		125	−55		125	−55		125	−55		125	−55		125	−55		125	°C
		Series 74	0		70	0		70	0		70	0		70	0		70	0		70	

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	'70			'72, '73, '76, '107			'74			'109			'110			'111			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8			0.8			0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			*−1.5			*−1.5			*−1.5			−1.5			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1			1			1			1			1	mA
I_{IH}	High-level input current	D, J, K, or $\overline{R}$	V_{CC} = MAX, V_I = 2.4 V			40			40			40			40			40			40	μA
		Clear				80			80			120			160			160			80	
		Preset				80			80			80			80			100			80	
		Clock				40			80			80			80			40			120	
I_{IL}	Low-level input current	D, J, K, or $\overline{R}$	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6			−1.6			−1.6			−1.6			−1.6	mA
		Clear				−3.2			−3.2			−3.2			−4.8			−3.2			−3.2	
		Preset				−3.2			−3.2			−1.6			−3.2			−3.2			−3.2	
		Clock				−1.6			−3.2			−3.2			−3.2			−1.6			−4.8	
I_{OS}	Short-circuit output current♦	Series 54	V_{CC} = MAX	−20		−57	−20		−57	−20		−57	−30		−85	−20		−57	−20		−57	mA
		Series 74		−18		−57	−18		−57	−18		−57	−30		−85	−18		−57	−18		−57	
I_{CC}	Supply current (Average per flip-flop)		V_{CC} = MAX See Note 1		13	26		10	20		8.5	15		9	15		20	34		14	20 b	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

♦Not more than one output should be shorted at a time.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is at 4.5 V for the '70, '110, and '111; and is grounded for all the others.

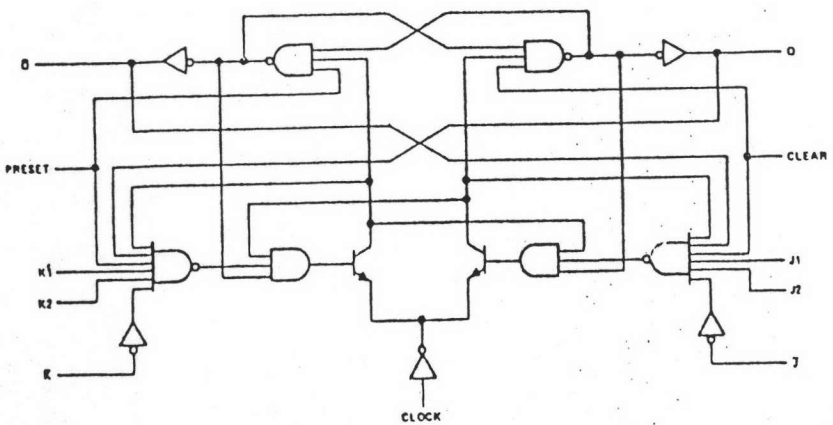
*The input clamp voltage specification is effective for Series 54/74 parts date-coded 7332 or higher.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

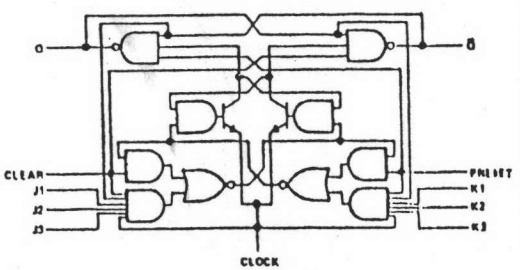
PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'70			'72, '73, '76, '107			'74			'109			'110			'111			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Note 2	20	35		15	20		15	25		25	33		20	25		20	25		MHz
t_{PLH}	Preset (as applicable)	Q				50		16	25			25		10	15		12	20		12	18	ns
t_{PHL}		$\bar{Q}$				50		25	40			40		23	35		18	25		21	30	
t_{PLH}	Clear (as applicable)	$\bar{Q}$				50		16	25			25		10	15		12	20		12	18	ns
t_{PHL}		Q				50		25	40			40		17	25		18	25		21	30	
t_{PLH}	Clock	Q or $\bar{Q}$		10	27	50	10	16	25	10	14	25	4	10	16	10	20	30	6	12	17	ns
t_{PHL}				10	18	50	10	25	40	10	20	40	9	18	28	6	13	20	10	20	30	

[1] f_{max} ≡ maximum clock frequency; t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output.
NOTE 2: Load circuit and voltage waveforms are shown on page 148.

functional block diagrams



'70–GATED J-K WITH CLEAR AND PRESET



'72–GATED J-K WITH CLEAR AND PRESET

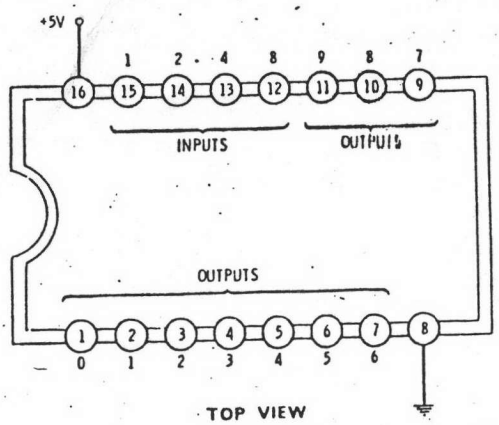
See following pages for:
'73–DUAL J-K WITH CLEAR
'74–DUAL D WITH CLEAR AND PRESET
'76–DUAL J-K WITH CLEAR AND PRESET
'107–DUAL J-K WITH CLEAR

'109–DUAL J-$\bar{K}$ WITH CLEAR AND PRESET
'110–GATED J-K WITH CLEAR AND PRESET
'111–DUAL J-K WITH CLEAR AND PRESET

ภาคผนวก ก.(ต่อ)

7445

BCD TO 1-OF-10 DECODER/DRIVER
(30-Volt, 80-mA Output)



TOP VIEW

This package accepts a 1-2-4-8 Binary Coded Decimal (BCD) input code and provides a *grounded* output for the selected state. All other outputs remain an open circuit. For instance, a 0111 input or "1" = 1, "2" = 1, "4" = 1, and "8" = 0 gives output line No. 7 a *low* state; all others remain open circuited.

Outputs can sink up to 80 milliamperes in the low state and withstand up to 30 volts in the off state. An output-high condition can only be obtained by a resistor or lamp load pulling up to some voltage less than 30. Note that the *supply* voltage for this package must be +5 volts.

The package can serve as a binary to 1-of-8 decoder by grounding pin No. 12.

Slight settling glitches and overlaps during address (input) changes are possible. Any input code over 1001 sends all inputs to the *open-circuit* condition.

Propagation delay ..... 45 nanoseconds

Current per package ..... 43 milliamperes

ภาคผนวก ก.(ต่อ)

TTL
MSI

TYPES SN5445, SN7445
BCD-TO-DECIMAL DECODERS/DRIVERS

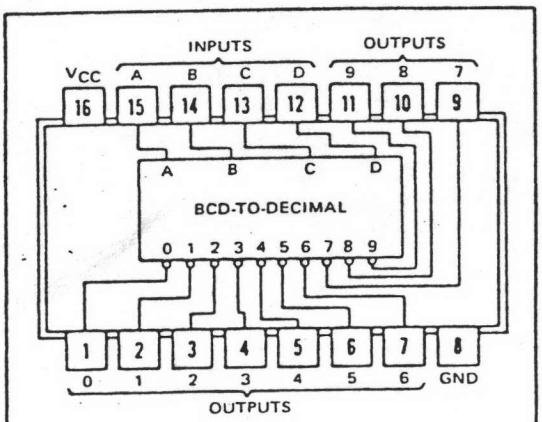
BULLETIN NO. DL-S 7211816, DECEMBER 1972

FOR USE AS LAMP, RELAY, OR MOS DRIVERS

featuring

- Full Decoding of Input Logic
- 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions

J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

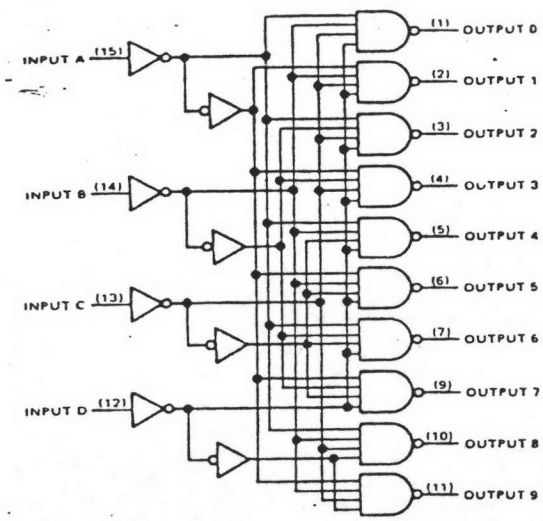
logic

FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level (off), L = low level (on.

functional block diagram



description

These monolithic BCD-to-decimal decoders/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature TTL inputs and high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (30 volts) will sink up to 80 milliamperes of current. Each input is one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts.

ภาคผนวก ก.(ต่อ)

TYPES SN5445, SN7445
BCD-TO-DECIMAL DECODERS/DRIVERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Maximum current into any output (off-state) . . . . . 1 mA
Operating free-air temperature range: SN5445 Circuits . . . . . −55°C to 125°C
SN7445 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5445			SN7445			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage			30			30	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
$V_{O(on)}$	On-state output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	$I_{O(on)}$ = 80 mA		0.5	0.9	V
			$I_{O(on)}$ = 20 mA			0.4	
$V_{O(off)}$	Off-state output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, $I_{O(off)}$ = 250 μA		30			V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	SN5445		43	62	mA
			SN7445		43	70	

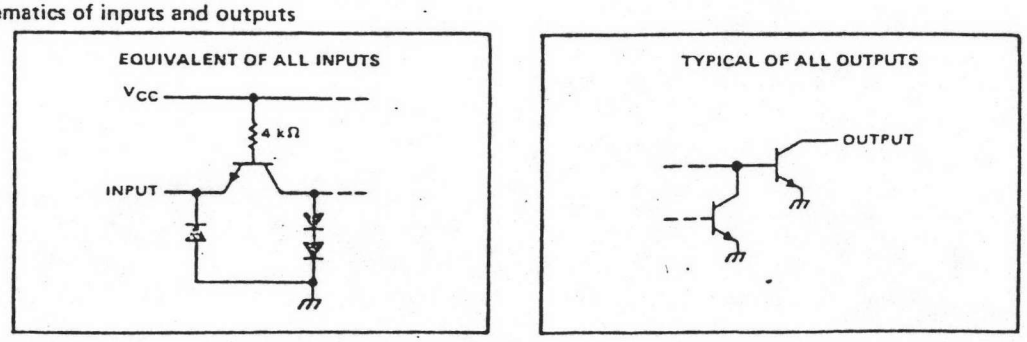
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 100 Ω, See Note 3			50	ns
t_{PHL}	Propagation delay time, high-to-low-level output				50	ns

NOTE 3: Load circuit and waveforms are shown on page 148.

schematics of inputs and outputs



ภาคผนวก ก. (ต่อ)

TTL MSI

TYPES SN5490A, SN5492A, SN5493A, SN54L90, SN54L93, SN7490A, SN7492A, SN7493A, SN74L90, SN74L93 DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

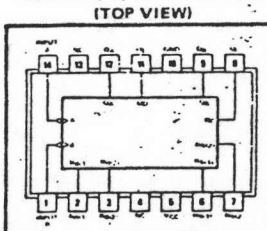
BULLETIN NO. DL-S 7211807, DECEMBER 1972

'90A, 'L90 . . . DECADE COUNTERS

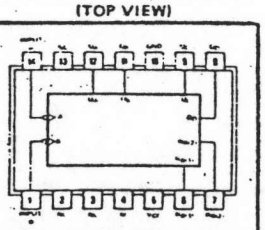
'92A . . . DIVIDE-BY-TWELVE COUNTER

'93A, 'L93 . . . 4-BIT BINARY COUNTERS

'90A . . . J, N, OR W PACKAGE
'L90 . . . J, N, OR T PACKAGE
(TOP VIEW)

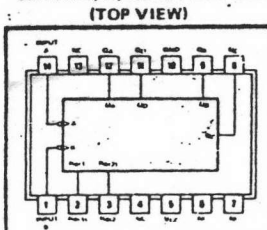


'92A . . . J, N, OR W PACKAGE
(TOP VIEW)

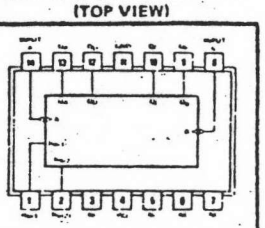


positive logic: see function tables

'93A . . . J, N, OR W PACKAGE
(TOP VIEW)



'L93 . . . J, N, OR T PACKAGE
(TOP VIEW)



positive logic: see function tables

NC—No internal connection

description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A and 'L90, divide-by-six for the '92A, and divide-by-eight for the '93A and 'L93.

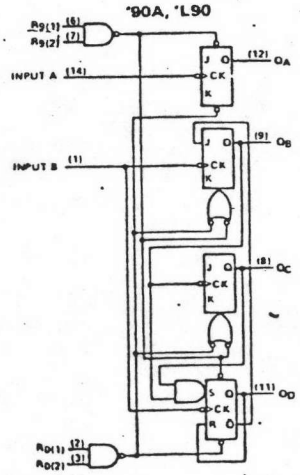
All of these counters have a gated zero reset and the '90A and 'L90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A or 'L90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

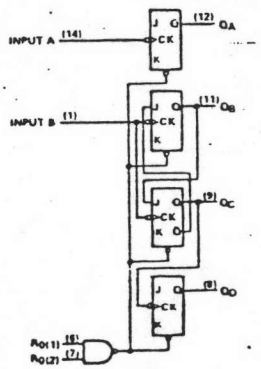
TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'L90	20 mW
'92A, '93A	130 mW
'L93	16 mW

functional block diagrams

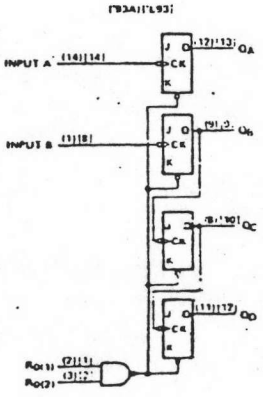
'90A, 'L90



'92A



'93A, 'L93



. . . dynamic input activated by transition from a high level to a low level.

The J and K inputs shown without connection are for reference only and are functionally at a high level.

TYPES SN5490A, SN5492A, SN5493A, SN7490A, SN7492A, SN7493A DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5490A, SN5492A, SN5493A . . . . . −55°C to 125°C
SN7490A, SN7492A, SN7493A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two R_0 inputs, and for the '90A circuit, it also applies between the two R_9 inputs.

recommended operating conditions

		SN5490A, SN5492A, SN5493A			SN7490A, SN7492A, SN7493A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Count frequency, f_{count} (see Figure 1)	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	15			15			
Reset inactive-state setup, t_{setup}		25			25			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'90A			'92A			'93A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			2			V
V_{IL}	Low-level input voltage						0.8			0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA¶			0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	Any reset	V_{CC} = MAX, V_I = 2.4 V				40			40			40	μA
		A input					80			80			80	
		B input					120			120			80	
I_{IL}	Low-level input current	Any reset	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6			−1.6	mA
		A input					−3.2			−3.2			−3.2	
		B input					−4.8			−4.8			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54'	−20		−57	−20		−57	−20		−57	mA
				SN74'	−18		−57	−18		−57	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 3			29	42		26	39		26	39	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
¶Outputs are tested at I_{OL} = 16 mA plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.
NOTE 3: I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

ภาคผนวก ก.(ต่อ)

TYPES SN5490A, SN5492A, SN5493A, SN54L90, SN54L93, SN7490A, SN7492A, SN7493A, SN74L90, SN74L93 DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

'90A, 'L90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'L90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'90A, 'L90
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

'92A
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

'93A, 'L93
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

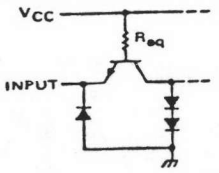
'92A, '93A, 'L93
RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

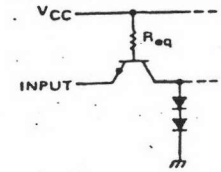
schematics of inputs and outputs

'90A, '92A, '93A
EQUIVALENT OF EACH INPUT



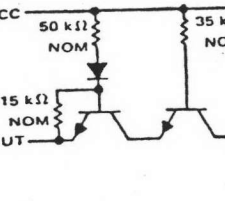
INPUT	R_{eq} NOM
A	2.5 kΩ
B ('90A, '92A)	1.25 kΩ
B ('93A)	2.5 kΩ
All resets	6 kΩ

'L90, 'L93
EQUIVALENT OF EACH INPUT EXCEPT A AND B OF 'L93

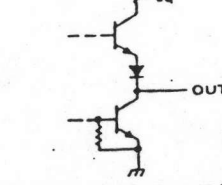


INPUT	R_{eq} NOM
A ('L90)	13.3 kΩ
B ('L90)	6.67 kΩ
All resets	40 kΩ

'L93
EQUIVALENT OF A OR B INPUT



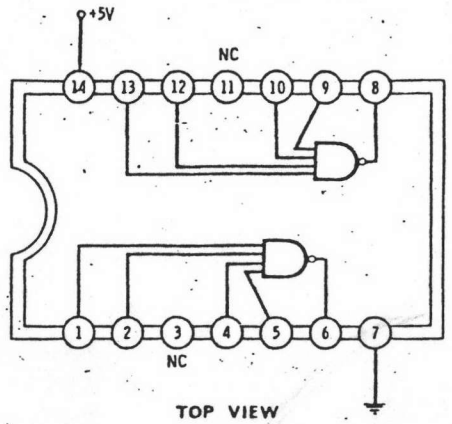
'90A, '92A, '93A, 'L90, 'L93
TYPICAL OF ALL OUTPUTS



'90A, '92A, '93A: R = 100 Ω NOM
'L90, 'L93: R = 500 Ω NOM

DUAL 4-INPUT NAND GATE

7420



TOP VIEW

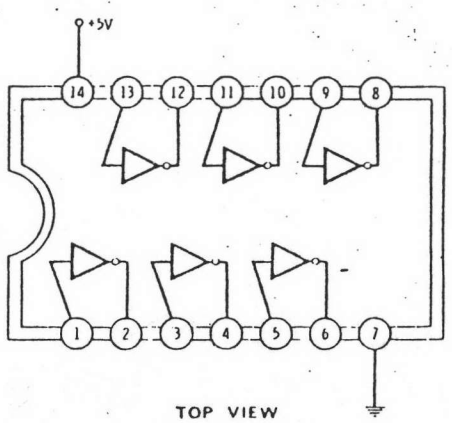
Both 4-input gates may be used independently. On either gate, *any* input-*low* condition drives the output *high*. When *all* inputs are high, the output is low.

Propagation delay ..... 10 nanoseconds typical

Current per package ..... 4 milliamperes average

HEX INVERTER

7404



TOP VIEW

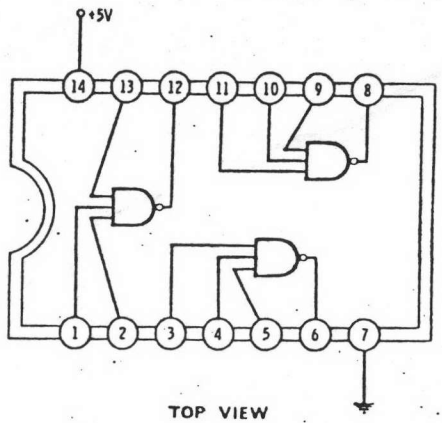
All six inverters may be used independently. On any one inverter, the *low*-input condition drives the output *high*. The *high*-input condition drives the output *low*.

Propagation delay ..... 10 nanoseconds average

Current per package ..... 12 milliamperes average

7410

TRIPLE 3-INPUT NAND GATE



TOP VIEW

All three positive-logic NAND gates may be used independently. On any one gate, when *any* input is *low*, the output is driven to a *high* state. When *all* three inputs are *high*, the output is driven to a *low* state.

Propagation delay ..... 9 nanoseconds average

Current per package ..... 6 milliamperes average

Electrical data of Linear Integrated Circuit

National Semiconductor

Audio, Radio and TV Circuits

LM1889 TV video modulator

general description

The LM1889 is designed to interface audio, color difference, and luminance signals to the antenna terminals of a TV receiver. It consists of a sound subcarrier oscillator, chroma subcarrier oscillator, quadrature chroma modulators, and RF oscillators and modulators for two low-VHF channels.

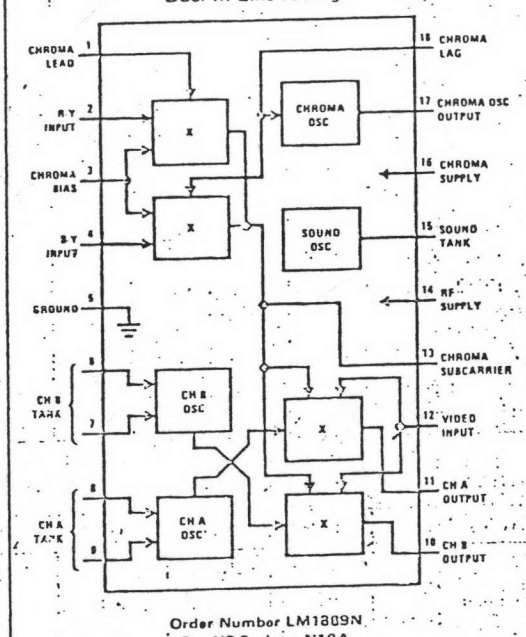
The LM1889 allows video information from VTR's, games, test equipment, or similar sources to be displayed on black and white or color TV receivers. When used with the MM57100 and MM53104, a complete TV game is formed.

features

- dc channel switching
- 12V to 18V supply operation
- Excellent oscillator stability
- Low intermodulation products
- 5 Vp-p chroma reference signal
- May be used to encode composite video

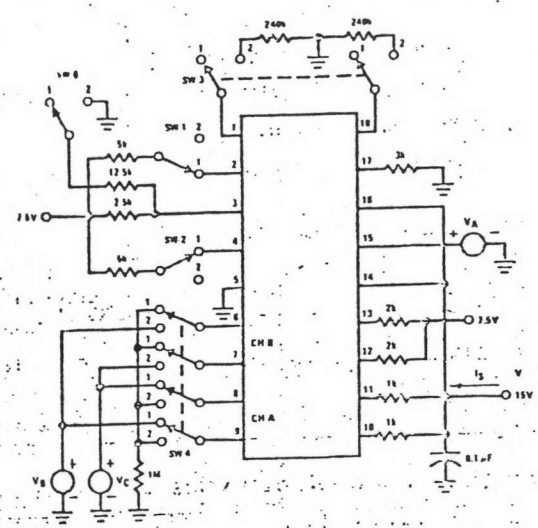
block diagram

Dual-In-Line Package



Order Number LM1889N
See NS Package N18A

dc test circuit



LM1889

2

absolute maximum ratings

Supply Voltage V14, V16 max	19 V_{dc}
Power Dissipation Package (Note 1)	1390 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Chroma Osc Current I_{17} max	10 mA_{dc}
(V16−V15) max	±5 V_{dc}
(V14−V10) max	7V
(V14−V11) max	7V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics (dc Test Circuit, All SW Normally Pos. 1, V = 15V, $V_B = V_C = 12V$)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, I_S		20	35	45	mA
Sound Oscillator, Current Change, ΔI_{15}	Change V_A From 12.5V to 17.5V	0.3	0.6	0.9	mA
Chroma Oscillator Balance, V17		9.5	11.0	12.5	V
Chroma Modulator Balance, V13		7.0	7.4	7.8	V
R-Y Modulator Output Level, ΔV13	SW 3, Pos. 2, Change SW 1 From Pos. 1 to Pos. 2	0.6	0.9	1.2	V
B-Y Modulator Output Level, ΔV13	SW 3, Pos. 2, Change SW 2 From Pos. 1 to Pos. 2	0.6	0.9	1.2	V
Chroma Modulator Conversion Ratio, ΔV13/ΔV3	SW 3, Pos. 2, Change SW 0 From Pos. 1 to Pos. 2. Divide ΔV13 by ΔV3	0.45	0.70	0.95	V/V
Ch. A Oscillator "OFF" Voltage, V8, V9	SW 4, Pos. 2	0.5	1.5	3.0	V
Ch. A Oscillator Current Level, I_9	V_B = 12V, V_C = 13V	2.5	3.5	5	mA
Ch. B Oscillator "OFF" Voltage, V6, V7		0.5	1.5	3.0	V
Ch. B Oscillator Current Level, I_6	SW 4, Pos. 2, V_B = 12V, V_C = 13V	2.5	3.5	5	mA
Ch. A Modulator Conversion Ratio, ΔV11/(V13−V12)	SW 1, SW 2, SW 3, Pos. 2, V_B = 12V, Change V_C From 13V to 11V For ΔV11 Divide By V13−V12	0.40	0.55	0.70	V/V
Ch. B Modulator Conversion Ratio, ΔV10/(V13−V12)	All SW, Pos. 2, V_B = 12V, Change V_C From 13V to 11V Divide as Above	0.40	0.55	0.70	V/V

ac electrical characteristics (ac Test Circuit, V = 15V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Chroma Oscillator Output Level, V17	$C_{LOAD} \leq 20$ pF	4	5		V_{p-p}
Sound Carrier Oscillator Level, V15	Loaded by RC Coupling Network	2	3	4	V_{p-p}
Ch. 3 RF Oscillator Level, V8, V9	Ch. Sw. Pos. 3, f = 61.25 MHz, Use FET Probe	200	350		mV_{p-p}
Ch. 4 RF Oscillator Level, V6, V7	Ch. Sw. Pos. 4, f = 67.25 MHz, Use FET Probe	200	350		mV_{p-p}

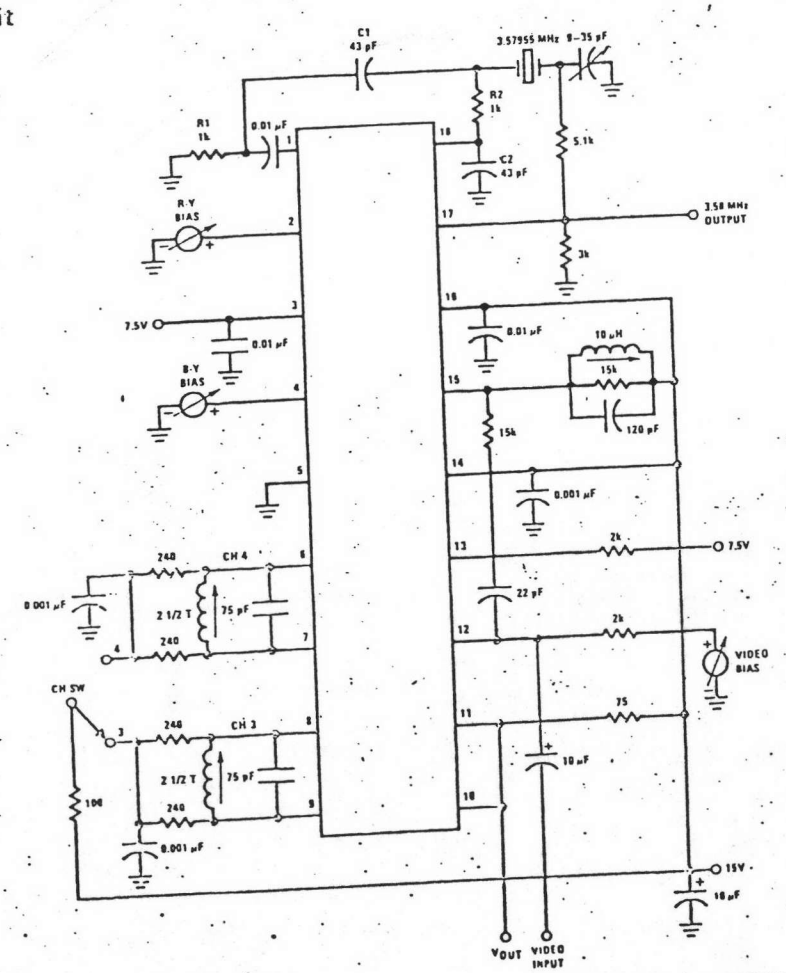
Note 1: For operation in ambient temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 90°C/W junction to ambient.

design characteristics (ac Test Circuit, V = 15V)

PARAMETER	TYP	UNITS
Oscillator Supply Dependence		
Chroma, f_o = 3.579545 MHz	3	Hz/V
Sound Carrier, RF	See Curves	
Oscillator Temperature Dependence (IC Only)		
Chroma	0.05	ppm/°C
Sound Carrier	−.15	ppm/°C
RF	−50	ppm/°C
Chroma Oscillator Output, Pin 17		
t_{RISE}, 10–90%	20	ns
t_{FALL}, 90–10%	30	ns
Duty Cycle (+) Half Cycle	51	%
(−) Half Cycle	49	%
RF Oscillator Maximum Operating Frequency (Temperature Stability Degraded)	100	MHz
Chroma Modulator (f = 3.58 MHz)		
B-Y Conversion Gain V13/(V4−V3)	0.6	Vp-p/V
R-Y Conversion Gain V13/(V2−V3)	0.6	Vp-p/V
Gain Balance	±0.5	dB
Bandwidth	See Curve	

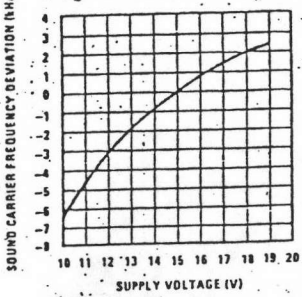
PARAMETER	TYP	UNITS
RF Modulator		
Conversion Gain, f = 61.25 MHz, V_{OUT}/(V13−V12)	10	mVrms/V
3.58 MHz Differential Gain	5	%
Differential Phase	3	degrees
2.5 Vp-p Video, 87.5% mod.		
Output Harmonics Below Carrier		
2nd, 3rd	−12	dB
4th and above	−20	dB
Input Impedances		
Chroma Modulator, Pins 2, 4	500k//2 pF	
RF Modulator, Pin 12	1M//2 pF	
Pin 13	250k//3.5 pF	

ac test circuit

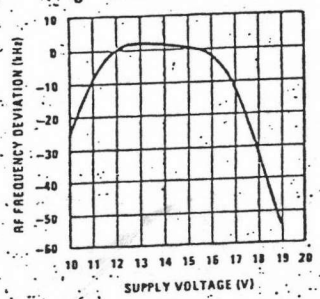


typical performance characteristics

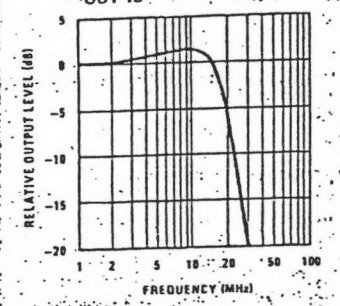
Sound Carrier Oscillator Supply Dependence (f_o = 4.5 MHz)



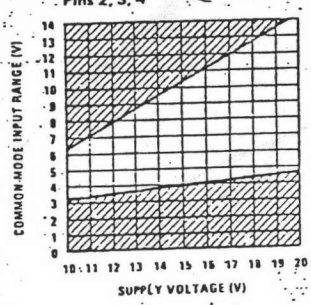
RF Oscillator Frequency Supply Dependence f_o = 67.25 MHz



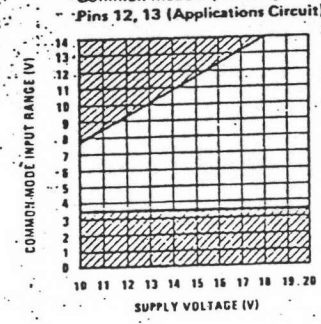
Chroma Modulator Transconductance Bandwidth $I_{OUT\ 13}/V_{1\ or\ 18}$



Chroma Modulator Common-Mode Input Range Pins 2, 3, 4



RF Modulator Common-Mode Input Range Pins 12, 13 (Applications Circuit)



circuit description (Refer to Circuit Diagram)

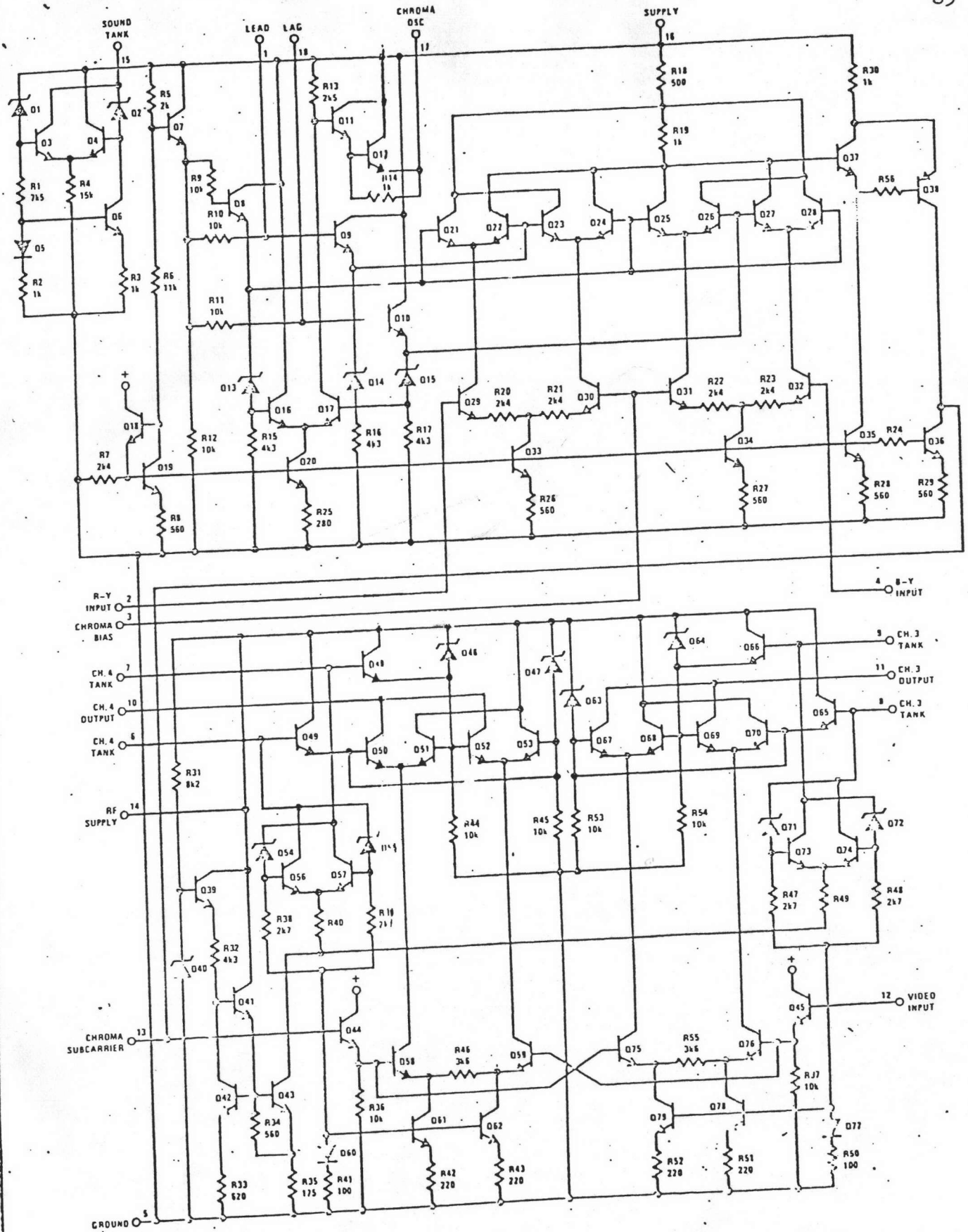
The sound carrier oscillator is formed by differential amplifier Q3, Q4 operated with positive feedback from the pin 15 tank to the base of Q4.

The chroma oscillator consists of the inverting amplifier Q16, Q17 and Darlington emitter follower Q11, Q12. An external RC and crystal network from pin 17 to pin 18 provides an additional 180 degrees phase lag back to the base of Q17 to produce oscillation at the crystal resonance frequency. (See ac test circuit).

The feedback signal from the crystal is split in a lead-lag network to pins 1 and 18, respectively, to generate the subcarrier reference signals for the chroma modulators. The R-Y modulator consists of multiplier devices Q29, Q30 and Q21–Q24, while the B-Y modulator consists of Q31, Q32 and Q25–Q28. The multiplier outputs are coupled through a balanced summing amplifier Q37, Q38 to the input of the RF modulators at pin 13. With 0 offset at the lower pairs of the multipliers, no chroma output is produced. However, when either pin 2 or pin 4 is offset relative to pin 3 a subcarrier output current of the appropriate phase is produced at pin 13.

The channel B oscillator consists of devices Q56 and Q57 cross-coupled through level-shift zener diodes Q54 and Q55. A current regulator consisting of devices Q39–Q43 is used to achieve good RF frequency stability over supply and temperature. The channel B modulator consists of multiplier devices Q58, Q59 and Q50–Q53. The top quad is coupled to the channel B tank through isolating devices Q48 and Q49. A dc offset between pins 12 and 13 offsets the lower pair to produce an output RF carrier at pin 10. That carrier is then modulated by both the chroma signal at pin 13 and the video and sound carrier signals at pin 12. The channel A modulator shares pin 12 and 13 buffers Q45 and Q44 with channel B and operates in an identical manner.

The current flowing through channel B oscillator diodes Q54, Q55 is turned around in Q60, Q61 and Q62 to source current for the channel B RF modulator. In the same manner, the channel A oscillator Q71–Q74 uses turn around Q77, Q78 and Q79 to source the channel A modulator. One oscillator at a time may be activated by connecting its tank to supply (see ac test circuit). The corresponding modulator is then activated by its current turn-around, and the other oscillator/modulator combination remains "OFF".


SOUND TANK
LEAD LAG
CHROMA OSC
SUPPLY
R-Y INPUT
CHROMA BIAS
CH. 4 TANK
CH. 4 OUTPUT
CH. 4 TANK
RF SUPPLY
CHROMA SUBCARRIER
GROUND
B-Y INPUT
CH. 3 TANK
CH. 3 OUTPUT
CH. 3 TANK
VIDEO INPUT

LM380

National Semiconductor

Audio, Radio and TV Circuits

LM380 audio power amplifier general description

The LM380 is a power audio amplifier for consumer application. In order to hold system cost to a minimum, gain is internally fixed at 34 dB. A unique input stage allows inputs to be ground referenced. The output is automatically self entering to one half the supply voltage.

The output is short circuit proof with internal thermal limiting. The package outline is standard dual-in-line. A copper lead frame is used with the center three pins on either side comprising a heat sink. This makes the device easy to use in standard p-c layout.

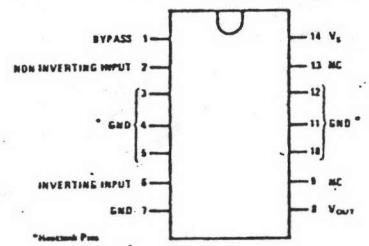
Uses include simple phonograph amplifiers, intercoms, line drivers, teaching machine outputs, alarms, ultrasonic drivers, TV sound systems, AM-FM radio, small servo drivers, power converters,etc.

A selected part for more power on higher supply voltages is available as the LM384. For more information see AN-69.

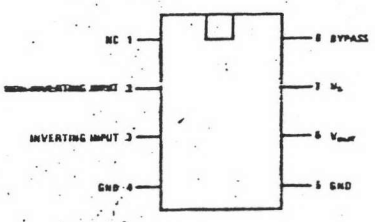
features

- Wide supply voltage range
- Low quiescent power drain
- Voltage gain fixed at 50
- High peak current capability
- Input referenced to GND
- High input impedance
- Low distortion
- Quiescent output voltage is at one-half of the supply voltage
- Standard dual-in-line package

connection diagrams (Dual-In-Line Packages, Top View)



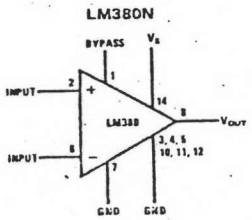
Order Number LM380N
See NS Package N14A



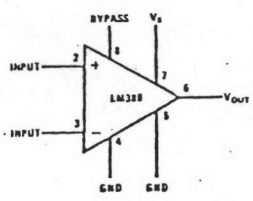
Order Number LM380N-8
See NS Package N08B

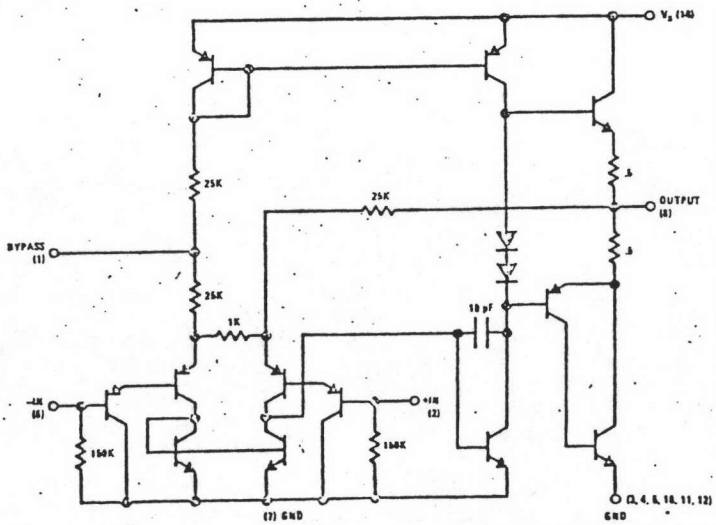
block and schematic diagrams

LM380N



LM380N-8





absolute maximum ratings

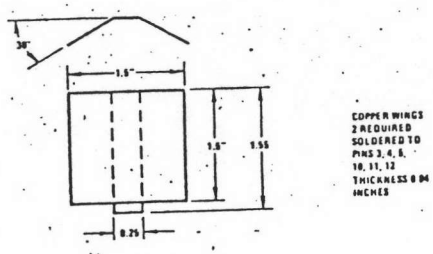
Supply Voltage	22V
Peak Current	1.3A
Package Dissipation 14-Pin DIP (Notes 6 and 7)	10W
Input Voltage	±0.5V
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec)	+300°C

electrical characteristics (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Power	$P_{OUT(RMS)}$	(Notes 3, 4) $R_L = 8\Omega$, THD = 3%	2.5			W
Gain	A_V		40	50	60	V/V
Output Voltage Swing	V_{OUT}	$R_L = 8\Omega$		14		V_{pp}
Input Resistance	Z_{IN}			150k		Ω
Total Harmonic Distortion	THD	(Note 4, 5)		0.2		%
Power Supply Rejection Ratio	PSRR	(Note 2)		38		dB
Supply Voltage	V_S		8		22	V
Bandwidth	BW	$P_{OUT} = 2W$, $R_L = 8\Omega$		100k		Hz
Quiescent Supply Current	I_Q			7	25	mA
Quiescent Output Voltage	V_{OUTQ}		8	9.0	10	V
Bias Current	I_{BIAS}	Inputs Floating		100		nA
Short Circuit Current	I_{SC}			1.3		A

Note 1: $V_S = 18V$ and $T_A = 25°C$ unless otherwise specified.
Note 2: Rejection ratio referred to the output with $C_{BYPASS} = 5\ \mu F$.
Note 3: With device Pins 3, 4, 5, 10, 11, 12 soldered into a 1/16" epoxy glass board with 2 ounce copper foil with a minimum surface of 6 square inches.
Note 4: If oscillation exists under some load conditions, add 2.7Ω and 0.1 μfd series network from Pin 8 to Gnd.
Note 5: $C_{BYPASS} = 0.47\ \mu fd$ on Pin 1.
Note 6: The maximum junction temperature of the LM380 is 150°C.
Note 7: The package is to be derated at 12°C/W junction to heat sink pins.

heat sink dimensions



National Semiconductor

Industrial/Automotive/Functional Blocks/ Telecommunications

LM555/LM555C timer

general description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

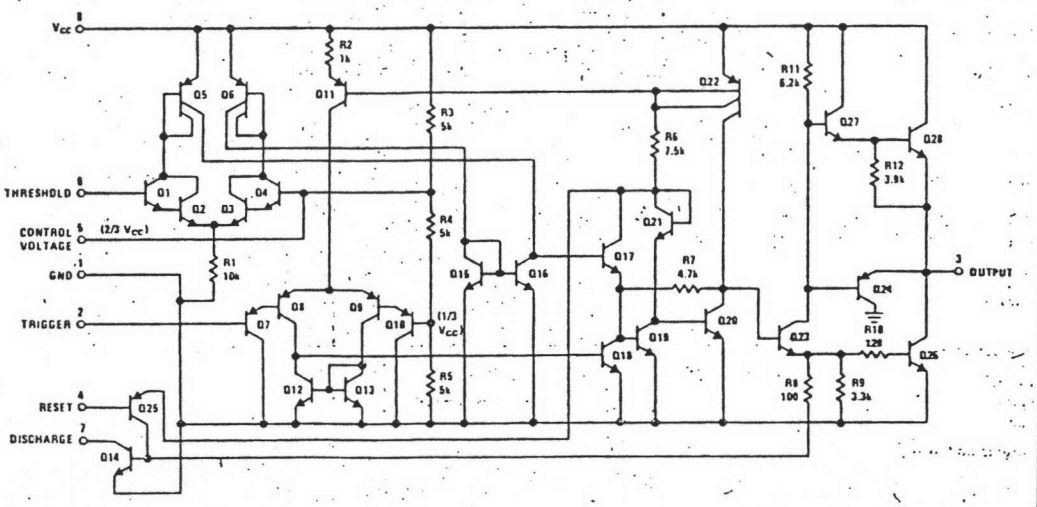
features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

applications

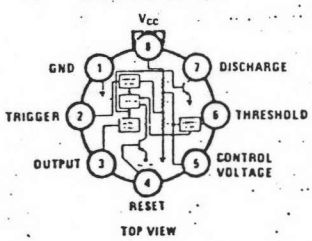
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

schematic diagram



connection diagrams

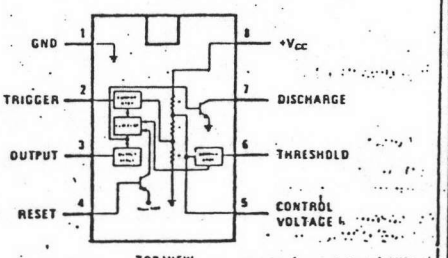
Metal Can Package



TOP VIEW

Order Number LM555H, LM555CH
See NS Package H08C

Dual-In-Line Package



TOP VIEW

Order Number LM555CN
See NS Package N08B

Order Number LM555J or LM555CJ
See NS Package J08A

absolute maximum ratings

Supply Voltage	+18V
Power Dissipation (Note 1)	600 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
LM555	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM555			LM555C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V, R_L = ∞ (Low State) (Note 2)		10	12		10	15	mA
Timing Error, Monostable								
Initial Accuracy			0.5	2		1		%
Drift with Temperature	R_A, R_B = 1k to 100 k, C = 0.1μF, (Note 3)		30			50		ppm/°C
Accuracy over Temperature			1.5	3.0		1.5		%
Drift with Supply			0.05	0.2		0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5	5		2.25	7	%
Drift with Temperature			90			150		ppm/°C
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15	0.2		0.30	0.5	%/V
Threshold Voltage			0.667			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.01	0.5		0.5	0.9	μA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 4)		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 5)								
Output Low	V_{CC} = 15V, I_7 = 15 mA		150			180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5 mA		70	100		80	200	mV
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.2		2	2.5	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							V
	I_{SINK} = 8 mA		0.1	0.25				V
	I_{SINK} = 5 mA					0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of +45° C/W junction to case for TO-5 and +150° C/W junction to ambient for both packages.

Note 2: Supply current when output high typically 1 mA less at V_{CC} = 5V.

Note 3: Tested at V_{CC} = 5V and V_{CC} = 15V.

Note 4: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

Note 5: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

ภาคผนวก ข (ต่อ)

applications information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

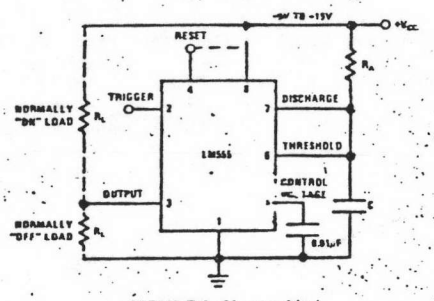


FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1\ R_A C$, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.

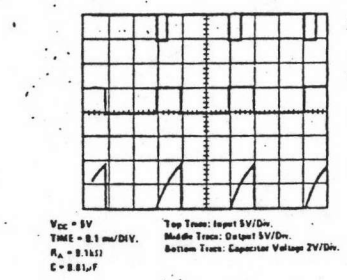


FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a

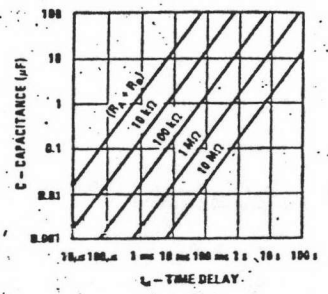


FIGURE 3. Time Delay

multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

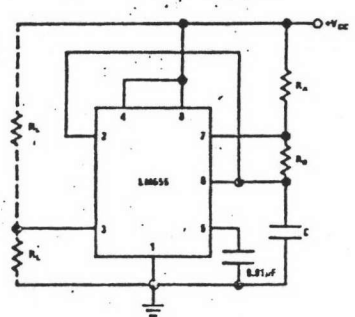


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 5 shows the waveforms generated in this mode of operation.

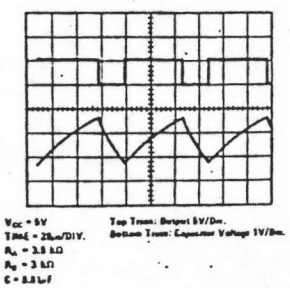


FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

ภาคผนวก ข (ต่อ)

applications information (con't)

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is: $D = \frac{R_B}{R_A + 2R_B}$

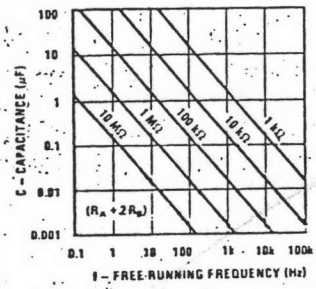


FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.

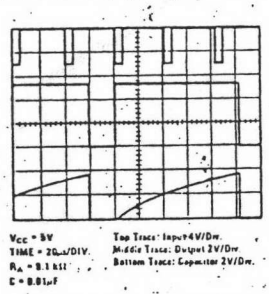


FIGURE 7. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.

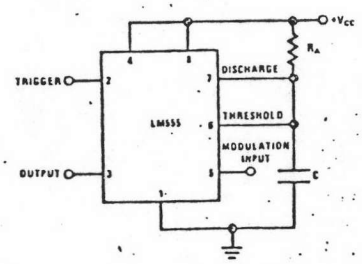


FIGURE 8. Pulse Width Modulator

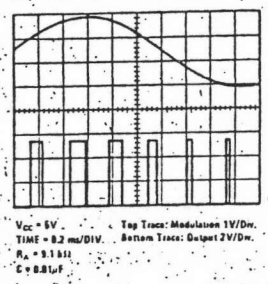


FIGURE 9. Pulse Width Modulator

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

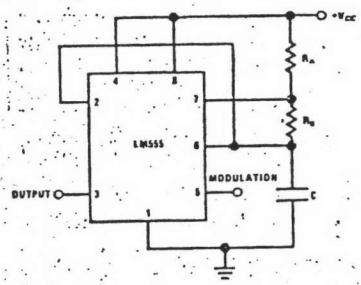


FIGURE 10. Pulse Position Modulator

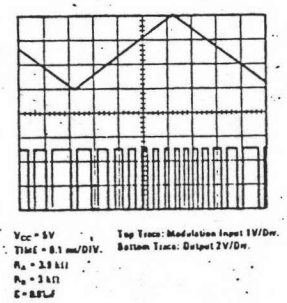


FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is

ภาคผนวก ช (ต่อ)

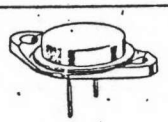
MC7800C Series

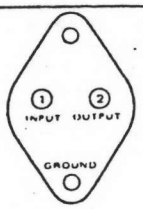
MC7800C SERIES THREE-TERMINAL POSITIVE VOLTAGE REGULATORS

The MC7800C Series of three-terminal positive voltage regulators are monolithic integrated circuits designed as fixed-voltage regulators for a wide variety of applications including local, on-card regulation. Available in seven fixed output voltage options from 5.0-to-24 volts, these regulators employ internal current limiting, thermal shutdown, and safe area compensation — making them essentially blow-out proof. With adequate heatsinking they can deliver output currents in excess of 1.0 ampere. The last two digits of the part number indicate nominal output voltage.

- Output Current in Excess of 1.0 Ampere
- No External Components Required
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Packaged in the Plastic Case 313 and Case 11 (TO-220 and Hermetic TO-3)

THREE-TERMINAL POSITIVE FIXED VOLTAGE REGULATORS



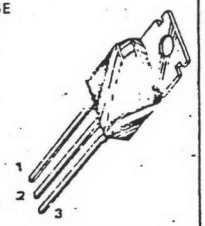


K SUFFIX
METAL PACKAGE
CASE 11-01
(TO-3 TYPE)

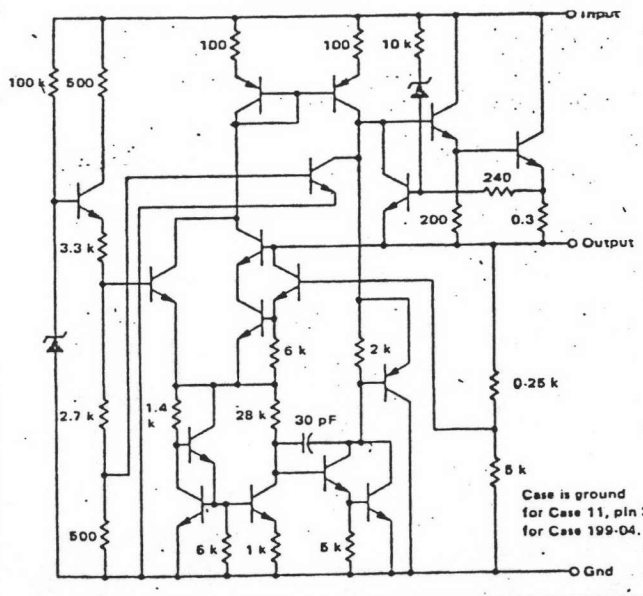
Pins 1 and 2 electrically isolated from case.
Case is third electrical connection.

T SUFFIX
PLASTIC PACKAGE
CASE 313
TO-220 Type

Pin 1. Input
2. Ground
3. Output

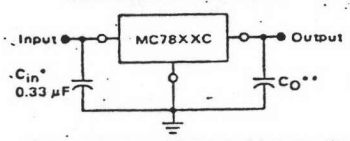


SCHEMATIC DIAGRAM



Case is ground for Case 11, pin 3 for Case 199-04.

STANDARD APPLICATION



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

XX = these two digits of the type number indicate voltage.

* = C_{in} is required if regulator is located an appreciable distance from power supply filter.

** = C_O is not needed for stability; however, it does improve transient response.

XX indicates nominal voltage

TYPE NO./VOLTAGE

MC7805C 5.0 Volts	MC7808C 8.0 Volts	MC7818C 18 Volts
MC7806C 6.0 Volts	MC7812C 12 Volts	MC7824C 24 Volts
	MC7815C 15 Volts	

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE
MC78XXCK	T_J = 0° C to +150° C	Metal Power
MC78XXCT	T_J = 0° C to +150° C	Plastic Power

MC7800C Series MAXIMUM RATINGS (T_J = +25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (5.0 V – 18 V) (24 V)	V_{in}	35 40	Vdc
Power Dissipation and Thermal Characteristics			
Plastic Package			
T_A = +25°C	P_D	Internally Limited	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	15.4	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	65	°C/W
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_C = +95°C (See Figure 1)	$1/\theta_{JC}$	200	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	5.0	°C/W
Metal Package			
T_A = +25°C	P_D	Internally Limited	Watts
Derate above T_A = +25°C	$1/\theta_{JA}$	22.5	mW/°C
Thermal Resistance, Junction to Air	θ_{JA}	45	°C/W
T_C = +25°C	P_D	Internally Limited	Watts
Derate above T_C = +65°C (See Figure 2)	$1/\theta_{JC}$	182	mW/°C
Thermal Resistance, Junction to Case	θ_{JC}	5.5	°C/W
Storage Junction Temperature Range	T_{stg}	−65 to +150	°C
Operating Junction Temperature Range	T_J	0 to +150	°C

MC7805C ELECTRICAL CHARACTERISTICS (V_{in} = 10 V, I_O = 500 mA, 0°C < T_J < +125°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	Vdc
Input Regulation	Reg_{in}				mV
(T_J = +25°C, I_O = 100 mA)					
7.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	7.0	50	
8.0 Vdc ≤ V_{in} ≤ 12 Vdc		–	2.0	25	
(T_J = +25°C, I_O = 500 mA)					
7.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	35	100	
8.0 Vdc ≤ V_{in} ≤ 12 Vdc		–	8.0	50	
Load Regulation	Reg_{load}				mV
T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A		–	11	100	
250 mA ≤ I_O ≤ 750 mA		–	4.0	50	
Output Voltage (7.0 Vdc ≤ V_{in} ≤ 20 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)	V_O	4.75	–	5.25	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.3	8.0	mA
Quiescent Current Change	ΔI_B				mA
7.0 Vdc ≤ V_{in} ≤ 25 Vdc		–	–	1.3	
5.0 mA ≤ I_O ≤ 1.0 A		–	–	0.5	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	40	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	20	mV/1.0 k HRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	70	–	dB
Input-Output Voltage Differential (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	–	2.0	–	Vdc
Output Resistance (I_O = 500 mA)	R_O	–	30	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	750	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	TCV_O	–	-1.0	–	mV/°C

MC7812C ELECTRICAL CHARACTERISTICS (V_{in} = 19 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	Vdc
Input Regulation (T_J = +25°C, I_O = 100 mA) 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 16 Vdc ≤ V_{in} ≤ 22 Vdc (T_J = +25°C, I_O = 500 mA) 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 16 Vdc ≤ V_{in} ≤ 22 Vdc	Reg_{in}	 – – – –	 13 6.0 55 24	 120 60 240 120	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 46 17	 240 120	mV
Output Voltage (14.5 Vdc ≤ V_{in} ≤ 27 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)	V_O	11.4	–	12.6	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.4	8.0	mA
Quiescent Current Change 14.5 Vdc ≤ V_{in} ≤ 30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	75	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	48	mV/1.0kHRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	61	–	dB
Input-Output Voltage Differential (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	 –	 2.0	 –	Vdc
Output Resistance (I_O = 500 mA)	R_O	–	75	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	350	–	mA
Average Temperature Coefficient of Output Voltage (I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C)	TCV_O	 –	 -1.0	 –	mV/°C

MC7815C ELECTRICAL CHARACTERISTICS (V_{in} = 23 V, I_O = 500 mA, $0^oC < T_J < +125^oC$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	Vdc
Input Regulation (T_J = +25°C, I_O = 100 mA) 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 20 Vdc ≤ V_{in} ≤ 26 Vdc (T_J = +25°C, I_O = 500 mA) 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 20 Vdc ≤ V_{in} ≤ 26 Vdc	Reg_{in}	 – – – –	 14 6.0 57 27	 150 75 300 150	mV
Load Regulation T_J = +25°C, 5.0 mA ≤ I_O ≤ 1.5 A 250 mA ≤ I_O ≤ 750 mA	Reg_{load}	 – –	 68 25	 300 150	mV
Output Voltage (17.5 Vdc ≤ V_{in} ≤ 30 Vdc, 5.0 mA ≤ I_O ≤ 1.0 A, P ≤ 15 W)	V_O	14.25	–	15.75	Vdc
Quiescent Current (T_J = +25°C)	I_B	–	4.4	8.0	mA
Quiescent Current Change 17.5 Vdc ≤ V_{in} ≤ 30 Vdc 5.0 mA ≤ I_O ≤ 1.0 A	ΔI_B	 – –	 – –	 1.0 0.5	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_N	–	90	–	μV
Long-Term Stability	$\Delta V_O/\Delta t$	–	–	60	mV/1.0kHRS
Ripple Rejection (I_O = 20 mA, f = 120 Hz)	RR	–	60	–	dB
Input-Output Voltage Differential (I_O = 1.0 A, T_J = +25°C)	$V_{in}-V_O$	 –	 2.0	 –	Vdc
Output Resistance (I_O = 500 mA)	R_O	–	95	–	mΩ
Short-Circuit Current Limit (T_J = +25°C)	I_{SC}	–	230	–	mA
Average Temperature Coefficient of Output Voltage I_O = 5.0 mA, 0°C ≤ T_A ≤ +125°C	TCV_O	 –	 -1.0	 –	mV/°C

ภาคผนวก ค.

Electrical data of Transistors.

型名	社名	用途	構造	最大定格 (T_a = 25°C)					電気的特性 (T_a = 25°C)												外形	備考
				V_{CBO} (V)	V_{EBO} (V)	I_C (mA)	P_C (mW)	T_j (°C)	I_{CBO} 最大値 (μA)	V_{CB}(V)	直流又はパルス h_{FE}	V_{CE}(V)	I_C(mA)	バイアス V_{CB}(V)	I_E(mA)	h_{fe} h_{fe}*	h_{ie} h_{ie}* (Ω)	h_{re} h_{re}* (×10⁻⁴)	h_{oe} h_{oe}* (μU)	f_{ab} f_T* (Mc)	C_{ob} (pF)	$r_{bb'}$ h_{ib}(real)* (Ω)		
2SC452	三菱	PA	Si.TP	100	4	1.2A	25 W (T_c=25°C)	200	500	28	>15	28	350	28	−100	30				180*	20	15*	112	
〃 453	〃	〃	〃	90	4	1.2A	25 W (T_c=25°C)	200	500	28	>10	28	350	28	−100	30				170*	20	15*	112	
〃 454	日立	RF.Conv.Mix Osc	Si.EP	30	5	100	200	125	0.5	18				12	−2	100				230*	1.8	$C_{r\,bb'}$ 100pS	37	
〃 455	〃	〃	〃	30	5	100	200	125	1	18				12	−2	40				230*	1.8	40	37	
〃 456	松下	PA	Si.EP	50	1.5	600	750	175	1	12	12	6	80	6	−80	20				200*	10	$C_{r\,bb'}$ 100pS	84A	
〃 457	日電	Diff	〃	25	5	50	300	175	0.1	10	80	1	1	6	−2		h_{FE1}/h_{FE2}=0.8~1.0			200*	4.5	40*	87B	2素子複合
〃 458	日立	RF	Si.EP	30	5	100	200	125	0.8	18	140	6	2	5	−0.1	130	16.5k	0.7	11	230*	1.8	100	37	
〃 459	〃	RF.Conv.Mix Osc	〃	30	5	100	200	125	1	18	160	12	2	12	−2	110	2800	1.6	20	230*	1.8	100	37	
〃 460	〃	〃	Si.P	30	5	100	200	125	0.5	18				12	−2	85				230*	1.8	40	37	
〃 461	〃	〃	〃	30	5	100	200	125	0.5	18				12	−2	85				230*	1.8	40	37	
〃 462	〃	RF	〃	40	4	50	200	200	0.5	20				10	−4	100	PG=26dB (f=45Mc)			600*	0.9		9	

型名	社名	用途	構造	最大定格 (T_a = 25°C)					電気的特性 (T_a = 25°C)												外形	備考
				V_{CBO} (V)	V_{EBO} (V)	I_C (mA)	P_C (mW)	T_j (°C)	I_{CBO} 最大値 (μA)	V_{CB}(V)	直流又はパルス h_{FE}	V_{CE}(V)	I_C(mA)	バイアス V_{CB}(V)	I_E(mA)	h_{fe} h_{fe}*	h_{ie} h_{ie}* (Ω)	h_{re} h_{re}* (×10⁻⁴)	h_{oe} h_{oe}* (μU)	f_{ab} f_T* (Mc)	C_{ob} (pF)	$r_{bb'}$ h_{ib}(real)* (Ω)		
2SC739	三菱	RF.Conv Mix.Osc	Si.EP	25	4	20	150	125	1	12				6	−1	60				350*	1.5	$C_{r\,bb'}$ 30pS	40	
〃 740	〃	〃	〃	25	2	20	150	150	0.5	10	40	10	10	10	−10	40				900*	1.4	$C_{r\,bb'}$ 8 pS	11A	
〃 741	〃	PA	〃	40	4	300	680	175	1	15	50	10	100				P_o=0.3W (f=150Mc, V_{CC}=13.5V, P_{in}=10mW)						84B	再登録
〃 742	富士通	〃	〃	65	4	1.5A	12.5W (T_c=25°C)	175	5	30				10	−150	30				400*	8	10*	111	
〃 743	〃	〃	〃	65	4	3 A	25 W (T_c=25°C)	175	10	30				10	−300	30				350*	16	7*	111	
〃 744																								
〃 745	富士通	PA	Si.EP	50	4	1.5A	12.5W (T_c=25°C)	175	10	10				10	−150	45				450*	7	8*	111	
〃 746	〃	〃	〃	45	4	3 A	25 W (T_c=25°C)	175	20	10				10	−300	35				400*	20	6*	111	
〃 747																								
〃 748	富士通	PA	Si.EP	36	4	1 A	12.5W (T_c=25°C)	175	10	10				10	−150	25				400*	16	7*	111	
〃 749	〃	〃	〃	36	4	2 A	25 W (T_c=25°C)	175	25	10				10	−300	25				350*	32	5*	111	
〃 750																								
〃 751	東芝	RF	Si.EP	20	2	20	100	150	1	10				10	−8	50				650*	1.9	30	46C	
〃 752	〃	〃	〃	30	4	100	100	125	0.8	20				10	−10	80				300*	4	30	33	
〃 753	日電	RF.Conv.Mix Osc	〃	25		20	100	150	1	12				6	−2	70				1100*	0.7	$C_{r\,bb'}$ 12pS	23	
〃 754	〃	RF.AF	〃	20		150	150	150	1	20	100	1	20	6	−1	80				90*	6.5	25	23	
〃 755	〃	RF	〃	15		100	150	150	0.1	15	270	3	0.5	3	−0.5	300	15kΩ	16	3	100*	8	30*	23	
〃 756	ソニー	PA	Si.E	100	6	4 A	10 W (T_c=25°C)	175	3	50	80	2	100	10	−50	60				65*	35	$C_{r\,bb'}$ 80pS	84C	

型名	社名	用途	構造	最大定格 (T_a = 25°C)					電気的特性 (T_a = 25°C)												外形	備考
				V_{CBO} (V)	V_{EBO} (V)	I_C (mA)	P_C (mW)	T_j (°C)	I_{CBO} 最大値 (μA)	V_{CB}(V)	直流又はパルス h_{FE}	V_{CE}(V)	I_C(mA)	バイアス V_{CB}(V)	I_E(mA)	h_{fe} h_{fe}*	h_{ie} h_{ie}* (Ω)	h_{re} h_{re}* (×10⁻⁴)	h_{oe} h_{oe}* (μU)	f_{ab} f_T* (Mc)	C_{ob} (pF)	$r_{bb'}$ h_{ib}(real)* (Ω)		
2SC1211	三菱	RF.PA	Si.EP	65	4	500	500	125	1	25	100	2	150	6	−10					150*	10	$C_{r\,bb'}$ 100pS	138B	2SA697とコンプリ
〃 1212	日立	RF	〃	50	4	1 A	750	150	5	50	180	4	50	4	−30					160*	30	4*	160	再登録
〃 1213	〃	〃	〃	35	4	500	400	125	0.5	20	180	3	10	6	−1					50*	5	9*	170	2SA673とコンプリ
〃 1214	〃	〃	〃	50	4	500	600	125	0.5	20	180	3	10	6	−1					50*	5	9*	170	
〃 1215	松下	〃	〃	30	3	50	200	125	100	30	100	10	2	10	−10					1200*	C_{re} 1pF	30	138	
〃 1216	日電	SW	Si.E	40	5	200	300	150	0.1	30	140	1	10	10	−10		t_{on}<20nS, t_{off}<40nS t_{stg}<20nS			500*	3		49C	
〃 1217	〃	RF.SW	〃	150	5	300	750	175	0.1	100	70	10	50	10	−50					250*	3.7	13*	84B	
〃 1218	〃	〃	〃	80	5	500	750	175	0.1	50	80	10	50	10	−50					370*	3.5	20*	84B	
〃 1219	富士通	RF	Si.EP	30	5	500	200	125	1	12	160	2	100	6	−1					60*	12	70*	138	
〃 932	〃	〃	〃	30		3 A	10 W (T_c=25°C)	125	1 mA	25	70	2	1 A	5	−0.5A					120*	100	35	120	
〃 933	〃	RF.AF	Si.EP	50	5	300	300	125	1	45	150	5	20	6	−5					300*	5	$C_{r\,bb'}$ 120pS	138	
〃 934	〃	〃	〃	20	5	300	300	125	1	15	150	5	20	6	−5					300*	5	$C_{r\,bb'}$ 120pS	138	
〃 935	日立	PA	Si.TMe	300	5	2.5A	50 W (T_c=25°C)	150	I_{CBO} 1mA	300	14	10	300	15	−200					5*	75	20	102	
〃 936	〃	〃	〃	1000	5	1 A	22 W	125	I_{CBO} 1mA	500	45	10	100	15	−200					7*	35	25	102	

ภาคผนวก (ง)

การคำนวนความถี่ของอาร์เอฟออสซิเลเตอร์

จากรูป 2.36 การคำนวนหาค่า C_b เมื่อรู้ค่า L_b และความถี่รีโซแนนซ์ (resonance) จากสมการของวงจรแทงค์เมื่อเกิดรีโซแนนซ์จะได้

$$f_o = \frac{1}{2\pi\sqrt{L_b C_b}}$$

ในที่นี้ f_o คือความถี่อาร์เอฟออสซิลเลเตอร์เท่ากับ 62.25 เมกกะเฮิทซ์

L_b คือค่าของอินดักแตนซ์ (inductance) ของคอล์ยเท่ากับ 0.08 ไมโครเฮนรี่

C_b คือค่าคาพิซิแตนซ์ที่ต้องการ

$$C_b = \frac{1}{4\pi^2 f_o^2 L_b}$$

แทนค่าได้

$$C_b = \frac{1}{4\pi^2 x(62.5x10^6)^2 x0.08x10^{-6}}$$

$$= 81x10^{-12}$$

จึงเลือก C_b = 82 PF

ประวัติผู้เขียน

นายวิชัย สุรพัฒน์ เกิดเมื่อวันที่ 14 มกราคม 2486 ณ. จังหวัดอุบลราชธานี สำเร็จการศึกษาวิศวกรรมศาสตร์บัณฑิต จากคณะวิศวกรรมศาสตร์ สถาบันเทคโนโลยี-พระจอมเกล้าวิทยาเขตเจ้าคุณทหาร ลาดกระบังเมื่อปีพ.ศ. 2514 เคยทำงานที่สถานีโทรทัศน์ช่อง 4 ฝ่ายช่างมีประสบการณ์ทางด้านโทรทัศน์มากกว่า 8 ปี พ.ศ. 2518 ได้รับทุนภายใต้แผนโคลัมโบเดินทางไปศึกษาอบรมและดูงานที่สถานีโทรทัศน์ NHK ประเทศญี่ปุ่น ในสาขาวิชาวิศวกรรมโทรทัศน์ เป็นเวลา 3 เดือน เคยเขียนตำรา " ทฤษฎีโทรทัศน์" เมื่อปี 2518 ปี 2523ได้รับทุนไปศึกษาอบรมดูงานทางด้าน " Television Broadcasting Management " ที่ " Ministry of Posts and Telecommunications " ณ. กรุงโตเกียวประเทศญี่ปุ่นเป็นเวลา 42 วัน

ปัจจุบันรับราชการเป็นอาจารย์ประจำภาควิชาเทคนิคอุตสาหกรรมสาขาวิชาเทคโนโลยีโทรทัศน์ ในตำแหน่งอาจารย์ระดับ 4 ที่สถาบันเทคโนโลยีพระจอมเกล้า วิทยาเขตเจ้าคุณทหาร ลาดกระบัง ตั้งแต่ วันที่ 15 เดือน พฤษภาคม 2517