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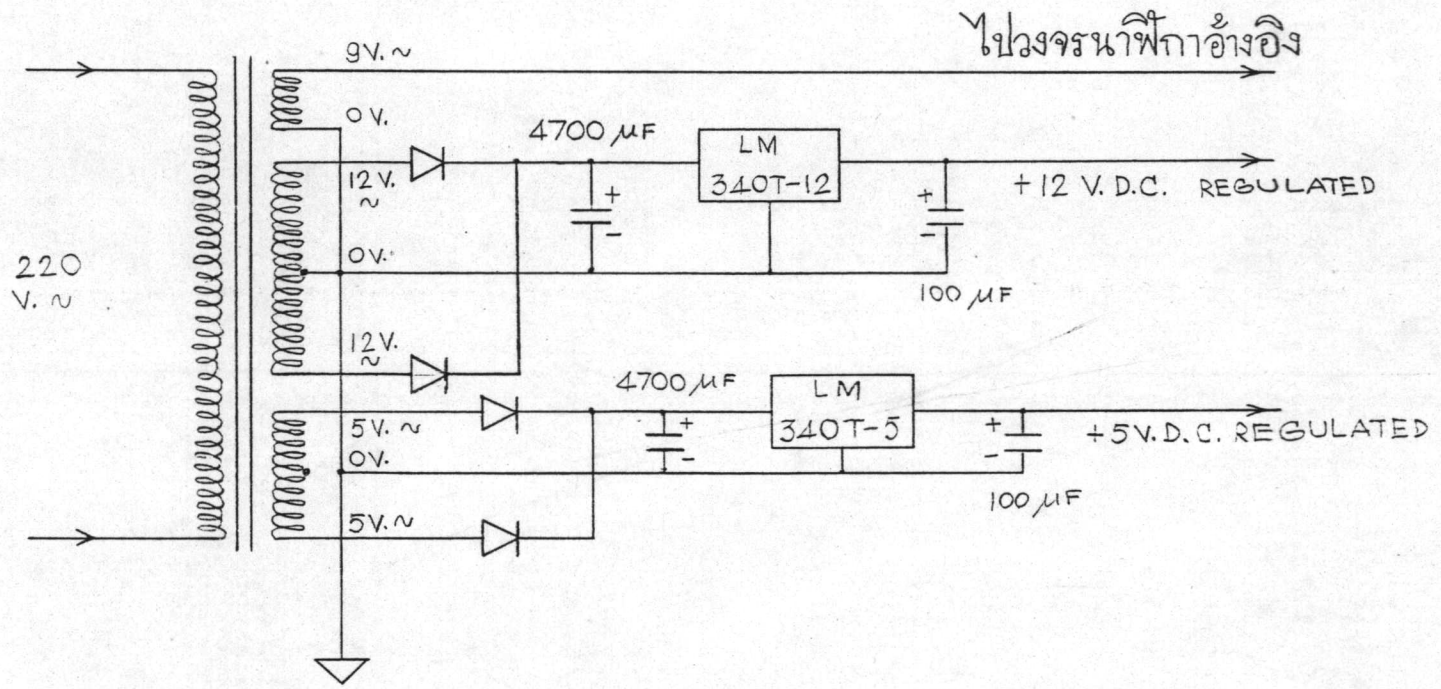
ภาคผนวก

ภาคผนวก ก

วงจรจ่ายไฟตรง



วงจรจ่ายไฟตรง

หมายเหตุ สายดินของวงจรนี้ต่อกับสายดินของเครื่อง SMC 8080

ภาคผนวก ข

ข้อกำหนดของเครื่อง SMC 8080 และคำสั่งของไมโครโพรเซสเซอร์ 8080

ข้อกำหนดของเครื่อง SMC-8080

1. วงจรทั้งหมดของเครื่อง SMC-8080 รวมทั้งคีย์บอร์ด (Keyboard) และไดโอดเปล่งแสง ถูกบรรจุอยู่บนแผ่นวงจรพิมพ์สองหน้าแผ่นเดียว ที่มีขนาดกว้าง 9 นิ้ว ยาว 12 นิ้ว

2. ใช้สัญญาณนาฬิกา 2 เมกกะเฮิกซ์ (M Hz.)

3. มีหน่วยความจำชั่วคราว (RAM) 1 กิโลไบท์ (Kilo-byte) มีที่ให้ขยายได้ถึง 2 กิโลไบท์ บนแผ่นวงจรพิมพ์

4. มีหน่วยความจำถึงถาวร (EPROM) 1 กิโลไบท์ มีที่ให้ขยายได้ถึง 2 กิโลไบท์ บนแผ่นวงจรพิมพ์

5. ในหน่วยความจำถึงถาวรมีโปรแกรมควบคุมการทำงานของเครื่อง (Monitor Programme) อยู่ประมาณ 600 ไบท์ ซึ่งควบคุมการรับข้อมูลจากคีย์บอร์ด การส่งข้อมูลไปแสดงผลบนไดโอดเปล่งแสง การอ่านและการเขียนข้อมูลในหน่วยความจำและการเอ็กซิคิวโปรแกรม

6. สามารถตั้งให้เครื่องทำงานทีละคำสั่งได้

7. สามารถตั้งจุดเบรคพอยท์ (Break Point) ได้

8. ดูค่ารีจีสเตอร์ทุกตัวในหน่วยจัดการข้อมูลกลาง (CPU) ระหว่างเอ็กซิคิวโปรแกรมได้

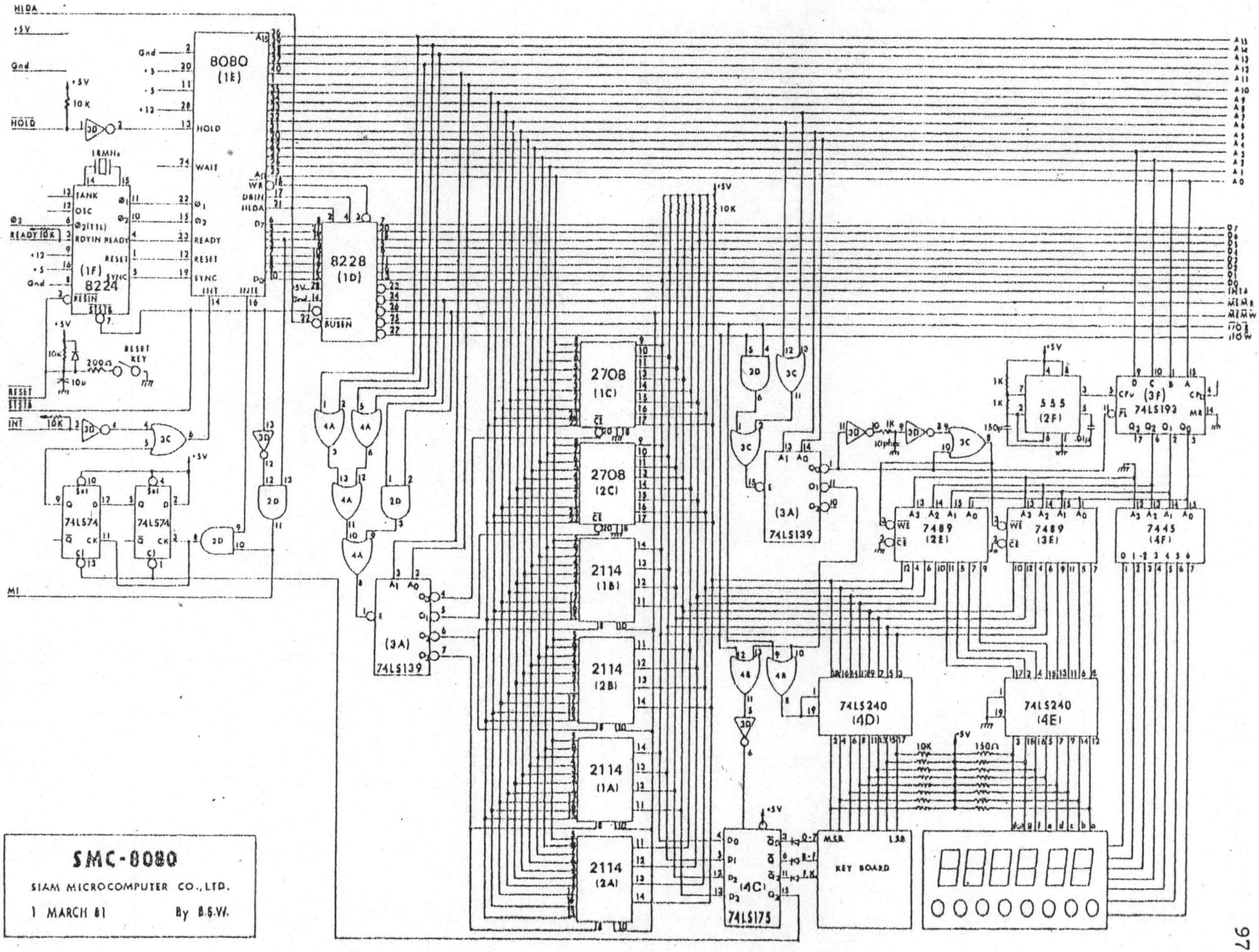
9. มีขั้วต่อสายสำหรับนำไปควบคุมวงจรภายนอกหรือขยายขีดความสามารถของเครื่อง 40 สาย คือ บัสแอดเดรส 16 สาย บัสข้อมูล 8 สาย บัสควบคุม 13 สาย สัญญาณนาฬิกา ϕ_2 (TTL) แหล่งจ่ายไฟ +5V และ 0V ซึ่งจะสามารถจ่ายกระแสให้วงจรภายนอกได้ 500 mA

10. แหล่งจ่ายไฟใช้ไฟสลับขาเข้า 220 โวลท์ จ่ายไฟตรงขาออกที่เรกูเลต (Regulated) แล้ว 3 ระดับคือ +5V 1.5A, +12V 200mA, -5V 100mA.

SMC - 8080 RESTART INTRUCTION

```
0000    C3 3B 00    RESET    JMP  START     ; RESET, RESTART O
0003    00                    NOP
0004    00                    NOP
0005    00                    NOP
0006    00                    NOP
0007    00                    NOP
0008    C3 D9 OF              JMP  RARSTl    ; RESTART 1
000B    00                    NOP
000C    00                    NOP
000D    00                    NOP
000E    00                    NOP
000F    00                    NOP
0010    C3 DC OF              JMP  RARST2    ; RESTART 2
0013    00                    NOP
0014    00                    NOP
0015    00                    NOP
0016    00                    NOP
0017    00                    NOP
0018    C3 DF OF              JMP  RARST3    ; RESTART 3
001B    00                    NOP
001C    00                    NOP
001D    00                    NOP
```

```
001E    00              NOP
001F    00              NOP
0020    C3 E2 OF        JMP   RARST4     ; RESTART 4
0023    00              NOP
0024    00              NOP
0025    00              NOP
0026    00              NOP
0027    00              NOP
0028    C3 E5 OF        JMP   RARST5     ; RESTART 5
002B    00              NOP
002C    00              NOP
002D    00              NOP
002E    00              NOP
002F    00              NOP
0030    C3 E8 OF        JMP   RARST6     ; RESTART 6
0033    00              NOP
0034    00              NOP
0035    00              NOP
0036    00              NOP
0037    00              NOP
0038    C3 71 01        JMP   RSTADR     ; RESTART 7
```



CIRCUIT DIAGRAM

คำสั่งของไมโครโพรเซสเซอร์ 8080

8080 Instruction Set (Intel Corp. Summary)

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
MOV r1,r2	Move register to register	0	1	D	D	D	S	S	S	5
MOV M r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r M	Move memory to register	0	1	D	D	D	1	1	0	7
HLT	Halt	0	1	1	1	0	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
INR r	Increment register	0	0	D	D	D	1	0	0	5
DCR r	Decrement register	0	0	D	D	D	1	0	1	5
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive Or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10
JZ	Jump on zero	1	1	0	0	1	0	1	0	10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10
JP	Jump on positive	1	1	1	1	0	0	1	0	10
JM	Jump on minus	1	1	1	1	1	0	1	0	10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
CALL	Call unconditional	1	1	0	0	1	1	0	1	17
CC	Call on carry	1	1	0	1	1	1	0	0	11/17
CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17
CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
CP	Call on positive	1	1	1	1	0	1	0	0	11/17
CM	Call on minus	1	1	1	1	1	1	0	0	11/17
CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	5/11
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11

Mnemonic	Description	Instruction Code[1] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock[2] Cycles
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
RP	Return on positive	1	1	1	1	0	0	0	0	5/11
RM	Return on minus	1	1	1	1	1	0	0	0	5/11
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
RST	Restart	1	1	A	A	A	1	1	1	11
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
LXI B	Load immediate register Pair B & C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D & E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H & L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
PUSH B	Push register Pair B & C on stack	1	1	0	0	0	1	0	1	11
PUSH D	Push register Pair D & E on stack	1	1	0	1	0	1	0	1	11
PUSH H	Push register Pair H & L on stack	1	1	1	0	0	1	0	1	11
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	11
POP B	Pop register pair B & C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register pair D & E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register pair H & L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
XCHG	Exchange D & E, H & L Registers	1	1	1	0	1	0	1	1	4
XTHL	Exchange top of stack, H & L	1	1	1	0	0	0	1	1	18
SPHL	H & L to stack pointer	1	1	1	1	1	0	0	1	5
PCHL	H & L to program counter	1	1	1	0	1	0	0	1	5
DAD B	Add B & C to H & L	0	0	0	0	1	0	0	1	10
DAD D	Add D & E to H & L	0	0	0	1	1	0	0	1	10
DAD H	Add H & L to H & L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H & L	0	0	1	1	1	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
INX B	Increment B & C registers	0	0	0	0	0	0	1	1	5
INX D	Increment D & E registers	0	0	0	1	0	0	1	1	5
INX H	Increment H & L registers	0	0	1	0	0	0	1	1	5
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5
DCX B	Decrement B & C	0	0	0	0	1	0	1	1	5
DCX D	Decrement D & E	0	0	0	1	1	0	1	1	5
DCX H	Decrement H & L	0	0	1	0	1	0	1	1	5
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
SHLD	Store H & L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H & L direct	0	0	1	0	1	0	1	0	16
EI	Enable interrupts	1	1	1	1	1	0	1	1	4
DI	Disable interrupt	1	1	1	1	0	0	1	1	4
NOP	No operation	0	0	0	0	0	0	0	0	4

NOTES: 1. DDD or SSS – 000 B – 001 C – 010 D – 011 E – 100 H – 101 L – 110 Memory – 111 A.
2. Two possible cycle times, (5/11) indicate instruction cycles dependent on condition flags.

ภาคผนวก ค

ข้อมูลจำเพาะของอุปกรณ์อีเล็คโทรนิคส์

1N4001 thru 1N4007

$V_R = 50\text{-}1000$ V
$I_O = 1$ A

CASE 59

Surmetic rectifiers, subminiature size, axial lead mounted rectifiers for general purpose low-power applications.

MAXIMUM RATINGS

Rating	Symbol	1N4001	1N4002	1N4003	1N4004	1N4005	1N4006	1N4007	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	$V_{RM(rep)}$ $V_{RM(wkg)}$ V_R	50	100	200	400	600	800	1000	Volts
Non-Repetitive Peak Reverse Voltage (halfwave, single phase, 60 Hz peak)	$V_{RM(non-rep)}$	60	120	240	480	720	1000	1200	Volts
RMS Reverse Voltage	V_r	35	70	140	280	420	560	700	Volts
Average Rectified Forward Current (single phase, resistive load, 60 Hz, see Figure 6, T_A = 75°C)	I_O	1.0							Amp
Non-Repetitive Peak Surge Current (surge applied at rated load conditions, see Figure 2)	$I_{FM(surge)}$	30 (for 1 cycle)							Amp
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +175							°C

ELECTRICAL CHARACTERISTICS

Characteristic and Conditions	Symbol	Max	Unit
Maximum Instantaneous Forward Voltage Drop (i_F = 1.0 Amp, T_J = 25°C) Figure 1	V_F	1.1	Volts
Maximum Full-Cycle Average Forward Voltage Drop (I_O = 1.0 Amp, T_L = 75°C, 1 inch leads)	$V_{F(AV)}$	0.8	Volts
Maximum Reverse Current (rated dc voltage) T_J = 25°C T_J = 100°C	I_R	0.01 0.05	mA
Maximum Full-Cycle Average Reverse Current (I_O = 1.0 Amp, T_L = 75°C, 1 inch leads)	$I_{R(AV)}$	0.03	mA

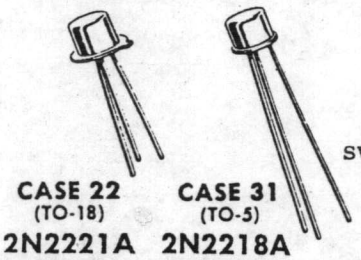
SWITCHING DIODES/RECTIFIERS

IN ORDER OF: (1)RECOVERY TIME-trr (2)If (3)PIV & (4)TYPE No.

4 TYPE No.	3 PIV	RECOVERY TIME 1 trr	TEST CONDITIONS 2 If	Vr	Zr	Ir	RL	CKT	di/dt	MIN. FORWARD CURRENT at 25°C IF	at Vf	MAX. REVERSE CURRENT Ir @25°C & Vr	Ir at T & Vr	TEMP T	TEST VOLT Vr	CAP. at ZERO	ABSOLUTE MAX RATING AVG. FWD I	MAX. TEMP	MAT.	DESCRIPTION DWG. No.
	(V)	(s)	(A)	(V)	(Ω)	(A)	(Ω)		(A/us)	(A)	(V)	(A)	(A)	(°C)	(V)	VOLTS (F)	(A)	(°C)		
SFD183	70	4.0nⓓ	10m	6.0			100			10m	1.0 Δ	1.0u				4.0pⓓ	75m	175S	Si=	DO7
1N914	75 $	4.0nⓓ	10m	6.0		1.0mØ				10m	1.0 Δ	5.0u	50u	150A	20	4.0pⓓ	75m	150A	SiΔ§	A398
1N914A	75 $	4.0nⓓ	10m	6.0		1.0mØ	100			20m	1.0 Δ	5.0u	50u	150A	20	4.0pⓓ	75m	175A	Si	A398

2N2222A

ALSO AVAILABLE AS JAN AND HI-REL UNITS



CASE 22 (TO-18)
2N2221A
2N2222A

CASE 31 (TO-5)
2N2218A
2N2219A

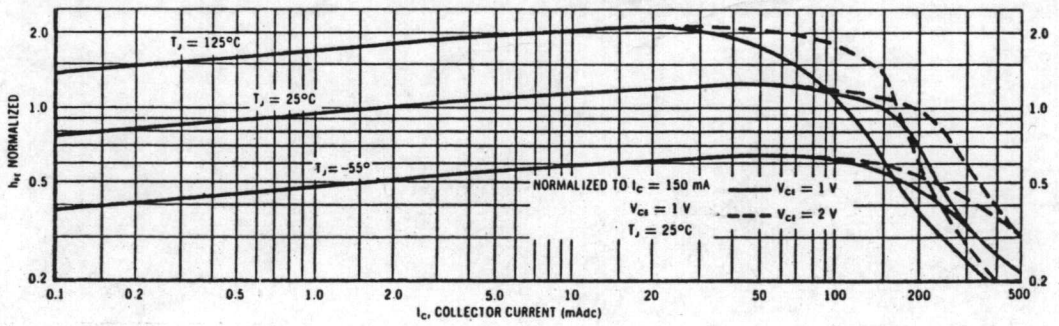
NPN silicon annular Star transistors for high-speed switching and DC to VHF amplifier applications.

Collector connected to case

MAXIMUM RATINGS

Rating	Symbol	2N2218A 2N2219A (TO-5)	2N2221A 2N2222A (TO-18)	Unit
Collector-Base Voltage	V_{CB}	75	75	Vdc
Collector-Emitter Voltage	V_{CEO}	40	40	Vdc
Emitter-Base Voltage	V_{EB}	6	6	Vdc
Total Device Dissipation at 25°C Case Temperature Derating Factor Above 25°C	P_D	3 20	1.8 12	Watts mW/°C
Total Device Dissipation at 25°C Ambient Temperature Derating Factor Above 25°C	P_D	0.8 5.33	0.5 3.33	Watts mW/°C
Junction Temperature Range	T_J	-65 to +175		°C
Storage Temperature Range	T_{stg}	-65 to +200		°C

TYPICAL CURRENT GAIN CHARACTERISTICS



2N2218A, 2N2219A, 2N2221A, 2N2222A (continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

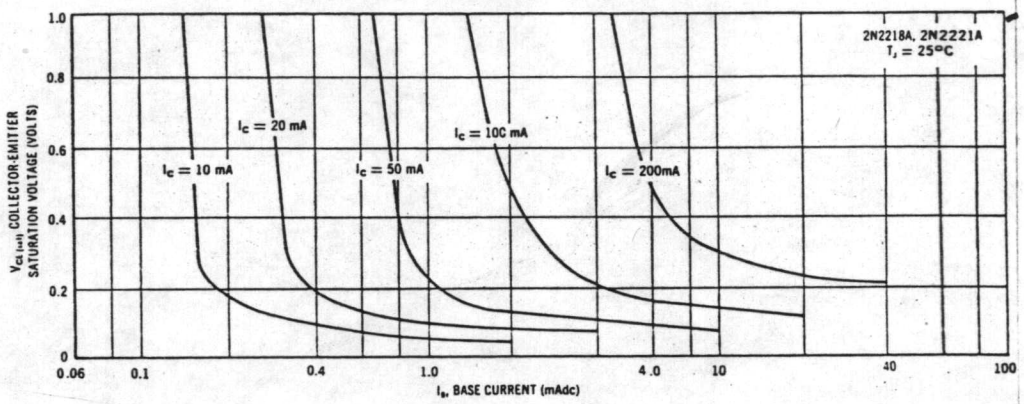
Static Characteristics		Symbol	Min	Max	Unit
Collector-Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	All Types	BV_{CBO}	75	—	Vdc
Collector-Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	All Types	BV_{CEO}	40	—	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	All Types	BV_{EBO}	6	—	Vdc
Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0)	All Types	I_{CBO}	—	0.01	μAdc
(V_{CB} = 60 Vdc, I_E = 0, T_A = 150°C)	All Types		—	10	
Collector Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	All Types	I_{CEX}	—	10	nAdc
Base Cutoff Current (V_{CE} = 60 Vdc, $V_{EB(off)}$ = 3.0 Vdc)	All Types	I_{BL}	—	20	nAdc
Emitter Cutoff Current (V_{BE} = 3 Vdc, I_C = 0)	All Types	I_{EBO}	—	10	nAdc
Collector-Emitter Saturation Voltage* (I_C = 150 mAdc, I_B = 15 mAdc)	All Types	$V_{CE(sat)}$*	—	0.3	Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)	All Types		—	1.0	
Base-Emitter Saturation Voltage* (I_C = 150 mAdc, I_B = 15 mAdc)	All Types	$V_{BE(sat)}$*	0.6	1.2	Vdc
(I_C = 500 mAdc, I_B = 50 mAdc)	All Types		—	2.0	
DC Forward Current Transfer Ratio* (I_C = 0.1 mAdc, V_{CE} = 10 Vdc)	2N2218A, 2N2221A	h_{FE}*	20	—	—
	2N2219A, 2N2222A		35	—	
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)	2N2218A, 2N2221A		25	—	
	2N2219A, 2N2222A		50	—	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)	2N2218A, 2N2221A		35	—	
	2N2219A, 2N2222A		75	—	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, T_A = -55°C)	2N2218A, 2N2221A		15	—	
	2N2219A, 2N2222A		35	—	
(I_C = 150 mAdc, V_{CE} = 10 Vdc)	2N2218A, 2N2221A		40	120	
	2N2219A, 2N2222A		100	300	
(I_C = 150 mAdc, V_{CE} = 1.0 Vdc)	2N2218A, 2N2221A		20	—	
	2N2219A, 2N2222A		50	—	
(I_C = 500 mAdc, V_{CE} = 10 Vdc)	2N2218A, 2N2221A		25	—	
	2N2219A, 2N2222A		40	—	

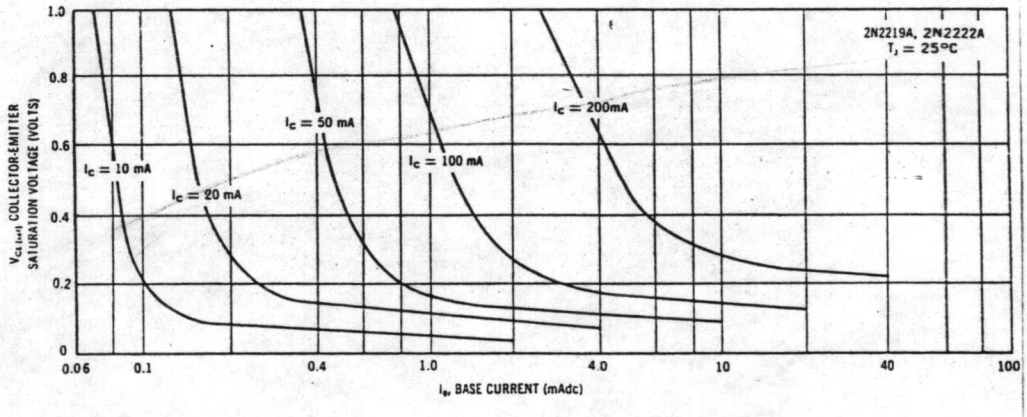
* Pulse Test ≤300 μs, duty cycle ≤2%

SMALL SIGNAL CHARACTERISTICS		Symbol	Min	Max	Unit
Small Signal Current Gain (I_C = 1.0 mA, V_{CE} = 10 V, f = 1 kHz)	2N2218A, 2N2221A	h_{fe}	30	150	—
	2N2219A, 2N2222A		50	300	
(I_C = 10 mA, V_{CE} = 10 V, f = 1 kHz)	2N2218A, 2N2221A		50	300	
	2N2219A, 2N2222A		75	375	
Voltage Feedback Ratio (I_C = 1.0 mA, V_{CE} = 10 V, f = 1 kHz)	2N2218A, 2N2221A	h_{re}	-	5	$X10^{-4}$
	2N2219A, 2N2222A		-	8	
(I_C = 10 mA, V_{CE} = 10 V, f = 1 kHz)	2N2218A, 2N2221A		-	2.5	
	2N2219A, 2N2222A		-	4	
Input Impedance (I_C = 1.0 mA, V_{CE} = 10 V, f = 1 kHz)	2N2218A, 2N2221A	h_{ie}	1	3.5	k ohms
	2N2219A, 2N2222A		2.0	8	
(I_C = 10 mA, V_{CE} = 10 V, f = 1 kHz)	2N2218A, 2N2221A		0.2	1.0	
	2N2219A, 2N2222A		0.25	1.25	
Output Admittance (I_C = 1.0 mA, V_{CE} = 10 V, f = 1 kHz)	2N2218A, 2N2221A	h_{oe}	3	15	μmhos
	2N2219A, 2N2222A		5	35	
(I_C = 10 mA, V_{CE} = 10 V, f = 1 kHz)	2N2218A, 2N2221A		10	100	
	2N2219A, 2N2222A		25	200	
Collector-Base Time Constant (I_C = 20 mA, V_{CE} = 20 V, f = 31.8 MHz)		$r'_b C_c$	-	150	ps
Noise Figure (I_C = 100μA, V_{CE} = 10 V, Rg = 1 kΩ, f = 1 kHz)	2N2219A, 2N2222A	NF	-	4	dB

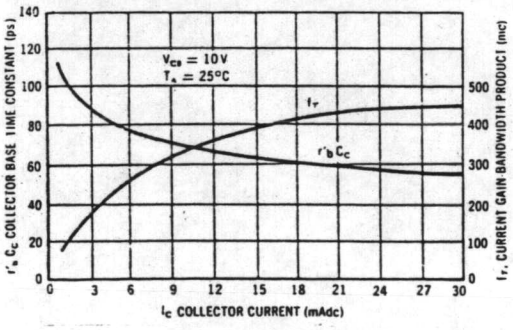
2N2218A, 2N2219A, 2N2221A, 2N2222A (continued)

COLLECTOR SATURATION VOLTAGE versus BASE CURRENT

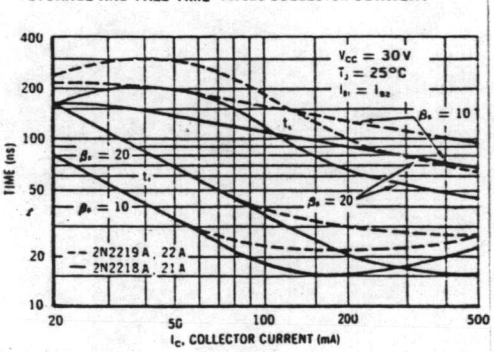




CURRENT-GAIN — BANDWIDTH PRODUCT and COLLECTOR BASE TIME CONSTANT versus COLLECTOR CURRENT



STORAGE AND FALL TIME versus COLLECTOR CURRENT



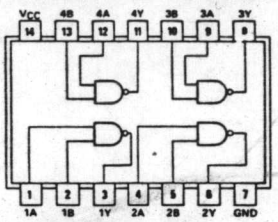
54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

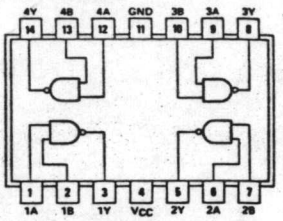
00
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

positive logic:
$Y = \overline{AB}$

See page 86



SN5400/SN7400(J, N)
SN54H00/SN74H00(J, N)
SN54L00/SN74L00(J, N)
SN54LS00/SN74LS00(J, N, W)
SN54S00/SN74S00(J, N, W)

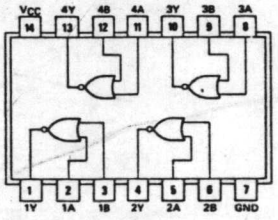


SN5400/SN7400(W)
SN54H00/SN74H00(W)
SN54L00/SN74L00(T)

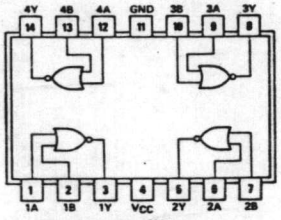
02
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

positive logic:
$Y = \overline{A+B}$

See page 92



SN5402/SN7402(J, N)
SN54L02/SN74L02(J, N)
SN54LS02/SN74LS02(J, N, W)
SN54S02/SN74S02(J, N, W)

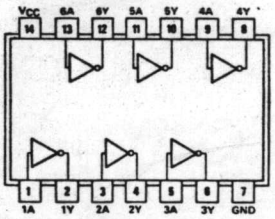


SN5402/SN7402(W)
SN54L02/SN74L02(T)

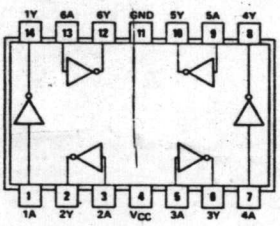
04
HEX INVERTERS

positive logic:
$Y = \overline{A}$

See page 86



SN5404/SN7404(J, N)
SN54H04/SN74H04(J, N)
SN54L04/SN74L04(J, N)
SN54LS04/SN74LS04(J, N, W)
SN54S04/SN74S04(J, N, W)

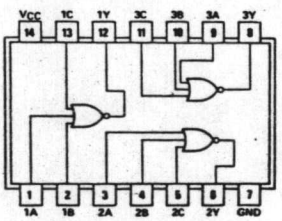


SN5404/SN7404(W)
SN54H04/SN74H04(W)
SN54L04/SN74L04(T)

27
TRIPLE 3-INPUT POSITIVE-NOR GATES

positive logic:
$Y = \overline{A+B+C}$

See page 92



SN5427/SN7427(J, N, W)
SN54LS27/SN74LS27(J, N, W)

PIN ASSIGNMENTS (TOP VIEWS)

QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

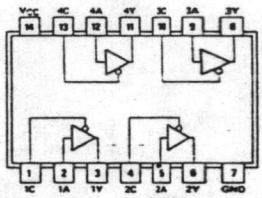
125

positive logic:

Y = A

Output is off (disabled) when C is high.

See page 6-33



SN54125 (J, W) SN74125 (J, N)
SN54LS125 (J, W) SN74LS125 (J, N)

DUAL J-K FLIP-FLOPS WITH CLEAR

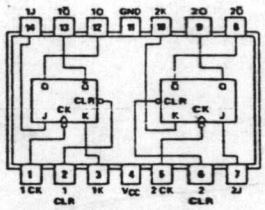
73

'73, 'H73, 'L73
FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⊓	L	L	Q_0	$\bar{Q}_0$
H	⊓	H	L	H	L
H	⊓	L	H	L	H
H	⊓	H	H	TOGGLE	

'LS73
FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$



SN5473 (J, W) SN7473 (J, N)
SN54H73 (J, W) SN74H73 (J, N)
SN54L73 (J, T) SN74L73 (J, N)
SN54LS73 (J, W) SN74LS73 (J, N)

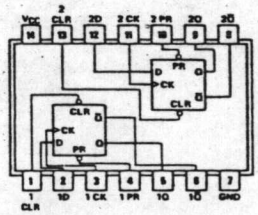
See pages 6-46, 6-50, 6-54, and 6-56

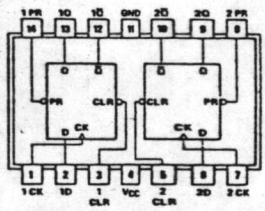
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

74

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$





SN5474 (J) SN7474 (J, N) SN5474 (W)
SN54H74 (J) SN74H74 (J, N) SN54H74 (W)
SN54L74 (J) SN74L74 (J, N) SN54L74 (T)
SN54LS74A (J, W) SN74LS74A (J, N)
SN54S74 (J, W) SN74S74 (J, N)

See pages 6-46, 6-50, 6-54, and 6-56

TTL MSI

TYPES SN5490A, SN5492A, SN5493A, SN54L90, SN54L93, SN54LS90, SN54LS92, SN54LS93, SN7490A, SN7492A, SN7493A, SN74L90, SN74L93, SN74LS90, SN74LS92, SN74LS93 DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

BULLETIN NO. DL-S 7611807, MARCH 1974—REVISED OCTOBER 1976

'90A, 'L90, 'LS90 . . . DECADE COUNTERS

'92A, 'LS92 . . . DIVIDE-BY-TWELVE COUNTERS

'93A, 'L93, 'LS93 . . . 4-BIT BINARY COUNTERS

TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'L90	20 mW
'LS90	45 mW
'92A, '93A	130 mW
'LS92, 'LS93	45 mW
'L93	16 mW

description

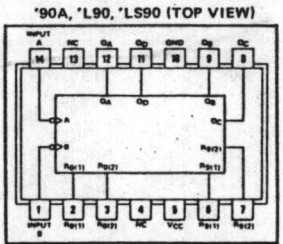
Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A, 'L90, and 'LS90, divide-by-six for the '92A and 'LS92, and divide-by-eight for the '93A, 'L93, and 'LS93.

All of these counters have a gated zero reset and the '90A, 'L90, and 'LS90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A, 'L90, or 'LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

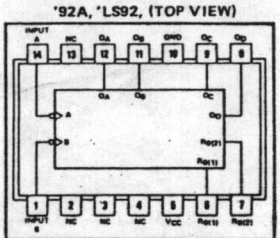
SN54', SN54LS' . . . J OR W PACKAGE
SN54L' . . . J OR T PACKAGE
SN54', SN74L', SN74LS' . . . J OR N PACKAGE

'90A, 'L90, 'LS90 (TOP VIEW)



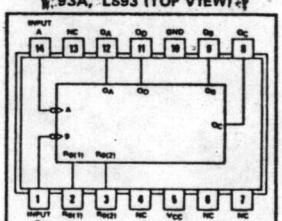
positive logic: see function tables

'92A, 'LS92, (TOP VIEW)



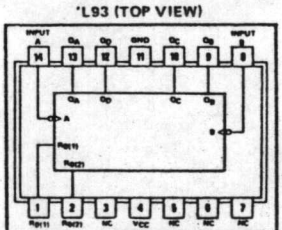
positive logic: see function tables

'93A, 'LS93 (TOP VIEW)



positive logic: see function tables

'L93 (TOP VIEW)



positive logic: see function tables

NC—No internal connection

TYPES SN5490A, '92A, '93A, SN54L90, 'L93, SN54LS90, 'LS92, 'LS93, SN7490A, '92A, '93A, SN74L90, 'L93, SN74LS90, 'LS92, 'LS93 DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

'90A, 'L90, 'LS90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'L90, 'LS90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'92A, 'LS92
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

'93A, 'L93, 'LS93
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

'90A, 'L90, 'LS90
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

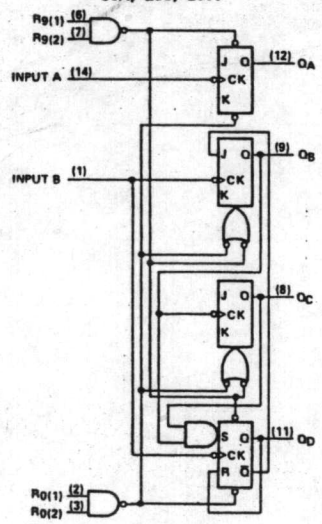
'92A, 'LS92, '93A, 'L93, 'LS93
RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

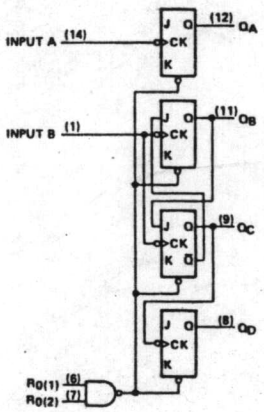
NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

functional block diagrams

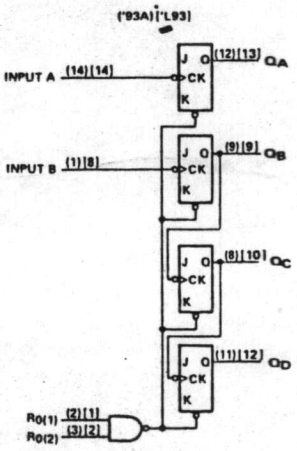
'90A, 'L90, 'LS90



'92A, 'LS92



'93A, 'L93, 'LS93



The J and K inputs shown without connection are for reference only and are functionally at a high level.

TTL MSI

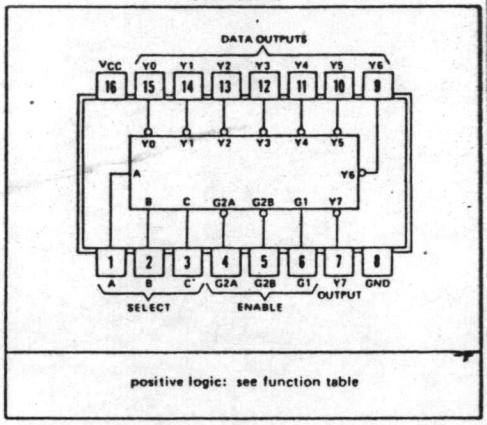
TYPES SN54LS138, SN54LS139, SN54S138, SN54S139, SN74LS138, SN74LS139, SN74S138, SN74S139 DECODERS/DEMULTIPLEXERS

BULLETIN NO. DL-S 7611804, DECEMBER 1972–REVISED OCTOBER 1976

- Designed Specifically for High-Speed:
  Memory Decoders
  Data Transmission Systems
- 'S138 and 'LS138 3-to-8-Line Decoders Incorporate 3 Enable Inputs to Simplify Cascading and/or Data Reception
- 'S139 and 'LS139 Contain Two Fully Independent 2-to-4-Line Decoders/ Demultiplexers
- Schottky Clamped for High Performance

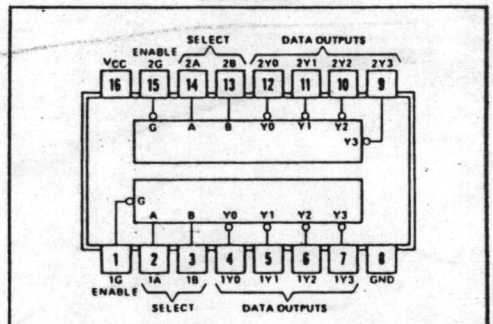
TYPE	TYPICAL PROPAGATION DELAY (3 LEVELS OF LOGIC)	TYPICAL POWER DISSIPATION
'LS138	22 ns	32 mW
'S138	8 ns	245 mW
'LS139	22 ns	34 mW
'S139	7.5 ns	300 mW

SN54LS138, SN54S138 . . . J OR W PACKAGE
SN74LS138, SN74S138 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

SN54LS139, SN54S139 . . . J OR W PACKAGE
SN74LS139, SN74S139 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

The 'LS138 and 'S138 decode one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

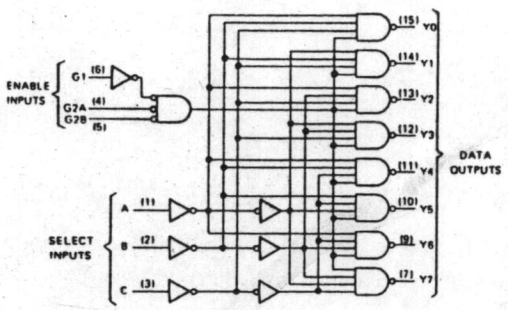
The 'LS139 and 'S139 comprise two individual two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs each of which represents only one normalized Series 54LS/74LS load ('LS138, 'LS139) or one normalized Series 54S/74S load ('S138, 'S139) to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design. Series 54LS and 54S devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74LS and 74S devices are characterized for 0°C to 70°C industrial systems.

TYPES SN54LS138, SN54S138, SN54LS139, SN54S139
SN74LS138, SN74S138, SN74LS139, SN74S139
DECODERS/DEMULTIPLEXERS

functional block diagrams and logic

'LS138, 'S138



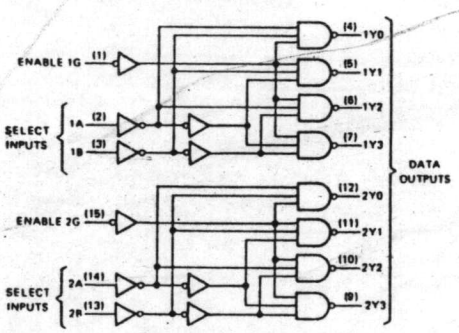
'LS138, 'S138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B

H = high level, L = low level, X = irrelevant

'LS139, 'S139



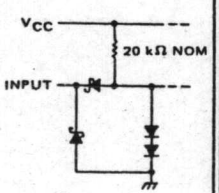
'LS139, 'S139
(EACH DECODER/DEMULTIPLEXER)
FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

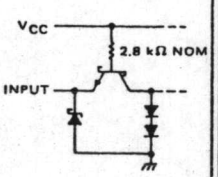
H = high level, L = low level, X = irrelevant

schematics of inputs and outputs

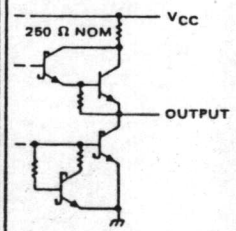
EQUIVALENT OF EACH INPUT OF 'LS138, 'LS139



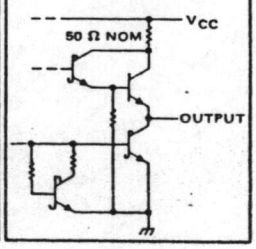
EQUIVALENT OF EACH INPUT OF 'S138, 'S139



TYPICAL OF OUTPUTS OF 'LS138, 'LS139



TYPICAL OF OUTPUTS OF 'S138, 'S139



Am8212

Eight-Bit Input/Output Port

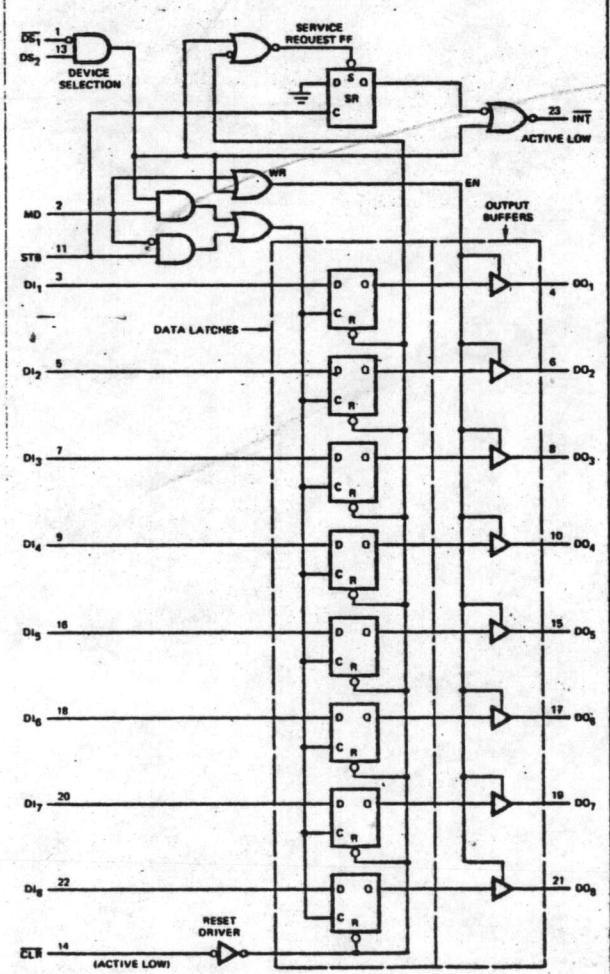
Distinctive Characteristics

- Fully parallel, 8-bit data register and buffer replacing latches, multiplexers and buffers needed in microprocessor systems.
- 4.0V output high voltage for direct interface to MOS microprocessors, such as the Am9080A family.
- Input load current 250μA max.
- Reduces system package count
- Available for operation over both commercial and military temperature ranges.
- Advanced Schottky processing with 100% reliability assurance testing in compliance with MIL-STD-883.
- Service request flip-flop for interrupt generation
- Three-state outputs sink 15mA
- Asynchronous register clear with clock over-ride

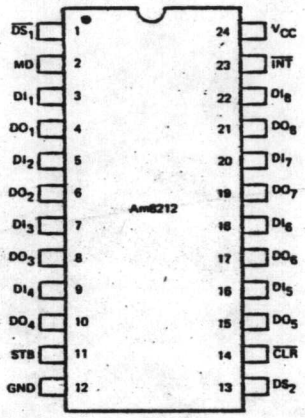
FUNCTIONAL DESCRIPTION

All of the principal peripheral and input/output functions of a Microcomputer System can be implemented with the Am8212. The Am8212 input/output port consists of an 8-bit latch with 3-state output buffers along with control and device selection logic, which can be used to implement latches, gated buffers or multiplexers.

LOGIC DIAGRAM



CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

PIN DEFINITION

$DI_1 - DI_8$	DATA IN
$DO_1 - DO_8$	DATA OUT
$\overline{DS_1} - DS_2$	DEVICE SELECT
MD	MODE
STB	STROBE
$\overline{INT}$	INTERRUPT (ACTIVE LOW)
$\overline{CLR}$	CLEAR (ACTIVE LOW)

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	–55°C to +125°C	AM8212DM
Hermetic DIP	0°C to +70°C	C8212
Molded DIP	0°C to +70°C	P8212
Dice	0°C to +70°C	AM8212XC
Hermetic DIP	0°C to +70°C	C3212
Molded DIP	0°C to +70°C	P3212

National Semiconductor

MOS EPROMs

MM2708, MM2704 8k and 4k UV Erasable PROM

General Description

The MM2708, MM2704 are high speed 8192/4096-bit UV erasable and electrically reprogrammable EPROMs ideally suited for applications where fast turn-around and pattern experimentation are important requirements.

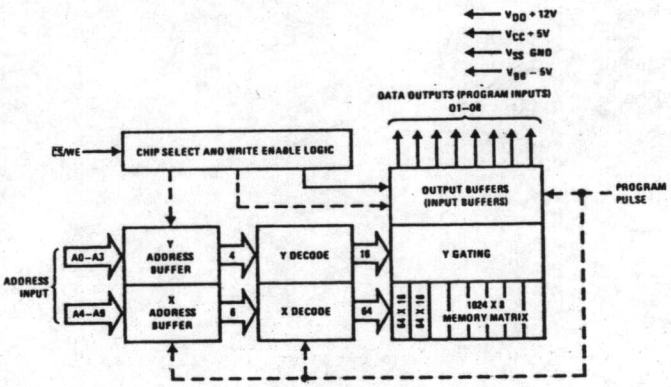
The MM2708, MM2704 are packaged in a 24-pin dual-in-line package with transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the devices by following the programming procedure.

The MM2708, MM2704 is fabricated with the reliable, high volume, time proven, N-channel silicon gate technology.

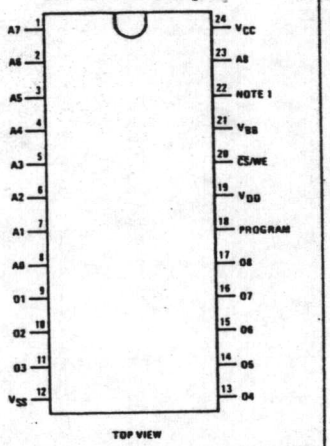
Features

- 1024 x 8 organization (MM2708)
- 512 x 8 organization (MM2704)
- 800 mW max
- Low power during programming
- Access time—450 ns max
- Standard power supplies: 12V, 5V, −5V
- Static—no clocks required
- Inputs and outputs TTL compatible during both read and program modes
- TRI-STATE® output

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM2708Q or MM2704Q
See Package 21

Order Number MM2708JQ or MM2704JQ
See Package 10C

Note. MM2704: Pin 22 = V_{SS}
MM2708: Pin 22 = A9

Pin Connection During Read or Program

MODE	PIN NUMBER						
	9–11, 13–17	12	18	19	20	21	24
Read	D_{OUT}	V_{SS}	V_{SS}	V_{DD}	V_{IL}	V_{BB}	V_{CC}
Program	D_{IN}	V_{SS}	Pulsed V_{IHP}	V_{DD}	V_{IHW}	V_{BB}	V_{CC}

Pin Description

A0–A9	Address inputs
O1–O8	Data outputs
$\overline{CS}$/WE	Chip select/write enable input

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−25°C to +85°C
Storage Temperature	−65°C to +125°C
V_{DD} with Respect to V_{BB}	20V to −0.3V
V_{CC} and V_{SS} with Respect to V_{BB}	15V to −0.3V
All Input or Output Voltages with Respect to V_{BB} During Read	15V to −0.3V
$\overline{CS}$/WE Input with Respect to V_{BB} During Programming	20V to −0.3V
Program Input with Respect to V_{BB}	35V to −0.3V
Power Dissipation	1.5 W
Lead Temperature (Soldering, 10 seconds)	300°C

Read Operation

DC Operating Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5%, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V, unless otherwise noted, (Note 3)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Address and Chip Select Input Sink Current	V_{IN} = 5.25V or V_{IN} = V_{IL}		1	10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.25V, $\overline{CS}$/WE = 5V		1	10	μA
I_{DD}	V_{DD} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		44	65	mA
I_{CC}	V_{CC} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		7	10	mA
I_{BB}	V_{BB} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		34	45	mA
V_{IL}	Input Low Voltage		V_{SS}		0.65	V
V_{IH}	Input High Voltage		3.0		V_{CC}+1	V
V_{OH1}	Output High Voltage	I_{OH} = −100 μA	3.7			V
V_{OH2}	Output High Voltage	I_{OH} = −1 mA	2.4			V
V_{OL}	Output Low Votlage	I_{OL} = 1.6 mA			0.45	V
P_D	Power Dissipation				800	mW

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±5%, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V, unless otherwise noted

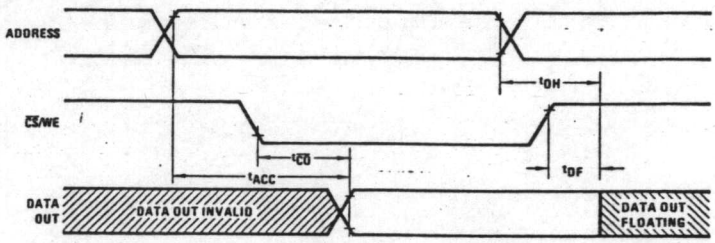
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{ACC}	Address to Output Delay	Output Load: 1 TTL Gate and C_L = 100 pF, Input Rise and Fall Times ≤ 20 ns: Timing Measurement Reference Levels: 0.8V and 2.8V for Inputs; 0.8V and 2.4V for Outputs, Input Pulse Levels: 0.65V to 3V		280	450	ns
t_{CO}	Chip Select to Output Delay			60	120	ns
t_{DF}	Chip Deselect to Output Delay		0		120	ns
t_{OH}	Address to Output Hold		0			ns
CAPACITANCE, (Note 2)						
C_{IN}	Input Capacitance	V_{IN} = 0V, T_A = 25°C, f = 1 MHz		4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, T_A = 25°C, f = 1 MHz		8	12	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing. T_A = 25°C, f = 1 MHz

Note 3: Typical conditions are for operation at: T_A = 25°C, V_{CC} = 5V, V_{DD} = 12V, V_{BB} = −5V, and V_{SS} = 0V.

Switching Time Waveforms



Programming Instructions

Initially, and after each erasure, all bits of the MM2708, MM2704 are in the "1" state (output high). Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The circuit is set up for programming operation by raising the $\overline{CE}$/WE input (pin 20) to +12V. The word address is selected in the same manner as in the read mode. Data to be programmed are presented, 8 bits in parallel, to the data output lines (O1—O8). Logic levels for address and data lines and the supply voltages are the same as for the read mode. After address and data set up, one program pulse per address is applied to the program input (pin 18). One pass through all addresses is defined as a program loop. The number of loops (N) required is a function of the program pulse width (t_{PW}) according to N x $t_{PW} \geq 100$ ms.

The width of the program pulse is from 0.1 to 1 ms. The number of loops (N) is from a minimum of 100 (t_{PW} = 1 ms) to greater than 1000 (t_{PW} = 0.1 ms). There must be N successive loops through all 1024 addresses. *It is not permitted to apply N program pulses to an address and then change to the next address to be programmed.* Caution should be observed regarding the end of a program sequence. The $\overline{CS}$/WE falling edge transition must occur before the first address transition when changing from a program to a read cycle. The program pin should also be pulled down to V_{ILP} with an active instead of a passive device. This pin will source a small amount of current (I_{IPL}) when $\overline{CS}$/WE is at V_{IHW} (12V) and the program pulse is at V_{ILP}.

Programming Characteristics

T_A = 25°C, V_{CC} = 5V ±5%, V_{DD} = 12V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V, unless otherwise noted

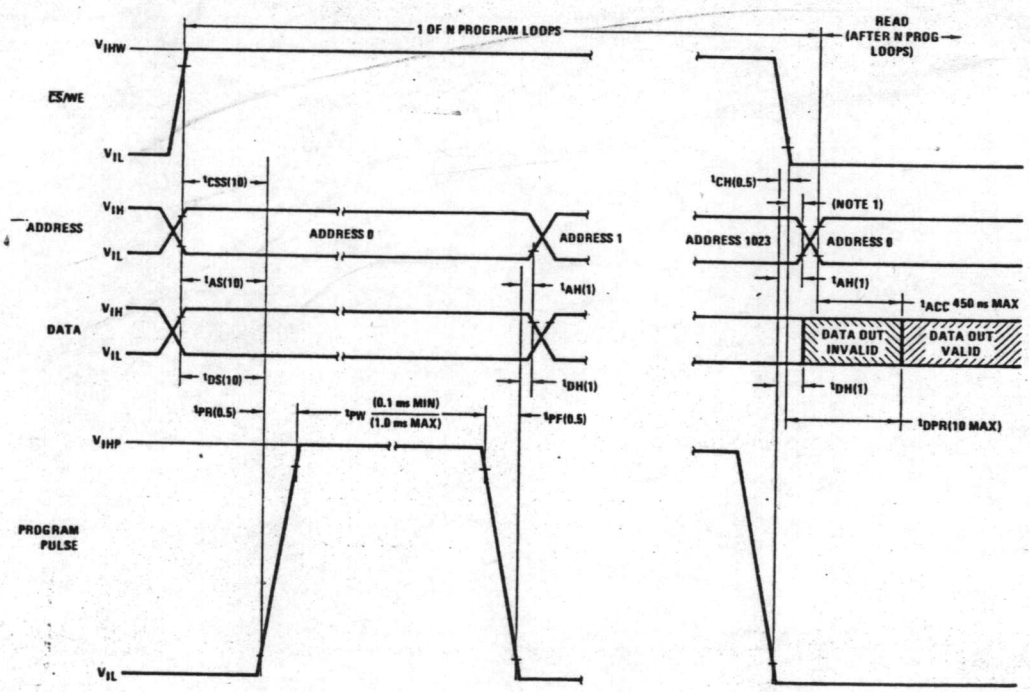
DC Programming Characteristics

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{LI}	Address and $\overline{CS}$/WE Input Sink Current	V_{IN} = 5.25V			10	μA
I_{IPL}	Program Pulse Source Current				3	mA
I_{IPH}	Program Pulse Sink Current				20	mA
I_{DD}	V_{DD} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		44	65	mA
I_{CC}	V_{CC} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		7	10	mA
I_{BB}	V_{BB} Supply Current	Worst-Case Supply Currents, All Inputs High, $\overline{CS}$/WE = 5V, T_A = 0°C		34	45	mA
V_{IL}	Input Low Level (Except Program)		V_{SS}		0.65	V
V_{IH}	Input High Level, All Addresses and Data		3.0		V_{CC}+1	V
V_{IHW}	$\overline{CS}$/WE Input High Level	Referenced to V_{SS}	11.4		12.6	V
V_{IHP}	Program Pulse High Level	Referenced to V_{SS}	25		27	V
V_{ILP}	Program Pulse Low Level	$V_{IHP} - V_{ILP}$ = 25V Min	V_{SS}		1	V

AC Programming Characteristics

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{AS}	Address Set-Up Time		10			μs
t_{CSS}	$\overline{CS}$/WE Set-Up Time		10			μs
t_{DS}	Data Set-Up Time		10			μs
t_{AH}	Address Hold Time		1			μs
t_{CH}	$\overline{CS}$/WE Hold Time		0.5			μs
t_{DH}	Data Hold Time		1			μs
t_{DF}	Chip Deselect to Output Float Delay		0		120	μs
t_{DPR}	Program to Read Delay				10	μs
t_{PW}	Program Pulse Width		0.1		1.0	ms
t_{PR}	Program Pulse Rise Time		0.5		2.0	μs
t_{PF}	Program Pulse Fall Time		0.5		2.0	μs

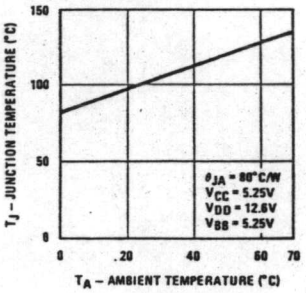
Programming Waveforms



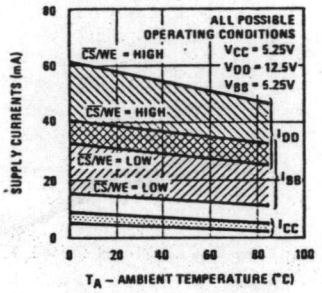
Note 1: The $\overline{CS}$/WE transition must occur after the program pulse transition and before the address transition.
Note 2: Numbers in parentheses indicate minimum timing in microseconds unless otherwise specified.

Typical DC Performance Characteristics

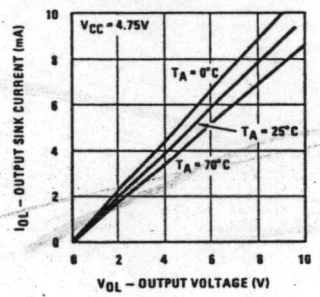
Maximum Junction Temperature vs Ambient Temperature



Range of Supply Currents vs Temperature

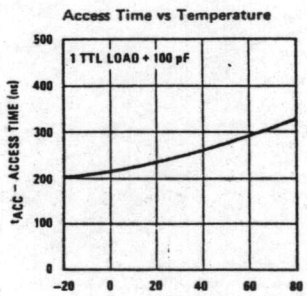


Output Sink Current vs Output Voltage

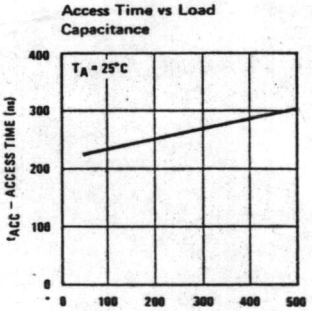


Typical AC Performance Characteristics

Access Time vs Temperature



Access Time vs Load Capacitance



Voltage Regulators

LM340 series voltage regulators

general description

The LM340-XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

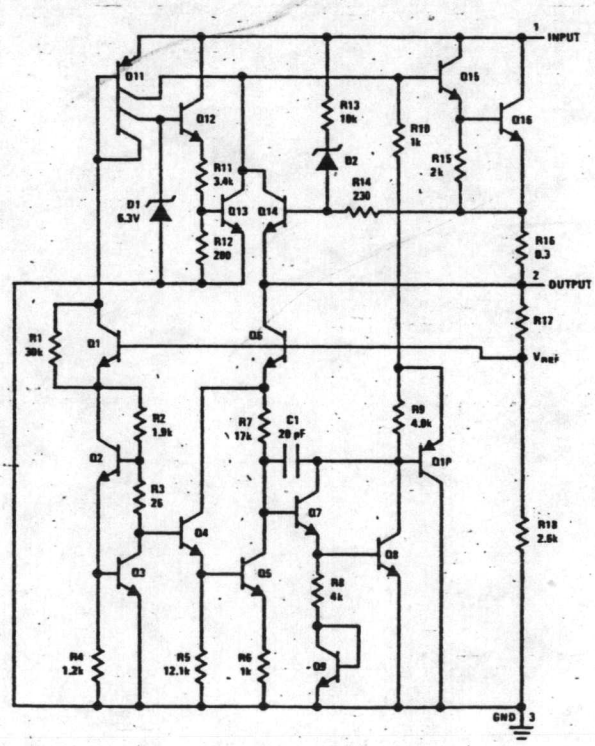
The LM340-XX series is available in two power packages. Both the plastic TO-220 and metal TO-3 packages allow these regulators to deliver over 1.5A if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe-area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expended to make the LM340-XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

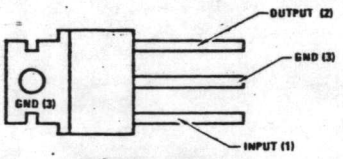
features

- Output current in excess of 1.5A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-220 and metal TO-3 packages

schematic and connection diagrams



Plastic Package



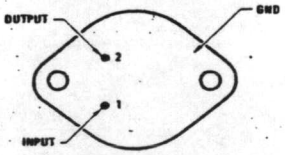
TOP VIEW

Order Numbers

LM340T-5.0	LM340T-12
LM340T-6.0	LM340T-15
LM340T-8.0	LM340T-18
LM340T-10	LM340T-24

See Package 26

Metal Can Package
(K) (Steel)
(KC) (Aluminum)



BOTTOM VIEW

Order Numbers

LM340K-5	LM340KC-5.0
LM340K-6	LM340KC-6.0
LM340K-8	LM340KC-8.0
LM340K-10	LM340KC-10
LM340K-12	LM340KC-12
LM340K-15	LM340KC-15
LM340K-18	LM340KC-18
LM340K-24	LM340KC-24

See Package 18

absolute maximum ratings

Input Voltage (V_O = 5V through 18V)	35V
(V_O = 24V)	40V
Internal Power Dissipation (Note 1)	Internally Limited
Operating Temperature Range	0°C to 70°C
Maximum Junction Temperature	
TO-3 Package	150°C
TO-220 Package	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
TO-3 Package (Soldering, 10 sec)	300°C
TO-220 Package (Soldering, 10 sec)	230°C

electrical characteristics

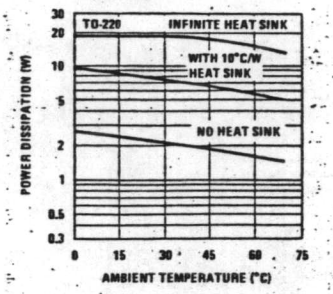
T_A = 0°c to 70°C, I_O = 500 mA, unless otherwise noted.

OUTPUT VOLTAGE			5V			6V			8V			10V			12V			15V			18V			24V			UNITS
INPUT VOLTAGE (unless otherwise noted)			10V			11V			14V			17V			19V			23V			27V			33V			
PARAMETER		CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_O	Output Voltage	T_J = 25°C	4.8	5	5.2	5.75	6	6.25	7.7	8	8.3	9.6	10	10.4	11.5	12	12.5	14.4	15	15.6	17.3	18	18.7	23	24	25	V
		$P_D \leq$ 15W, 5 mA $\leq I_O \leq$ 1000 mA and $V_{MIN} \leq V_{IN} \leq V_{MAX}$	4.75		5.25	5.7		6.3	7.6		8.4	9.5		10.5	11.4		12.6	14.25		15.75	17.1		18.9	22.8		25.2	V
			(7 ≤ V_{IN} ≤ 20)			(8 ≤ V_{IN} ≤ 21)			(10.5 ≤ V_{IN} ≤ 23)			(12.5 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 27)			(17.5 ≤ V_{IN} ≤ 30)			(21 ≤ V_{IN} ≤ 33)			(27 ≤ V_{IN} ≤ 38)			V
ΔV_O	Line Regulation	T_J = 25°C, I_O = 100 mA		50			60			80			100			120			150			180			240	mV
		T_J = 25°C, I_O = 500 mA		100			120			160			200			240			300			360			480	mV
			(7 ≤ V_{IN} ≤ 25)			(8 ≤ V_{IN} ≤ 25)			(10.5 ≤ V_{IN} ≤ 25)			(12.5 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			(21 ≤ V_{IN} ≤ 33)			(27 ≤ V_{IN} ≤ 38)			V
ΔV_O	Load Regulation	T_J = 25°C		100			120			160			200			240			300			360			480	mV
			(5 ≤ I_O ≤ 1500)			(5 ≤ I_O ≤ 1500)			(5 ≤ I_O ≤ 1500)			(5 ≤ I_O ≤ 1500)			(5 ≤ I_O ≤ 1500)			(5 ≤ I_O ≤ 1500)			(5 ≤ I_O ≤ 1000)			(5 ≤ I_O ≤ 1000)			mA
ΔV_O	Long Term Stability			20			24			32			40			48			60			72			96		mV/1000 hrs
I_Q	Quiescent Current	T_J = 25°C		7	10		7	10		7	10		7	10		7	10		7	10		7	10		7	10	mA
ΔI_Q	Quiescent Current Change	$I_{MIN} \leq I_O \leq I_{MAX}$		0.5			0.5			0.5			0.5			0.5			0.5			0.5			0.5		mA
			(5 ≤ I_O ≤ 1500)			(5 ≤ I_O ≤ 1500)			(5 ≤ I_O ≤ 1500)			(5 ≤ I_O ≤ 1500)			(5 ≤ I_O ≤ 1500)			(5 ≤ I_O ≤ 1500)			(5 ≤ I_O ≤ 1000)			(5 ≤ I_O ≤ 1000)			mA
		$V_{MIN} \leq V_O \leq V_{MAX}$		1.3			1.3			1.0			1.0			1.0			1.0			1.0			1.0		mA
			(7 ≤ V_{IN} ≤ 25)			(8 ≤ V_{IN} ≤ 25)			(10.5 ≤ V_{IN} ≤ 25)			(12.5 ≤ V_{IN} ≤ 25)			(14.5 ≤ V_{IN} ≤ 30)			(17.5 ≤ V_{IN} ≤ 30)			(21 ≤ V_{IN} ≤ 33)			(27 ≤ V_{IN} ≤ 38)			V
V_n	Output Noise Voltage	T_J = 25°C, f = 10 Hz – 100 kHz		40			45			52			70			75			90			110			170		μV
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	Ripple Rejection	f = 120 Hz		60			57			55			54			52			50			48			44		dB
	Input Voltage Required to Maintain Line Regulation	T_J = 25°C		7			8			10.5			12.5			14.5			17.5			21			27		V

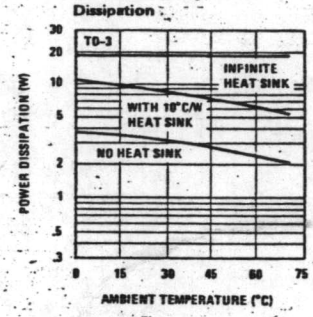
Note 1: Thermal resistance without a heat sink for junction to case temperature is 4°C/W for the TO-3 package and 4°C/W for the TO-220 package. Thermal resistance for case to ambient temperature is 35°C/W for the TO-3 package and 50°C/W for the TO-220 package.

typical performance characteristics

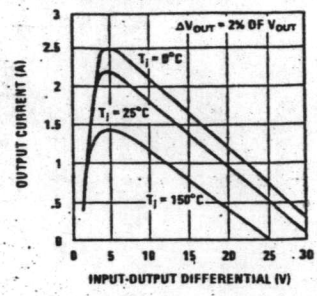
Maximum Average Power Dissipation



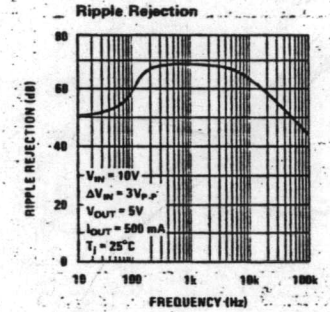
Maximum Average Power Dissipation



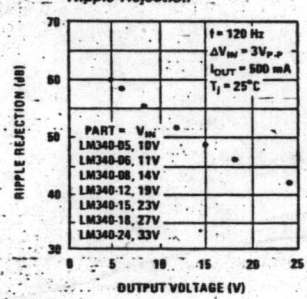
Peak Output Current



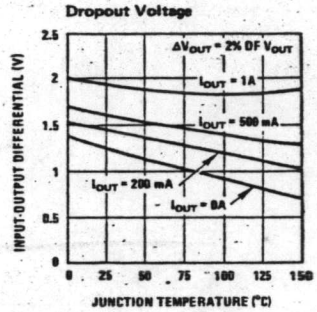
Ripple Rejection



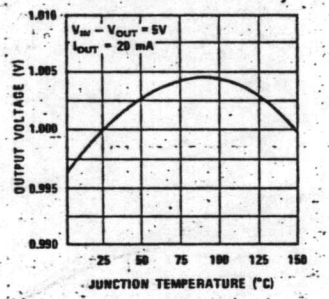
Ripple Rejection



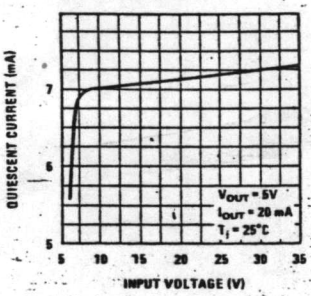
Dropout Voltage



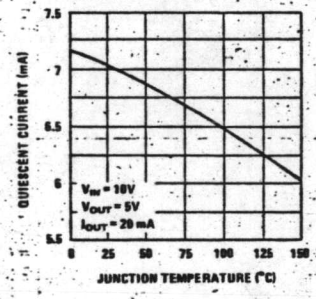
Output Voltage (Normalized to 1V at 25°C T_J)



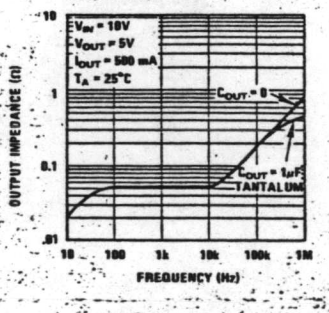
Quiescent Current



Quiescent Current



Output Impedance



Am555

Precision Timer

Distinctive Characteristics

- Timing from microseconds through hours
- 200mA output sink current
- Variable duty cycle
- TTL output compatibility
- Temperature stability of 0.005%/°C
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am555 is a highly stable timing device used to provide accurate time delays or to build precision oscillators. When the device is used as a monostable, the time is precisely controlled using one external resistor and one external capacitor. When the device is used as a precision oscillator, the frequency and duty cycle are controlled by two external resistors and one external capacitor.

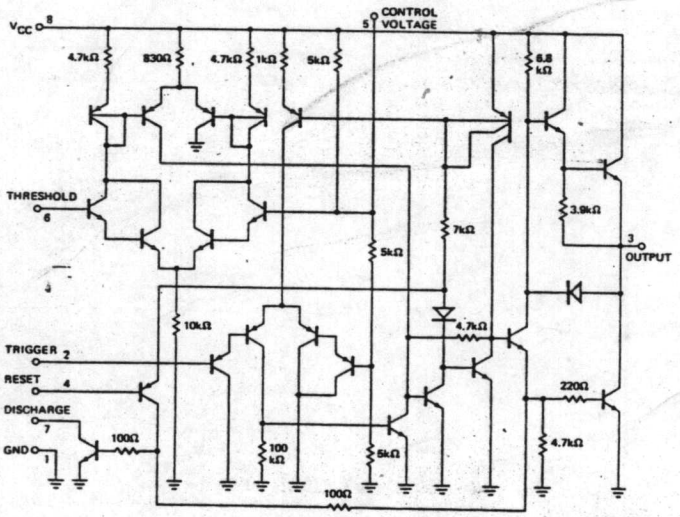
For monostable operation, a HIGH-to-LOW transition is applied to the trigger input. The device is triggered when the input trigger voltage reaches 1/3 V_{CC}.

Once the circuit is triggered, it will remain in the triggered state until the set time has elapsed, even if it is triggered again. The output pulse width is equal to 1.1 $R_A C$.

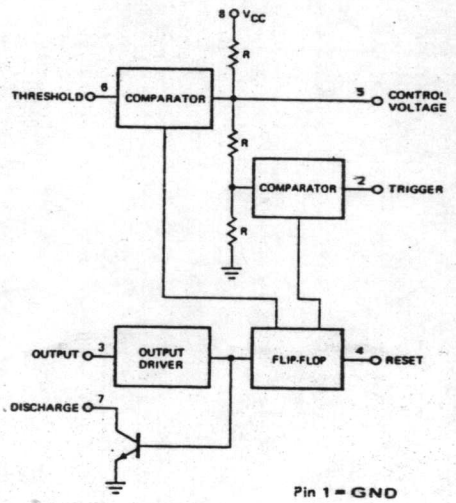
For continuous oscillation, two external resistors are used such that the external capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. The charge time is given by $t_{charge} = 0.693 (R_A + R_B)C$ while the discharge time is $t_{discharge} = 0.693 R_B C$.

The device also features a direct reset that overrides all other inputs. When the reset is LOW the output is LOW regardless of the other inputs.

SCHEMATIC DIAGRAM



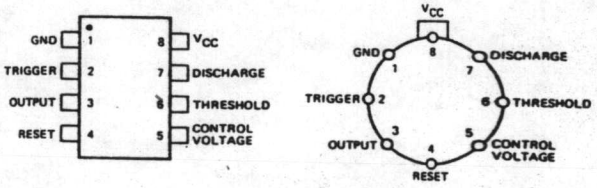
LOGIC SYMBOL



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Mini-DIP	0°C to +70°C	NE555V
TO-5	0°C to +70°C	NE555T
Dice	0°C to +70°C	AM555XC
TO-5	–55°C to +125°C	SE555T
Dice	–55°C to +125°C	AM555XM

CONNECTION DIAGRAMS



Note: Pin 1 is marked for orientation.

MAXIMUM RATING (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	
Military Grade	−55°C to +125°C
Commercial Grade	0°C to +70°C
Supply Voltage to Ground Potential	+18V
Power Dissipation	600mW
Lead Temperature (Soldering, 60 seconds)	+300°C

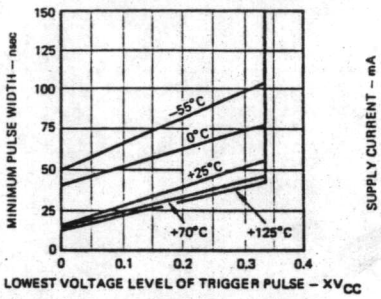
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = +5V to +15V Unless Otherwise Noted)

Parameter	Test Conditions		Military Min.	Military Typ.	Military Max.	Commercial Min.	Commercial Typ.	Commercial Max.	Units
Supply Voltage			4.5		18	4.5		16	V
Supply Current (LOW State)	V_{CC} = 5V, R_L = ∞			3	5		3	6	mA
	V_{CC} = 15V, R_L = ∞ (Note 1)			10	12		10	15	
Threshold Voltage				2/3			2/3		XV_{CC}
Trigger Voltage	V_{CC} = 15V		4.8	5	5.2		5		V
	V_{CC} = 5V		1.45	1.67	1.9		1.67		
Trigger Current				0.5			0.5		μA
Reset Voltage			0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current				0.1			0.1		mA
Threshold Current	(Note 3)			0.1	.25		0.1	.25	μA
Control Voltage Level	V_{CC} = 15V		9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5V		2.9	3.33	3.8	2.6	3.33	4	
Output Voltage (LOW)	V_{CC} = 15V	I_{SINK} = 10mA		0.1	0.15		0.1	.25	V
		I_{SINK} = 50mA		0.4	0.5		0.4	.75	
		I_{SINK} = 100mA		2.0	2.2		2.0	2.5	
		I_{SINK} = 200mA		2.5			2.5		
	V_{CC} = 5V	I_{SINK} = 8mA		0.1	0.25				V
		I_{SINK} = 5mA					.25	.35	
Output Voltage (HIGH)	V_{CC} = 15V	I_{SOURCE} = −200mA		12.5			12.5		V
	V_{CC} = 15V	I_{SOURCE} = −100mA	13.0	13.3		12.75	13.3		V
	V_{CC} = 5V		3.0	3.3		2.75	3.3		
Timing Error (Monostable)									
Initial Accuracy	R_A = 1kΩ to 100kΩ			0.5	2		1		%
Drift with Temp.	C = 0.1μF (Note 2)			30	100		50		ppm/°C
Drift with Sup. Volt.				0.05	0.2		0.1		%/Volt
Rise Time of Output				100			100		nsec.
Fall Time of Output				100			100		

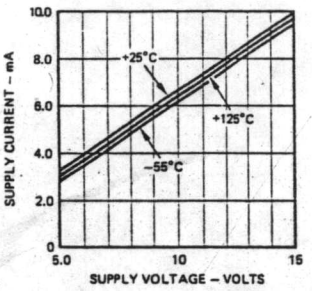
Notes: 1. Supply current when output HIGH typically 1mA less.
2. Tested at V_{CC} = 5V and V_{CC} = 15V
3. Determines the maximum value of $R_A + R_B$. For 15V operation, the max. total R = 20mΩ.

TYPICAL CHARACTERISTICS

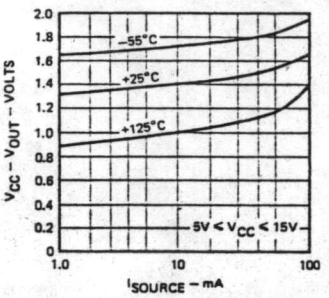
Minimum Pulse Width Required for Triggering



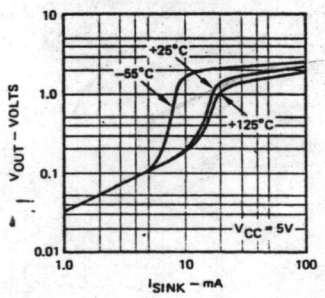
Supply Current Versus Supply Voltage



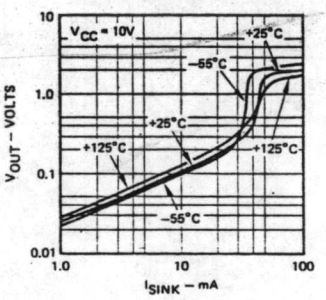
High Output Voltage Versus Output Source Current



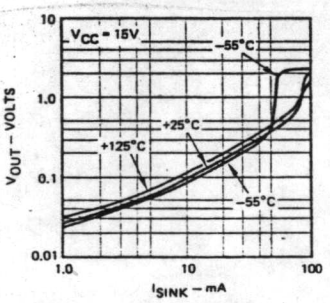
Low Output Voltage Versus Output Sink Current



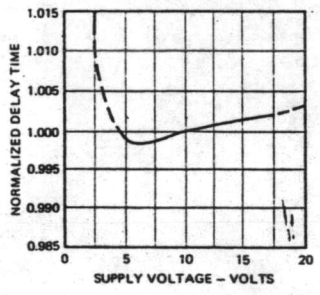
Low Output Voltage Versus Output Sink Current



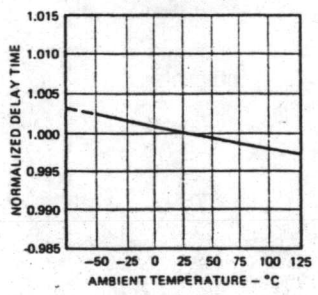
Low Output Voltage Versus Output Sink Current



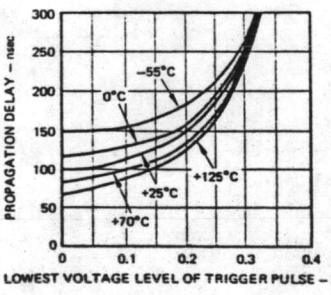
Delay Time Versus Supply Voltage



Delay Time Versus Temperature



Propagation Delay Versus Voltage Level of Trigger Pulse



APPLICATIONS

MONOSTABLE OPERATION

When the timer is operated as a monostable multivibrator, one external capacitor, C, and one external resistor, R_A, are used as shown in Figure 1. When the trigger input is reduced below 1/3 V_{CC}, the timer internal flip-flop is set. This releases the short circuit across the external capacitor and the Q output goes HIGH. The voltage across the capacitor begins to rise exponentially with the time constant R_AC. When the capacitor voltage reaches 2/3 V_{CC}, the internal comparator resets the flip-flop and the external capacitor, C, is rapidly discharged provided the trigger voltage is returned above 1/3 V_{CC}. The output is now in LOW state and a new timing cycle may be initiated. The time that the output is in the HIGH state is given by 1.1 R_AC or can be taken directly from Figure 2. Both the charge rate and internal threshold are directly proportional to the V_{CC} supply voltage. Thus, the timer output pulse width is independent of the power supply voltage. If a LOW is applied to the reset input, the output is forced LOW and the external capacitor discharged regardless of the other inputs.

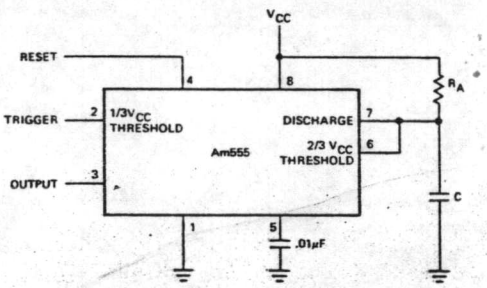


Fig. 1. Monostable Operation of the Am555.

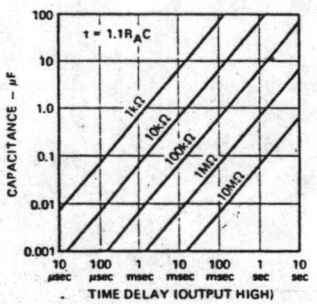


Fig. 2. Monostable Pulse Width.

ASTABLE OPERATION

When the timer is operated in the astable mode, two external resistors, R_A and R_B, and one external capacitor, C, are used as shown in Figure 3. With this connection scheme, the external capacitor, C, charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. The charge time (output HIGH) is

$$t_{AB} = 0.693\ (R_A + R_B)\ C$$

The discharge time (output LOW) is

$$t_B = 0.693\ R_BC$$

The total period for one cycle of output HIGH and output LOW is

$$T = t_{AB} + t_B = 0.693\ (R_A + 2R_B)\ C$$

The frequency for this period, T, is

$$f = \frac{1}{T} = \frac{1}{0.693\ (R_A + 2R_B)\ C}$$

The astable free running frequency can also be found from the graph shown in Figure 4. The duty cycle, time the output is LOW divided by the period, is given by

$$D = \frac{t_B}{t_{AB} + t_B} = \frac{R_B}{R_A + 2R_B}$$

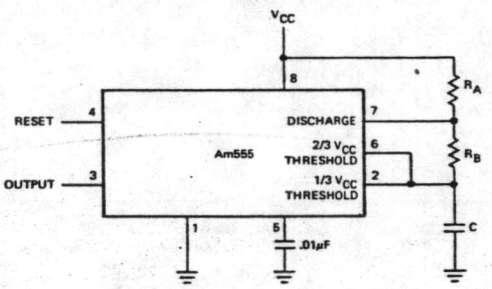


Fig. 3. Astable Operation of the Am555.

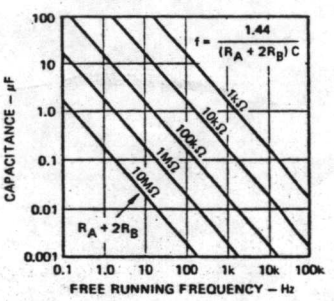
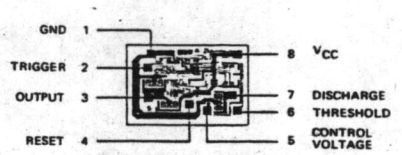


Fig. 4. Astable Free Running Frequency.

Metallization and Pad Layout



DIE SIZE: 0.040" X 0.060"

Monsanto

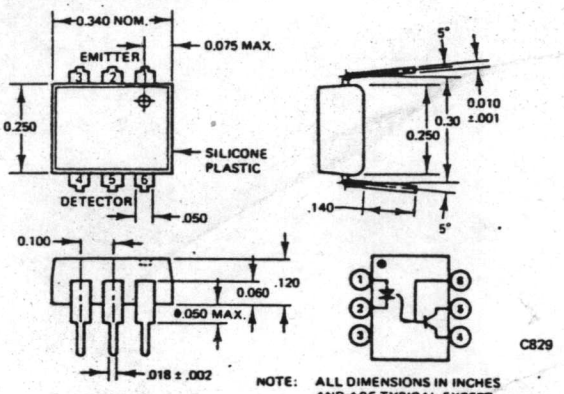
PHOTOTRANSISTOR OPTO-ISOLATOR

MCT26

PRODUCT DESCRIPTION

The MCT26 is a NPN silicon planar phototransistor optically coupled to a gallium arsenide diode. It is mounted in a six lead plastic DIP.

PACKAGE DIMENSIONS



NOTE: ALL DIMENSIONS IN INCHES AND ARE TYPICAL EXCEPT AS NOTED

APPLICATIONS

- AC line/digital logic isolator
- Digital logic/digital logic isolator
- Telephone/telegraph line receiver
- Twisted pair line receiver
- High frequency power supply feedback control
- Relay contact monitor
- Power supply monitor

ABSOLUTE MAXIMUM RATINGS

Storage Temperature −55°C to 150°C
Operating temperature −55°C to 100°C
Lead temperature (Soldering, 10 sec) 260°C

Input Diode
- Forward DC current . . . . . 60 mA
- Reverse current . . . . . 10 μA
- Peak forward current (1 μs pulse, 300 pps) . . . . . 3.0 A
- Power dissipation at 25°C ambient . . . . 200 mW
- Derate linearly from 25°C . . . . . 2.6 mW/°C

Output Transistor
- Power Dissipation at 25°C ambient . . . . 200 mW
- Derate linearly from 25°C . . . . . 2.6 mW/°C

Input to output voltage . . . . . 1500 volts

Total package power dissipation at 25°C ambient (LED plus detector) . . . . 250 mW

Derate linearly from 25°C . . . . . 3.3 mW/°C

ELECTRO-OPTICAL CHARACTERISTICS (25°C Free Air Temperature Unless Otherwise Specified)

CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Emitter					
Forward voltage V_F	—	1.25	1.5	V	I_F = 20 mA
Reverse current I_R	—	.15	10	μA	V_R = 3.0 V
Capacitance C_J	—	50	—	pF	V = 0
Detector					
h_{FE}	—	150	—		V_{CE} = 5 V, I_C = 100 μA
BV_{CEO}	30	85	—	V	I_C = 1.0 mA, I_F = 0
BV_{ECO}	7	12	—	V	I_C = 100 μA, I_F = 0
I_{CEO}	—	5	100	nA	V_{CE} = 5 V, I_F = 0
Capacitance Collector-emitter C_{CE}	—	8	—	pF	V_{CE} = 0
BV_{CBO}	30	165	—	V	I_C = 10 μA
I_{CBO} (dark)	—	1	100	nA	V_{CB} = 5 V, I_F = 0
Coupled					
DC current transfer ratio CTR	6	14	—	%	I_F = 10 mA, V_{CE} = 10 V, note 1
Breakdown voltage	1500	2500	—	VDC	
	800	—	—		VAC, RMS @ f = 60 Hz
Resistance emitter-detector R_{I-O}	10^{11}	10^{12}		Ω	V_{E-D} = 500 VDC
V_{CE} (SAT)	—	0.2	0.3	V	I_C = 250 μA, I_F = 20 mA
	—	0.2	0.5	V	I_C = 1.6 mA, I_F = 60 mA
Capacitance LED to detector C_{I-O}	—	0.5	—	pF	f = 1 MHz
Bandwidth (see figure 5) B_W	—	300	—	kHz	I_C = 2 mA, note 2
Rise time + fall time (see oper. schematics) t_r t_f		2	—	μs	I_C = 2 mA, V_{CE} = 10 V, note 3

MCT26

TYPICAL ELECTRO-OPTICAL CHARACTERISTIC CURVES
(25°C Free Air Temperature Unless Otherwise Specified)

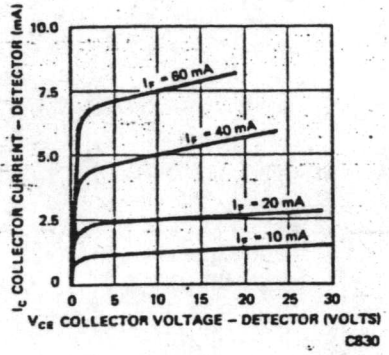


Fig. 1 Detector Output Characteristics

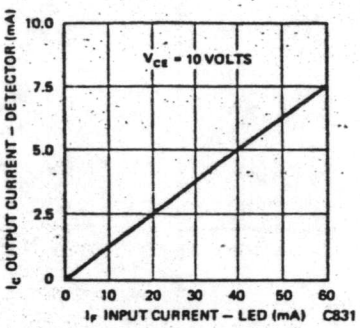


Fig. 2 Input Current vs. Output Current

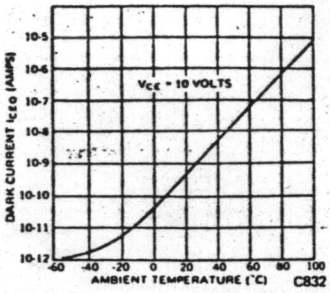


Fig. 3 Dark Current vs. Temperature (°C)

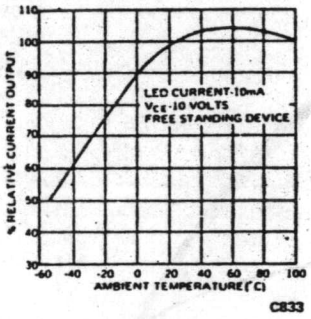


Fig. 4 Current Output vs. Temperature

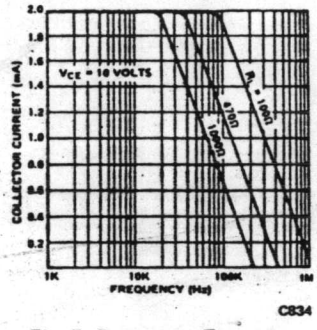


Fig. 5 Output vs. Frequency

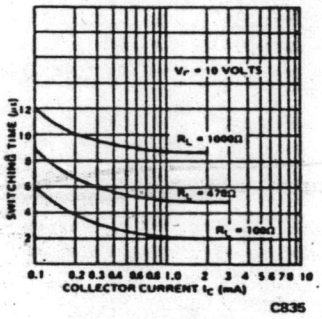


Fig. 6 Switching Time vs. Collector Current

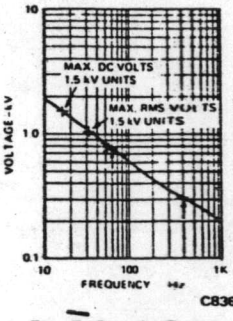
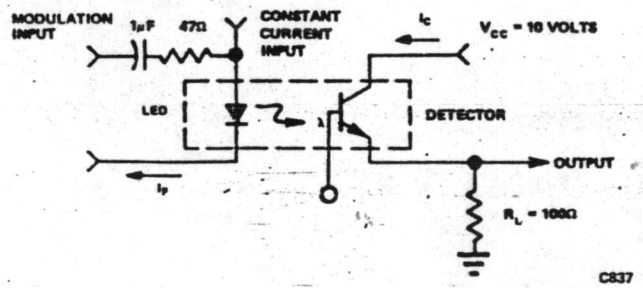


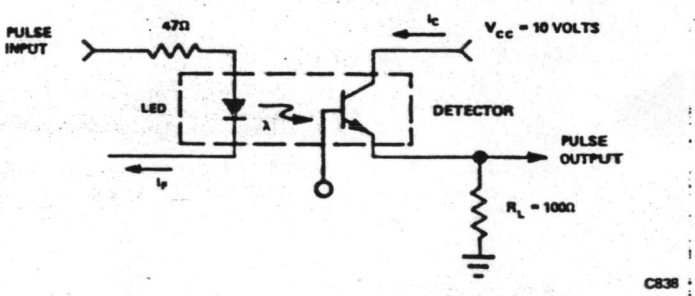
Fig. 7 Steady-State AC Voltage Limit of Isolation Dielectric

For additional characteristic curves, see figures 2, 3, 5, 6, 8, 11, 12, & 13 on MCT2.

OPERATING SCHEMATICS



Modulation Circuit Used to Obtain Output vs. Frequency Plot



Circuit Used to Obtain Switching Time vs. Collector Current Plot

NOTES

1. *The current transfer ratio (I_C/I_F) is the ratio of the detector collector current to the LED input current with V_{CE} at 10 volts.*
2. *The frequency at which i_c is 3 dB down from the 1 kHz value.*
3. *Rise time (t_r) is the time required for the collector current to increase from 10% of its final value to 90%. Fall time (t_f) is the time required for the collector current to decrease from 90% of its initial value to 10%.*

National Semiconductor

MM5309, MM5311, MM5312, MM5313, MM5314, MM5315 Digital Clocks

General Description

These digital clocks are monolithic MOS integrated circuits utilizing P-channel low-threshold, enhancement mode and ion implanted, depletion mode devices. The devices provide all the logic required to build several types of clocks. Two display modes (4 or 6-digits) facilitate end-product designs of varied sophistication. The circuits interface to LED and gas discharge displays with minimal additional components, and require only a single power supply. The timekeeping function operates from either a 50 or 60 Hz input, and the display format may be either 12 hours (with leading-zero blanking) or 24 hours. Outputs consist of multiplexed display drives ($\overline{BCD}$ and 7-segment) and digit enables. The devices operate over a power supply range of 11V to 19V and do not require a regulated supply. These clocks are packaged in dual-in-line packages.

Features

- 50 or 60 Hz operation
- 12 or 24-hour display format
- Leading-zero blanking (12-hour format)
- 7-segment outputs
- Single power supply
- Fast and slow set controls
- Internal multiplex oscillator
- For features of individual clocks, see Table I

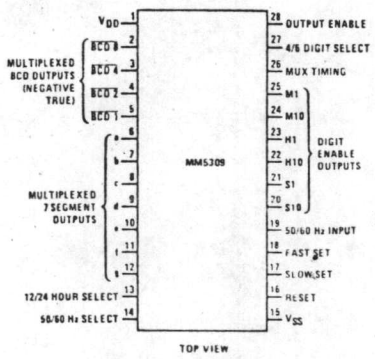
Applications

- Desk clocks
- Automobile clocks
- Industrial clocks
- Interval Timers

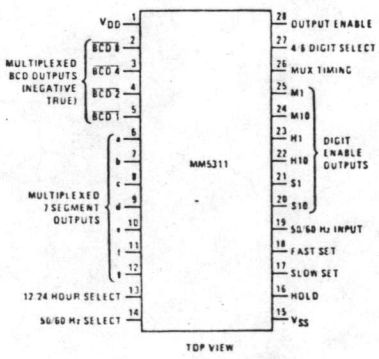
TABLE I

FEATURES	MM5309	MM5311	MM5312	MM5313	MM5314	MM5315
$\overline{BCD}$ Outputs	X	X	X	X		X
4/6-Digit Display Mode	X	X		X	X	X
Hold Count Control		X		X	X	X
1 Hz Output			X	X		
Output Enable Control	X	X			X	
Reset	X					X

Connection Diagrams (Dual-In-Line Packages)



Order Number MM5309M
See Package 23



Order Number MM5311N
See Package 23

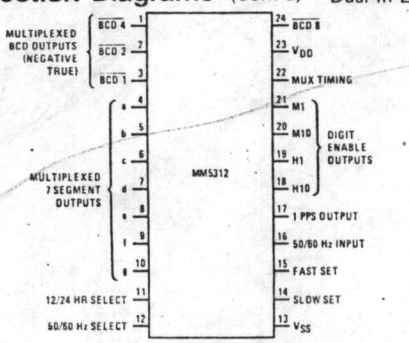
Absolute Maximum Ratings

Voltage at Any Pin	V_{SS} + 0.3 to V_{SS} −20V
Operating Temperature	−25°C to +70°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

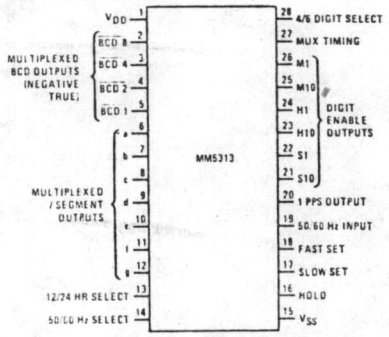
Electrical Characteristics T_A within operating range, V_{SS} = 11V to 19V, V_{DD} = 0V, unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{SS} (V_{DD} = 0V)	11		19	V
Power Supply Current	V_{SS} = 14V, (No Output Loads)			10	mA
50/60 Hz Input Frequency		dc	50 or 60	60k	Hz
50/60 Hz Input Voltage					
Logical High Level		V_{SS}−1	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{SS}−10	V
Multiplex Frequency	Determined by External R & C	0.100	1.0	60	kHz
All Logic Inputs	Driven by External Timebase	dc		60	kHz
Logical High Level	Internal Depletion Device to V_{SS}	V_{SS}−1	V_{SS}	V_{SS}	V
Logical Low Level		V_{DD}	V_{DD}	V_{SS}−10	V
$\overline{BCD}$ and 7-Segment Outputs					
Logical High Level	Loaded 2 kΩ to V_{DD}	2.0		20	mA source
Logical Low Level				0.01	mA source
Digital Enable Outputs					
Logical High Level				0.3	mA source
Logical Low Level	Loaded 100 Ω to V_{SS}	5.0		25	mA sink

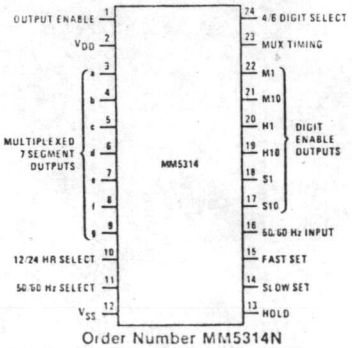
Connection Diagrams (Cont'd) Dual-In-Line Packages (Top Views)



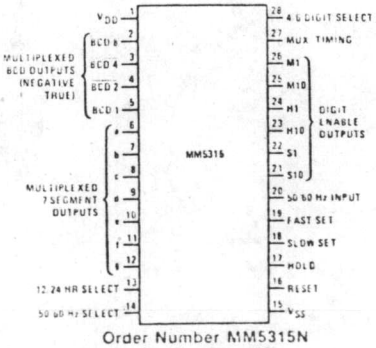
Order Number MM5312N
See Package 22



Order Number MM5313N
See Package 23



Order Number MM5314N
See Package 22



Order Number MM5315N
See Package 23

Functional Description

A block diagram of the MM5309 digital clock is shown in *Figure 1*. MM5311, MM5312, MM5313, MM5314 and MM5315 clocks are bonding options of MM5309 clock. Table I shows the pin-outs for these clocks.

50 or 60 Hz Input: This input is applied to a Schmitt Trigger shaping circuit which provides approximately 5V of hysteresis and allows using a filtered sinewave input. A simple RC filter such as shown in *Figure 10* should be used to remove possible line voltage transients that could either cause the clock to gain time or damage the device. The shaper output drives a counter chain which performs the timekeeping function.

50 or 60 Hz Select Input: This input programs the prescale counter to divide by either 50 or 60 to obtain a 1 Hz timebase. The counter is programmed for 60 Hz operation by connecting this input to V_{DD}. An internal depletion device is common to this pin; simply leaving this input unconnected programs the clock for 50 Hz operation. As shown in *Figure 1*, the prescale counter provides both 1 Hz and 10 Hz signals, which can be brought out as bonding options.

Time Setting Inputs: Both fast and slow setting inputs, as well as a hold input, are provided. Internal depletion devices provide the normal timekeeping function. Switching any of these inputs (one at a time) to V_{DD} results in the desired time setting function.

The three gates in the counter chain *(Figure 1)* are used for setting time. During normal operation, gate A connects the shaper output to a prescale counter (÷50 or ÷60); gates B and C cascade the remaining counters. Gate A is used to inhibit the input to the counters for the duration of slow, fast or hold time-setting input activity. Gate B is used to connect the shaper output directly to a seconds counter (÷60), the condition for slow advance. Likewise, gate C connects the shaper output directly to a minutes counter (÷60) for fast advance.

Fast set then, advances hours information at one hour per second and slow set advances minutes information at one minute per second.

12 or 24-Hour Select Input: This input is used to program the hours counter to divide by either 12 or 24, thereby providing the desired display format. The 12-hour display format is selected by connecting this input to V_{DD}; leaving the input unconnected (internal depletion device) selects the 24-hour format.

Output Multiplexer Operation: The seconds, minutes, and hours counters continuously reflect the time of day. Outputs from each counter (indicative of both units and tens of seconds, minutes, and hours) are time-division multiplexed to provide digit-sequential access to the time data. Thus, instead of requiring 42 leads to interconnect a 6-digit clock and its display (7 segments per digit), only 13 output leads are required. The multiplexer is addressed by a multiplex divider decoder, which is driven by a multiplex oscillator. The oscillator and external timing components set the frequency of the multiplexing function and, as controlled by the 4 or 6-digit select input, the divider determines whether data will be output for 4 or 6 digits. A zero-blanking circuit suppresses the zero that would otherwise sometimes appear in the tens-of-hours display; blanking is effective only in the 12-hour format. The multiplexer addresses also become the display digit-enable outputs. The multiplexer outputs are applied to a decoder which is used to address a programmable (code converting) ROM. This ROM generates the final output codes, i.e., $\overline{\text{BCD}}$ and 7-segment. The sequential output order is from digit 6 (unit seconds) through digit 1 (tens of hours).

Multiplex Timing Input: The multiplex oscillator is shown in *Figure 2*. Adding an external resistor and capacitor to this circuit via the multiplex timing input (as shown in *Figure 4a*) produces a relaxation oscillator. The waveform at this input is a quasi-sawtooth that is squared by the shaping action of the Schmitt Trigger in *Figure 2*. *Figure 3* provides guidelines for selecting the external components relative to desired multiplex frequency.

Figure 4 also illustrates two methods of synchronizing the multiplex oscillator to an external timebase. The external RC timing components may be omitted and this input may be driven by an external timebase; the required logic levels are the same as 50 or 60 Hz input.

Reset: Applying V_{DD} to this input resets the counters to 0:00:00.00 in 12-hour format and 00:00:00.00 in 24-hour formats leaving the input unconnected (internal depletion pull-up) selects normal operation. Proper reset will be ensured when V_{DD} to V_{SS} slew rate is no faster than one volt per microsecond. This can be accomplished with a capacitor from the reset input to V_{SS}.

4 or 6-Digit Select Input: Like the other control inputs, this input is provided with an internal depletion pull-up device. With no input connection the clock outputs data for a 4-digit display. Applying V_{DD} to this input provides a 6-digit display.

Output Enable Input: With this pin unconnected the $\overline{\text{BCD}}$ and 7-segment outputs are enabled (via an internal depletion pull-up). Switching V_{DD} to this input inhibits these outputs. (Not applicable to MM5312, MM5313, and MM5315 clocks.)

Output Circuits: *Figure 5a* illustrates the circuit used for the $\overline{\text{BCD}}$ and 7-segment outputs. *Figure 5b* shows the digit enable output circuit. *Figure 6* illustrates interfacing these outputs to standard and low power TTL. *Figures 7 and 8* illustrate methods of interfacing these outputs to common anode and common cathode LED displays, respectively. A method of interfacing these clocks to gas discharge display tubes is shown in *Figure 9*. When driving gas discharge displays which enclose more than one digit in a common gas envelope, it is necessary to inhibit the segment drive voltage(s) during inter-digit transitions. *Figure 9* also illustrates a method of generating a voltage for application to the output enable input to accomplish the required inter-digit blanking.

Functional Description (Cont'd)

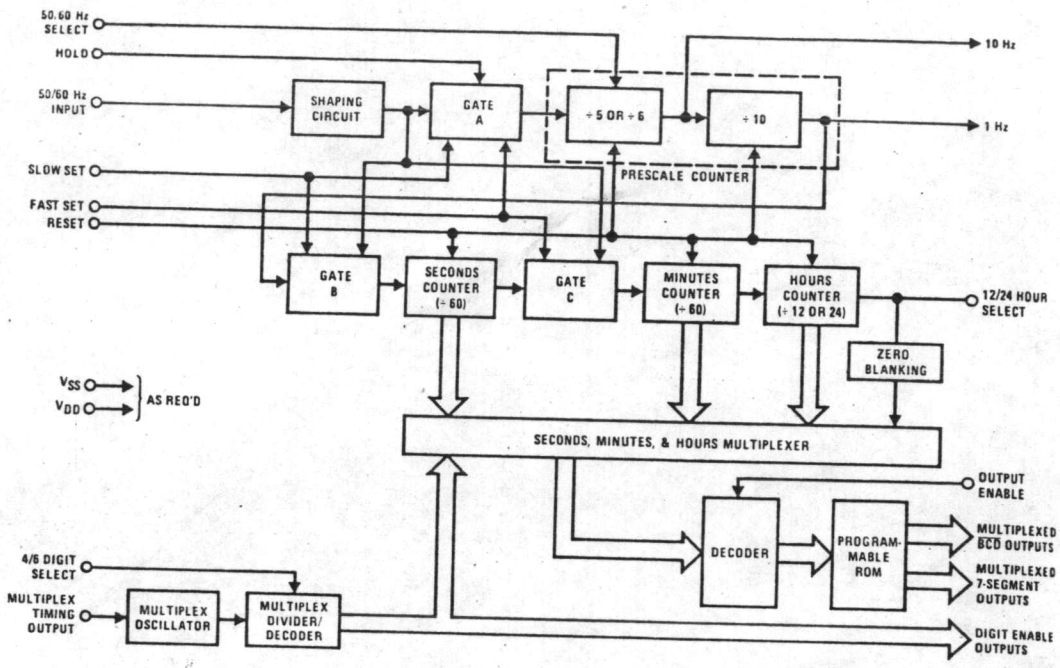


FIGURE 1. MM5309 Digital Clock Block Diagram

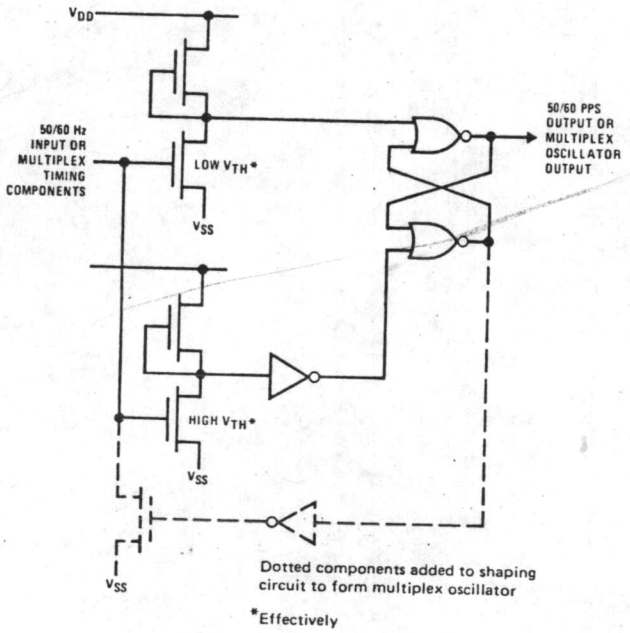


FIGURE 2. 50/60 Hz Shaping Circuit/Multiplex Oscillator

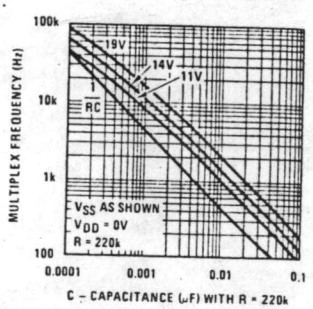


FIGURE 3. Multiplex Timing Component Selection Gu

Functional Description (Cont'd)

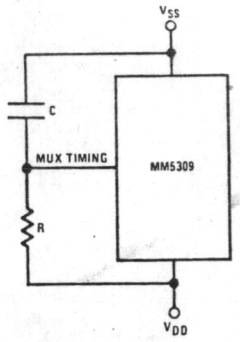


FIGURE 4a. Relaxation Oscillator

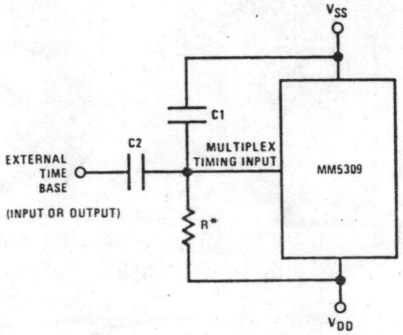


FIGURE 4b. External Time Base

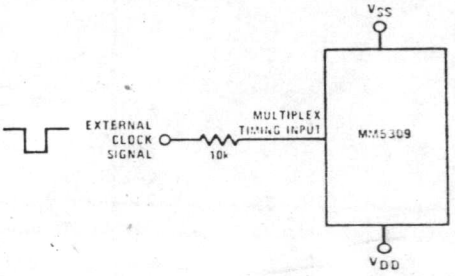


FIGURE 4c. External Clock

Note. Free running frequency should be set to run slightly lower than system frequency over temperature. External time base may be input or output.
* R=100k.

FIGURE 4. Synchronizing or Triggering Multiplex Oscillators

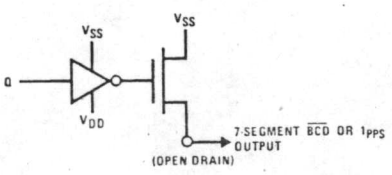


FIGURE 5a

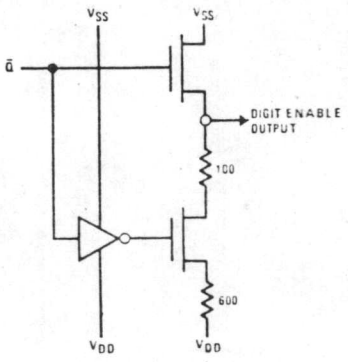
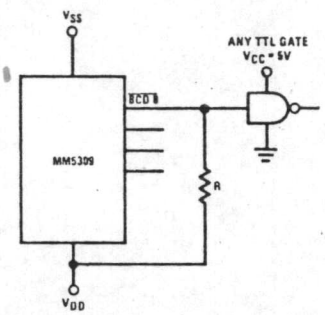


FIGURE 5b

FIGURE 5. Output Circuits

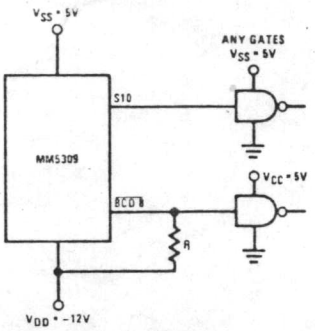
Functional Description (Cont'd)

MOS to Low Power TTL Interface



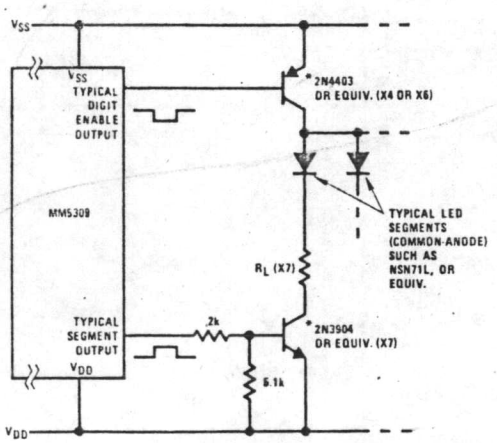
For V_{SS} = 5, V_{DD} = 12, R = 10k
For V_{SS} = 10 to 17V, V_{DD} = Gnd, R = 3k

MOS to TTL Interface



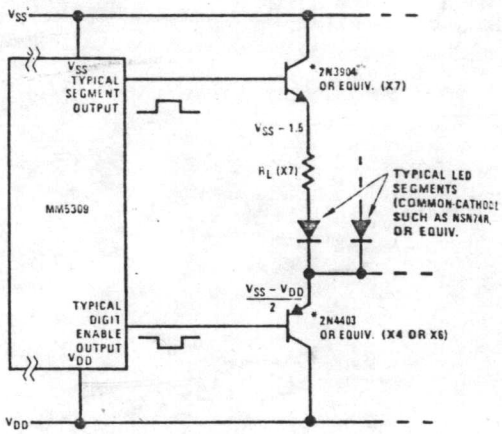
For V_{SS} = 5, V_{DD} = −12, R = 7.5k
Note. Digit select will drive TTL directly when 5, −12 supplies are used.

FIGURE 6. Interfacing TTL



$$R_L = \frac{V_{SS} - V_{DD} - V_F - 0.6V}{N(I_F)}$$

Where R_L as in kΩ
And V_F = forward drop of LED
0.6V ≈ voltage drop of transistors
N = number of digits in display
I_F = required average LED current



$$R_L = \frac{V_{SS} - V_{DD})/2 - V_F - 1.5V}{N(I_F)}$$

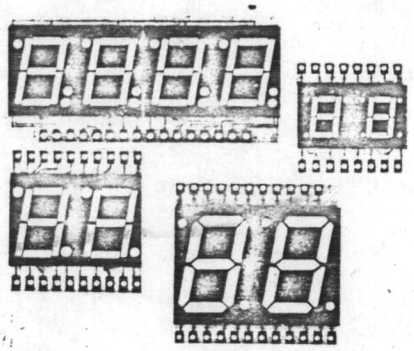
Where R_L is in kΩ
And V_F = forward drop of LED
0.9V = voltage drop of transistors
N = number of digits in display
I_F = required average LED current

*Transistors may be replaced by DM75491, DM75492, DM8861, DM8863 or equivalent segment/digit drivers.

FIGURE 7. Interfacing Common Anode LED Displays

FIGURE 8. Interfacing Common Cathode LED Displays

Displays



multidigit LED numeric series

general description

Multidigit GaAsP LED reflective displays from National Semiconductor, represent the latest in design advances in 0.3", 0.5" and 0.7" formats. The series provides the designer with an effective, easy to implement answer to the need for an inexpensive large numeric display.

Basically 2-digit and 4-digit displays, the units are end stackable for applications requiring additional digits. When combined with the options for overflow, polarity and other indications, virtually all display requirements can be satisfied. Versatility is offered the designer with direct drive and multiplex versions in both the common anode and common cathode forms. Electrical contact is by PCB type terminals on the edges of the display.

The optical design of this display series, creates a distinct easy-to-read display with a wide viewing angle, excellent "ON-OFF" contrast and segment uniformity.

applications

- Test and measurement equipment
- Consumer products
- Instrumentation
- Industrial controls
- Digital instruments
- Desk top calculator
- Clocks
- Elevator floor indicator
- TV channel indicator

absolute ratings

Average Current/Segment	20 mA max
Peak Current/Segment	75 mA max
Reverse Voltage/Segment	3.0V max
Operating and Storage Temperature	−20°C to +70°C
Relative Humidity at 35°C	98%
Terminal Temperature (Soldering, 5 seconds)	230°C

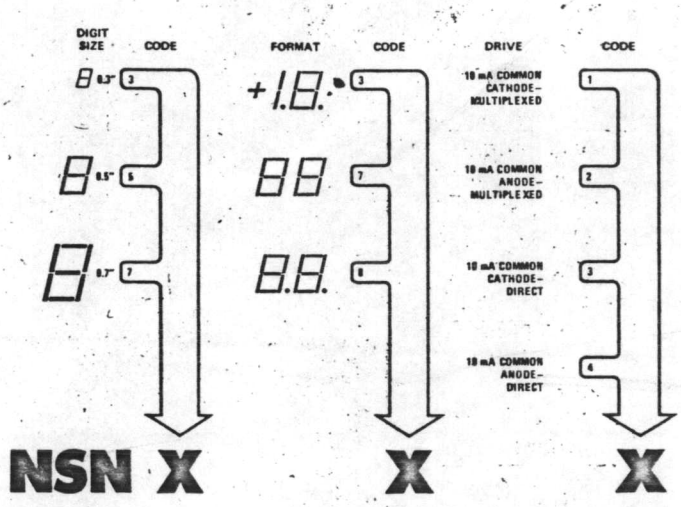
electrical and optical characteristics $T_A = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Segment Light Intensity (Peak)	10 mA/Seg. Peak	0.10	0.20		mcd
Digit and D.P. Light Intensity (Peak)	10 mA/Seg. Peak	0.80	1.6		mcd
Segment Forward Voltage	10 mA/Seg. Peak		1.7	2.0	V
Segment Reverse Voltage	100μA/Seg.	3.0	8.0		V
Peak Wavelength			660		nm
Spectral Width, Half-Intensity			40		nm
Viewing Angle, Off Axis			60		degrees
Intensity Matching	10 mA/Seg. Avg.		±33		%

recommended display processing

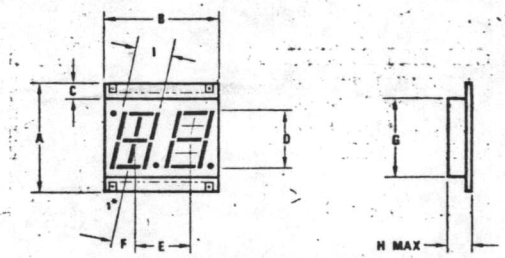
The multidigit series display is constructed on a standard printed circuit board substrate and covered with a plastic lens. The edge connector tab will stand a temperature of 230°C for 5 seconds. The display lens area must not be elevated in temperature above 70°C. To do so will result in permanent damage to the display. Since the display is not hermetic, immersion of the entire package during flux and clean operations may cause condensation of flux or cleaner on the underside of the lens. It is recommended that only the edge connectors be immersed. Only rosin core solder, solid core solder, and low activity organic fluxes are recommended. Cleaning solvents are Freon TF, Isopropanol, Methanol, or Ethanol. These solvents are recommended only at room temperature and for short time periods. The use of other solvents or elevated temperature use of the recommended solvents may cause permanent damage to the lens or display.

available display formats (Dual Digits)



DEVICES CURRENTLY AVAILABLE	
NSN334	+1.8.
NSN381	8.8.
NSN382	8.8.
NSN373	88
NSN374	88
NSN534	+1.8.
NSN581	8.8.
NSN582	8.8.
NSN583	8.8.
NSN584	8.8.
NSN734	+1.8.
NSN781	8.8.
NSN782	8.8.
NSN783	8.8.
NSN784	8.8.

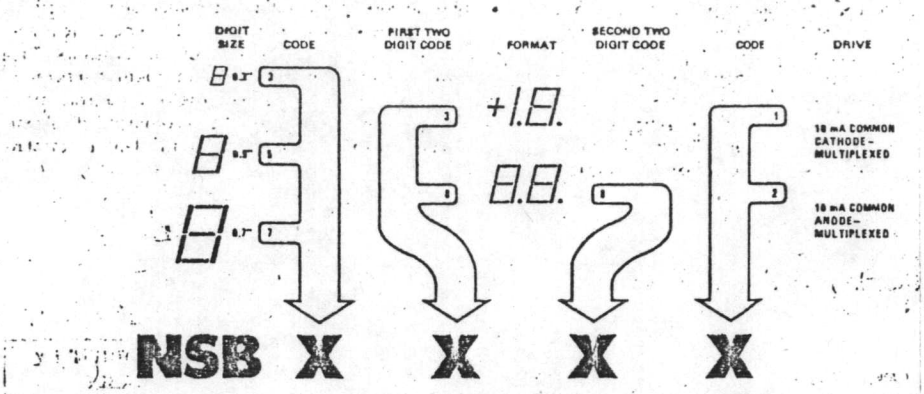
physical dimensions



*Pin 1 as shown, pin out follows counterclockwise

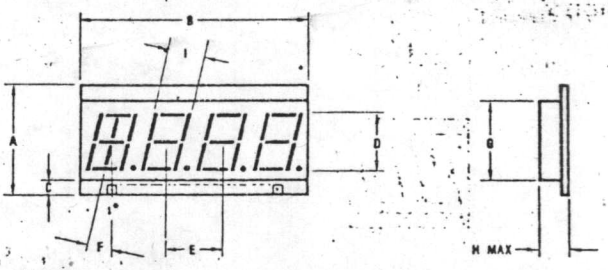
DIMENSIONS									
DIGIT SIZE	A	B	C	D	E	F	G	H	I
0.3	0.85	0.8	0.175	0.3	0.4	5°	0.5	0.225	0.188
0.5	1.05	1.0	0.175	0.5	0.5	10°	0.7	0.28	0.3
0.7	1.25	1.2	0.180	0.7	0.6	10°	0.89	0.3	0.38

available display formats (Quad Digits)



DEVICES CURRENTLY AVAILABLE
NSB3382 +1.8.8.8.
NSB3881 8.8.8.8.
NSB3882 8.8.8.8.
NSB5382 +1.8.8.8.
NSB5881 8.8.8.8.
NSB5882 8.8.8.8.
NSB7382 +1.8.8.8.
NSB7881 8.8.8.8.
NSB7882 8.8.8.8.

physical dimensions



*Pin 1 as shown, pin out follows counterclockwise

DIMENSIONS									
DIGIT SIZE	A	B	C	D	E	F	G	H	I
0.3	0.83	1.59	0.165	0.3	0.4	5°	0.5	0.225	0.188
0.5	1.0	1.99	0.180	0.5	0.5	10°	0.7	0.28	0.3
0.7	1.15	2.39	0.180	0.7	0.6	10°	0.89	0.3	0.38

connection tables (Continued) (Quad Digits)

PIN NUMBER	NSB3382	NSB3881	NSB3882
1	NC	NC	NC
2	Cathode E	Anode E	Cathode E
3	Common Anode Digit 1	Common Cathode Digit 1	Common Anode Digit 1
4	Cathode J Digit 1	NC	NC
5	Cathode H Digit 1	NC	NC
6	Common Anode Digit 2	Common Cathode Digit 2	Common Anode Digit 2
7	Cathode D	Anode D	Cathode D
8	Cathode G	Anode G	Cathode G
9	NC	NC	NC
10	Common Anode Digit 3	Common Cathode Digit 3	Common Anode Digit 3
11	Cathode B	Anode B	Cathode B
12	Cathode A	Anode A	Cathode A
13	Cathode F	Anode F	Cathode F
14	Common Anode Digit 4	Common Cathode Digit 4	Common Anode Digit 4
15	Cathode D.P.	Anode D.P.	Cathode D.P.
16	Cathode C	Anode C	Cathode C

segment identification

ประวัติ

นายสุธนะ สามโกเศศ เกิดเมื่อวันที่ 25 เมษายน พุทธศักราช 2494 ที่โรงพยาบาลศิริราช จังหวัดธนบุรี ได้รับปริญญาบัณฑิต สาขาวิศวกรรมไฟฟ้า จากมหาวิทยาลัยสงขลานครินทร์ เมื่อพุทธศักราช 2517 และได้เข้าทำงานที่การไฟฟ้าฝ่ายผลิตแห่งประเทศไทย ในปีเดียวกันลาออกจากการไฟฟ้าฝ่ายผลิตเพื่อทำธุรกิจส่วนตัว เมื่อพุทธศักราช 2519 ระหว่างที่ทำงานอยู่ที่การไฟฟ้าฝ่ายผลิตแห่งประเทศไทย ได้รับตำแหน่งวิศวกรอันดับหนึ่งประจำแผนกโทรมาตร กองระบบสื่อสารฝ่ายบำรุงรักษาไฟฟ้า ทำงานเกี่ยวกับระบบโทรมาตรซึ่งใช้ระบบ เอฟเอสเค (FSK, Frequency Shift Keying) ระหว่างที่ทำธุรกิจส่วนตัว ได้สร้างเครื่องโทรศัพท์แบบกดปุ่ม ใช้งานได้กับระบบโทรศัพท์ พีเอบีเอ็กซ์ (PABXs) ต่อมาได้เข้าศึกษาต่อที่บัณฑิตวิทยาลัย จุฬาลงกรณ์มหาวิทยาลัย ภาควิชาวิศวกรรมไฟฟ้า ในปีการศึกษาพุทธศักราช 2520 ต่อมาได้เข้าทำงานที่บริษัทการบินไทย จำกัด ในปีพุทธศักราช 2522 จนกระทั่งปัจจุบัน ในตำแหน่งออบเปอร์เรชั่นส์เอ็นจิเนียร์ (Operations Engineer) ประจำแผนกเทคนิคการบิน ฝ่ายปฏิการ