การปลูกนาโนไวร์แกลเลียมอาร์เซไนด์ด้วยการใช้ตัวเองเป็นตัวเร่งปฏิกิริยาโดยวิธีปลูกผลึกจากลำโมเลกุลโดยตรงลงบนแผ่นฐานแกลเลียมอาร์เซไนด์ (111)B

นายสมัชชา วรธำรง

จุฬาลงกรณ์มหาวิทยาลัย
Chulalongkorn University

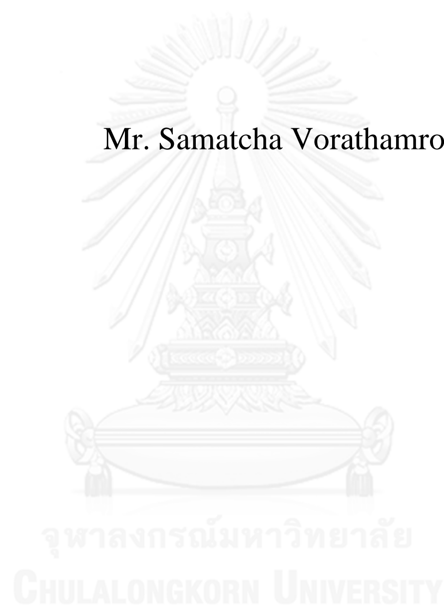
บทคัดย่อและแฟ้มข้อมูลฉบับเต็มของวิทยานิพนธ์ตั้งแต่ปีการศึกษา 2554 ที่ให้บริการในคลังปัญญาจุฬาฯ (CUIR)
เป็นแฟ้มข้อมูลของนิสิตเจ้าของวิทยานิพนธ์ ที่ส่งผ่านทางบัณฑิตวิทยาลัย
The abstract and full text of theses from the academic year 2011 in Chulalongkorn University Intellectual Repository (CUIR)
are the thesis authors' files submitted through the University Graduate School.

วิทยานิพนธ์นี้เป็นส่วนหนึ่งของการศึกษาตามหลักสูตรปริญญาวิศวกรรมศาสตรดุษฎีบัณฑิต
สาขาวิชาวิศวกรรมไฟฟ้า ภาควิชาวิศวกรรมไฟฟ้า
คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย
ปีการศึกษา 2559

ลิขสิทธิ์ของจุฬาลงกรณ์มหาวิทยาลัย

GROWTH OF SELF-CATALYZED GaAs NANOWIRES BY MOLECULAR BEAM EPITAXY DIRECTLY ON GaAs (111)B SUBSTRATES

Mr. Samatcha Vorathamrong



A Dissertation Submitted in Partial Fulfillment of the Requirements
for the Degree of Doctor of Philosophy Program in Electrical Engineering
Department of Electrical Engineering
Faculty of Engineering
Chulalongkorn University
Academic Year 2016
Copyright of Chulalongkorn University

Thesis Title	GROWTH OF SELF-CATALYZED GaAs NANOWIRES BY MOLECULAR BEAM EPITAXY DIRECTLY ON GaAs (111)B SUBSTRATES
By	Mr. Samatcha Vorathamrong
Field of Study	Electrical Engineering
Thesis Advisor	Associate Professor Dr.Somchai Ratanathammaphan

---

Accepted by the Faculty of Engineering, Chulalongkorn University in Partial Fulfillment of the Requirements for the Doctoral Degree

....Dean of the Faculty of Engineering
(Associate Professor Dr.Supot Teachavorasinskun)

THESIS COMMITTEE

....Chairman
(Professor Dr.Piyasan Praserthdam)

....Thesis Advisor
(Associate Professor Dr.Somchai Ratanathammaphan)

....Examiner
(Assistant Professor Dr.Chanin Wissawinthanon)

....Examiner
(Professor Dr.Somsak Panyakaew)

....External Examiner
(Associate Professor Dr.Banyong Toprasertpong)

CHULALONGKORN UNIVERSITY

สมัชชา วรธำรง : การปลูกนาโนไวร์แกลเลียมอาร์เซไนด์ด้วยการใช้ตัวเองเป็นตัวเร่งปฏิกิริยาโดยวิธีปลูกผลึกจากลำโมเลกุลโดยตรงลงบนแผ่นฐานแกลเลียมอาร์เซไนด์ (111)B (GROWTH OF SELF-CATALYZED GaAs NANOWIRES BY MOLECULAR BEAM EPITAXY DIRECTLY ON GaAs (111)B SUBSTRATES) อ.ที่ปรึกษาวิทยานิพนธ์หลัก: รศ. ดร.สมชัย รัตนธรรมพันธ์, 62 หน้า.

วิทยานิพนธ์นี้ได้ทำการศึกษาเพื่อพัฒนาการปลูกนาโนไวร์แกลเลียมอาร์เซไนด์ด้วยกระบวนการ VLS อย่างเป็นระบบ โดยวิธีการนี้สามารถปลูกนาโนไวร์ลงบนแผ่นฐานแกลเลียมอาร์เซไนด์ (111)B ได้โดยตรง แทนการใช้แผ่นฐานรองซิลิกอนที่ผ่านการฉายผิวด้วยซิลิกอนออกไซด์ดังเช่นการปลูกนาโนไวร์แบบดั้งเดิม โดยวิธีการนี้แก้ไขปัญหาที่พบได้ในการปลูกด้วยวิธีแบบดั้งเดิม ได้แก่ การเอียงของนาโนไวร์ และโครงสร้างปรสิต เป็นต้น สำหรับตัวแปรในการนี้ได้แก่ ความดันฟลักซ์ของแกลเลียมและอุณหภูมิ โดยการแปรค่าตัวแปรและศึกษาผลที่ได้เพื่อหาเงื่อนไขที่เหมาะสมในการปลูกนาโนไวร์ หลังจากนั้นทำการทดลองเพื่อเปรียบเทียบการปลูกนาโนไวร์บนแผ่นฐานแกลเลียมอาร์เซไนด์ (111)B และซิลิกอน (111) ที่ถูกเคลือบผิวด้วยซิลิกอนออกไซด์ด้วยเงื่อนไขเดียวกัน นอกจากนั้นได้ศึกษาการเติบโตของนาโนไวร์ด้วย RHEED ในขณะที่ทำการปลูกผลึก ผลที่ได้พบว่า นาโนไวร์สามารถเกิดขึ้นโดยตรงบนแผ่นฐานแกลเลียมอาร์เซไนด์ (111)B โดยไม่พบการเอียงและโครงสร้างปรสิต ความหนาแน่นของนาโนไวร์ลดลงในขณะที่อุณหภูมิแผ่นฐานรอง อย่างไรก็ตามอัตราการโตของนาโนไวร์มีค่าคงที่ในช่วงอุณหภูมิปลูกที่เหมาะสม โครงผลึกของนาโนไวร์ที่ได้เป็นแบบ WZ ซึ่งแตกต่างจากนาโนไวร์ที่ใช้วิธีดั้งเดิมที่ส่วนใหญ่นั้นเป็นแบบ ZB อันเนื่องมาจากผลของพลังงานพื้นผิวที่แตกต่างกันระหว่างแกเลียมอาร์เซไนด์และซิลิกอน จากการศึกษาการเติบโตของนาโนไวร์พบว่า โครงสร้างนาโนไวร์เริ่มต้นก่อตัวขึ้นจากหยดโลหะขนาดเล็ก ๆ แล้วยืดยาวขึ้นเป็นนาโนไวร์ หยดโลหะที่ไม่สามารถก่อตัวเป็นนาโนไวร์ได้เปลี่ยนรูปก่อตัวเป็นโครงสร้างคล้ายแหวนและกลายเป็นชั้นผลึกต่อไป ข้อมูลที่ได้นำไปสร้างแบบจำลองอย่างง่ายเพื่อทำความเข้าใจกลไกการเกิดของนาโนไวร์ที่ใช้หยดแกลเลียมเป็นตัวเร่งปฏิกิริยา

ภาควิชา	วิศวกรรมไฟฟ้า	ลายมือชื่อนิสิต	....
สาขาวิชา	วิศวกรรมไฟฟ้า	ลายมือชื่อ อ.ที่ปรึกษาหลัก	....
ปีการศึกษา	2559		

5671428621 : MAJOR ELECTRICAL ENGINEERING
KEYWORDS: GAAS NANOWIRE / GAAS (111)B SUBSTRATE / MOLECULAR BEAM EPITAXY / SELF-CATALYTIC VLS / DIRECTLY / WITHOUT SIO2

SAMATCHA VORATHAMRONG: GROWTH OF SELF-CATALYZED GaAs NANOWIRES BY MOLECULAR BEAM EPITAXY DIRECTLY ON GaAs (111)B SUBSTRATES. ADVISOR: ASSOC. PROF. DR.SOMCHAI RATANATHAMMAPHAN, 62 pp.

This dissertation is a systematic investigation to improve the growth method of GaAs nanowires by molecular beam epitaxy via self-catalytic VLS mode. The nanowire can be grown directly on GaAs (111)B substrates instead of SiO_2-covered substrates. The merit of this technique is to eliminate the common problems that occur with nanowires grown by conventional VLS mode such as tilted nanowire, and parasitic structure. Growth parameters namely Ga flux pressure, and growth temperature were varied to search the optimal conditions to grow nanowires. After obtaining the optimal conditions, the nanowire growth was performed on both GaAs (111)B and SiO_2 coated Si (111) for a comparison. Moreover, the nanowire samples were characterized by in-situ RHEED under varied growth time to study the growth evolution. Results show that GaAs nanowires are able to form directly on GaAs (111)B substrates without the existence of tilted wire, and parasitic structure. Density of nanowires increases with increasing the growth temperature however the growth rate remains nearly constant under a constant Ga flux in the optimal growth temperature. Nanowires grown by our method adopt WZ structure unlike conventional VLS nanowires which mostly adopt ZB structure, this is likely to be a result from different surface energy of substrate surface. Growth evolution shows that nanowires started forming as small dots before elongating to nanowire structure. Dots that unable to become nanowires are crystallized under As pressure to ring-like structure before getting buried by buffer layer. A simple growth model was proposed for better understanding of the self-catalyzed growth mode mechanism with using Ga as seed particles.

Department: Electrical Engineering Student's Signature ....
Field of Study: Electrical Engineering Advisor's Signature ....
Academic Year: 2016

จุฬาลงกรณ์มหาวิทยาลัย
CHULALONGKORN UNIVERSITY

ACKNOWLEDGEMENTS

I would like to express my gratitude to all people who assist and support me to complete this thesis.

Special thanks to my advisor, Assoc.Prof. Dr.Somchai Ratanathammaphan, who always gives me useful suggestions. I would like to thank my thesis committee including Prof. Dr.Piyasan Prasertdam, Prof. Dr.Somsak Panyakeow, Assoc.Prof. Dr.Banyong Toprasertpong, and Asst.Prof. Dr.Chanin Wissawinthanon for all advices during my proposal and defend.

I am very thankful to Ms.Patchareewan Prongjit who trained me to operate MBE system and started our research on nanowire together for the first time in our lab as well as Ms. Kamonchanok Khoklang, Ms.Nattapa Prapasawad, Ms.Zon, and Mr.Thanavorn Poempool for their helps in MBE growth and for being very good friends of mine.

I am very grateful to Ms.Chiraporn Tongyam's support for SEM characterization. My works would not have finished without Ms.Chiraporn's works.

I appreciate dedication from our staffs including Mr.Supachok Thainoi, Mrs. Kwanruan Thainoi, and Mr.Pattana Phuntuwong to keep this lab operating.

Another thing that is indispensable for my works is all financial supports from the Ratchadapisek Sompoch Endowment Fund (2015), Chulalongkorn University (CU-58-056-EN), the 100th Anniversary Chulalongkorn University Fund for Doctoral Scholarship, National Science and Technology Development Agency, National Nanotechnology Center, Asian Office of Aerospace Research and Development (FA2386-14-1-4081) and Office of Naval Research Global.

Finally, I have to thank my parents for their love and support. Their encouragements and advices will always be precious for me.

CONTENTS

Page

THAI ABSTRACT iv
ENGLISH ABSTRACT v
ACKNOWLEDGEMENTS vi
CONTENTS vii
Chapter 1 Introduction 1
1.1 Background and motivation 1
1.2 Objectives 2
Chapter 2 Fundamental knowledge 3
2.1 Nanowire overview 3
2.2 Nanowire properties 4
2.2.1 Electrical properties 4
2.2.2 Optical properties 5
2.3 Nanowire fabrication processes 7
2.3.1 Selective Area Epitaxy (SAE) 7
2.3.2 Au-catalyzed Vapor Solid Liquid (VLS) method 8
2.3.3 Oxide-assisted VLS method 9
2.3.4 Self-catalyzed VLS growth of GaAs nanowires without SiO_2 11
Chapter 3 Experimental procedure 13
3.1 Molecular Beam Epitaxy (MBE) 13
3.2 Reflection High-Energy Electron Diffraction (RHEED) 15
3.3 Scanning Electron Microscope (SEM) 16
3.4 X-Ray Diffraction (XRD) analysis 17
Chapter 4 Effect of Ga flux on self-catalyzed GaAs nanowires without SiO_2 20
4.1 Experimental detail 20
4.2 Results and discussions 21
4.2.1 Surface morphology 21
4.2.2 Growth rate 22
4.2.3 Nanowire density 23

Page

4.2.4 Elemental composition 24

4.2.5 Vertical yield 25

4.2.6 Crystal structure 26

4.3 Summary 26

Chapter 5 Effect of growth temperature on self-catalyzed GaAs nanowires without SiO_2 28

5.1 Experimental detail 28

5.2 Results and discussions 29

5.2.1 Surface morphology 29

5.2.2 Growth rate 29

5.2.3 Nanowire density 31

5.2.4 Elemental composition 32

5.2.5 Vertical yield 33

5.2.6 Crystal structure 33

5.3 Summary 34

Chapter 6 Comparison of self-catalyzed GaAs nanowire grown directly on GaAs substrate and on Si substrate with native SiO_2 35

6.1 Experimental detail 35

6.2 Results and discussions 36

6.2.1 Surface morphology 36

6.2.2 Growth rate, density, vertical yield, and elemental composition 37

6.2.3 Crystal structure 39

6.2.4 RHEED patterns analysis 40

6.3 Summary 44

Chapter 7 Growth mechanism of GaAs nanowires on GaAs (111)B susbtrates without SiO_2 layer 45

7.1 Experimental detail 45

7.2 Results and discussions 46

7.2.1 Growth evolution 46

Page

7.2.2 Surface morphology analysis 49
7.2.3 RHEED intensity evolution 51
7.2.4 Growth model 52
7.3 Summary 53
Chapter 8 Conclusion 55
REFERENCES 57
APPENDIX 59
VITA 62

Chapter 1
Introduction

1.1 Background and motivation

Nanostructure technology has been one of the topic that received a large amount of attention from various research fields lately. As Richard Feymann said "There's Plenty of Room at the Bottom.", introduction of nanostructures will open up many possibilities which are currently limited in bulk materials. At nano-size, materials experience quantum effects such as carrier confinement, tunneling, etc. which cause them to behave differently from larger-scale materials. Many nanostructures such as quantum well, quantum dot, or nanowire were proposed and developed for various kinds of application hence improving the fabrication processes of nanostructures has become more and more crucial topics with many factors that need to be considered such as simplicity of the process, product yield, and compatibility with the old existing processes. Of all nanostructures, we focus our interest in the nanowire especially GaAs nanowire since its fabrication process is compatible with molecular beam epitaxy technique which is the main research of our laboratory, moreover we can see some under-developed area and room for improvement in this research.

Nanowire is an elongated nanostructure which possesses many interesting properties that make it a potential for many applications. The nanowire is one of the candidates to replace conventional Silicon planar structure in electronics devices. The elongated shape makes it a natural carrier confined structure which is very useful for optical applications such as LED or LASER. Its high surface-area-to-volume ratio is an ideal for electron exchanger and light absorption device. However for GaAs nanowire, the development for applications is occasionally held back by fabrication processs. The fabrication of GaAs nanowires seems to be slightly problematic since the materials need to be collected in specific area for a certain period of time to form wires instead of uniformly forming layer by layer on substrates like typical

semiconductor fabrication. Currently the existing fabrication processes of GaAs nanowires still have some issues such as complication and expensiveness of the process, and contamination of undesired impurities, or issue that causes deformation of surface morphology. All of these problems occur inherently which makes them difficult to be eliminated since they are originated in the processes. These problems occasionally prevent GaAs nanowires from being studied and developed further for future applications hence it becomes necessary to have more advanced and efficient fabrication process to bring the nanowire to its full potential. We believe that the improved nanowire growth process will attract more extensive researches and developments not only for GaAs nanowire but also for all semiconductor nanowires that have similar fabrication process.

1.2 Objectives

Our objectives are to improve and simplify the process of nanowire fabrication as well as eliminating all inherent problems that normally occur in the conventional growth process by proposing a new process to fabricate GaAs nanowires based on molecular beam epitaxy technique. This research begins by finding proper conditions to grow GaAs nanowires under our process by growing GaAs nanowires at the different growth parameters namely Ga flux pressure, and growth temperature. All nanowire samples will be characterized and compared to obtain the proper conditions. To understand the basic growth mechanism, the nanowires will be grown at varied growth time while being characterized by in-situ investigation. Furthermore, the growth will be performed by our process and the conventional growth process at the same growth parameters, the grown nanowires will be extensively characterized and analyzed to address the advantages and drawbacks of both processes.

Chapter 2
Fundamental knowledge

This chapter will provide the fundamental and the basic knowledge which related to nanowires including theirs characteristics, properties, and current well-known fabrication methods. Unique properties that make the nanowires stand out from other nanostructures as well as advantages, drawbacks, and all issues of each fabrication method of nanowires will be addressed in order to understand the importance of improving nanowire growth process. Moreover at the end of this chapter, we will give the concept of our proposing method as a solution to overcome the existing problems occurring in the current fabrication methods.

2.1 Nanowire overview

Nanowire is a cylindrical-shaped or rod-like structure with a diameter in the range of nanometres. Nanowires can be manufactured from different types of material namely metals, semiconductors, and insulators. Due to the elongated shape, nanowire possesses a high surface-area-to-volume ratio which makes it an ideal structure for applications that involves carrier exchanges. Quantum effect such as tunneling, and quantum confinement also occurs in the nanowire owing to its diameter size. Nanowire is also regarded a one dimensional (1-D) structure as its shape is dominated by one dimensional space. Example images of nanowire morphology are provided in Fig. 2.1 (a)-(b).

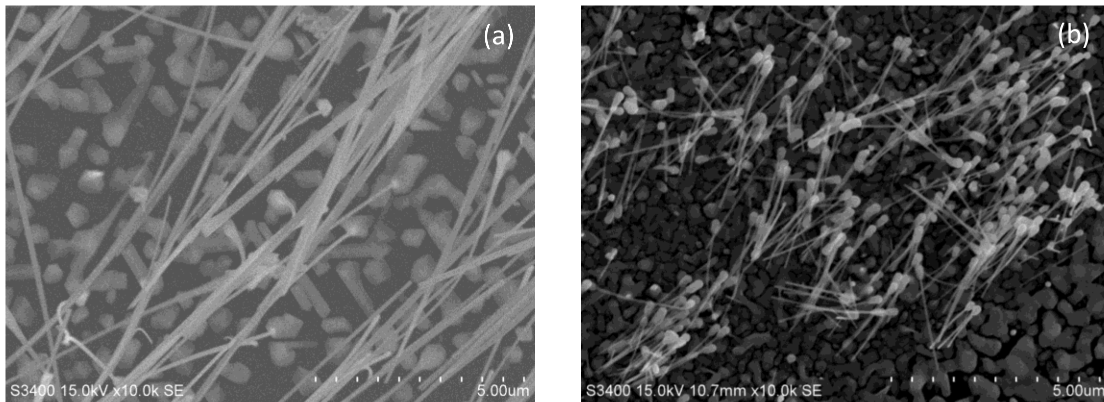


Fig. 2.1 Scanning electron microscope images of GaAs nanowires on Si (111) substrate (a) [1], and GaAs nanowires with GaSb parts on the top on Si (111) substrate (b)[2]

2.2 Nanowire properties

Nanowire was proposed as a promising building block for nanotechnology development[3]. Due to size and unique shape, nanowire possesses many interesting properties that make it standing out from bulk materials and other nanostructures. Moreover nanowire remarkable properties also depend on its size and diameter which can be controlled by varying parameters during the fabrication process. With fine-tuning in fabrication parameters and optimized conditions, the nanowires can be produced with properties as intended.

2.2.1 Electrical properties

Normally electrical conductivity of nanowires is lower than of bulk materials due to the large surface-area-to-volume ratio causing a high carrier recombination rate at the surface. In order to reduce the surface recombination, a core-shell structure which consists of a nanowire as a core passivated by a material with higher bandgap (E_g) as a shell as displayed in Fig. 2.2 (a) was introduced. The difference between the bandgaps of nanowire and shell creates electron and hole barriers at the interface and prevents electron and hole pairs from recombination at the surface as seen in Fig. 2.2 (b). This phenomenon is also known as “carrier confinement” which is very useful for

implementation of nanowires in applications like nanowire-based photovoltaic cell[4], or nanowire transistor[5].

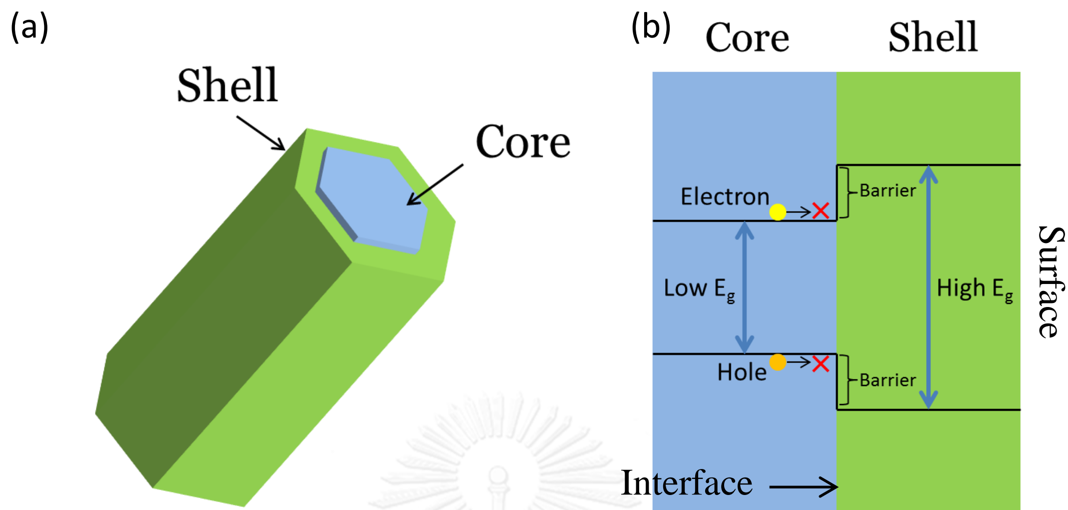


Fig. 2.2 Core-shell structure of a nanowire (a) the core-shell interface, and the electron and hole barriers created by the difference between E_g of core and shell materials

Moreover, due to the unique shape and size of nanowire, its energy level tends to split into discrete values which affect the electron transport. This effect was found by Yi et al.[6] and is very noticeable in nanowires with small diameters. Doping of semiconductor nanowires can be problematic due to its small size. A high concentration of doping is required to obtain uniform dopant distribution and avoid full depletion in wire structure[7]. With development fabrication and doping process, semiconductor nanowire can be a potential candidate for a device like Field-Effect Transistor (FET).

2.2.2 Optical properties

Optical absorption of nanowires shows very promising results by its light trapping property. Since the diameter of a nanowire have a smaller or similar size to the light wavelength, so the nanowire act like “a leaky-mode resonator” under illumination[8]. Light is passing through nanowire’s core while gradually radiating its

power to the surroundings as seen in Fig. 2.3 (a). This effect follows the intuitive resonant condition.

$$m\lambda_{eff} = 2\pi r \tag{2.1}$$

Where m = optical mode (0, 1, 2, 3, 4, …)

λ_{eff} = effective wavelength

and r = radius of nanowire

This effect significantly boosts the light absorption in the nanowire. According to Mie's theory, nanowire structure can increase light absorption up to 14 – 70 times compared to bulk materials[8]. This property makes nanowire a potential candidate for photovoltaic applications. Krogstrup et al. successfully fabricated single-nanowire solar cells which had efficiency exceeded Shockley-Queisser limit Core-shell structure is still necessary in order to produce high efficiency nanowire-based solar cells[9] since it reduces the surface recombination by a huge amount as discussed in the previous section.

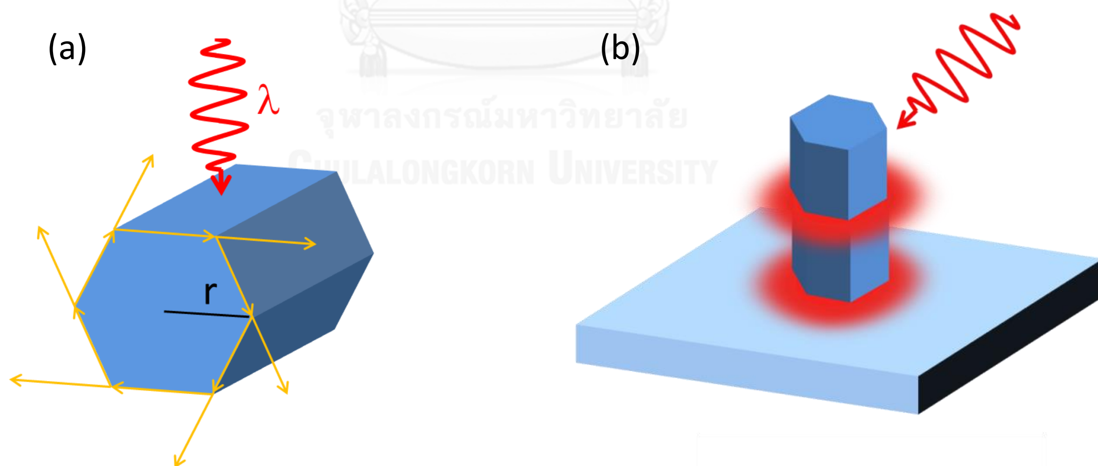


Fig. 2.3 Leaky-mode resonance in a nanowire (a) , and how lights travel through a nanowire as a leaky-mode waveguide (b)

จุฬาลงกรณ์มหาวิทยาลัย
Chulalongkorn University

Photoluminesence (PL) of nanowire structures does not display a vast difference from bulk materials[10] however there are some researches that worth mentioning. Wang et al. discovered that PL signals from nanowires were polarized as opposed to the signals from bulk materials, this is probably due to the difference between carrier lifetime in transverse and longitudinal direction of nanowires[11]. Moreover Yousefi and Kamaluddinfound that the photoluminescence peaks of ZnO nanowires also depend on their diameters[12]. There are many works about nanowire laser as small size and cylindrical shape of nanowire enable laser beam to emit in a very small spot size using a whole nanowire as an optical cavity[13]. However due to difficulty in electrical pumping, there are many works needed to be done before introducing nanowire to commercial applications[14].

2.3 Nanowire fabrication processes

Nanowires can be fabricated with many different types of process such as chemical processing[15], suspension[16], or epitaxial growth, etc. but in this research, we focus on epitaxial growth which is the most common process to fabricate semiconductor nanowires. This process is a bottom-down fabrication which means nanowires are grown by this process from assembly of additional materials. Currently there are three most recognized nanowire growth methods that come under epitaxial growth process including Selective Area Epitaxy, Au-catalyzed Vapor Liquid Solid, and self-catalyzed or oxide-assisted Vapor Liquid Solid.

2.3.1 Selective Area Epitaxy (SAE)

Selective area epitaxy is a method that forces nanowires to grow only in some specific area on patterned substrate[17]. This method starts by patterning substrate with specialized technique like electron beam lithography[18] or other techniques which form nanometer-scale patterns, after that materials are deposited on the substrate and nanowires will grow from the pre-made patterns as seen in Fig. 2.4. SAE yields high quality nanowires, moreover the density and order of nanowires grown by SAE can be fully controlled by modifying the patterns on the substrate. However since substrate patterning requires specialized techniques, this makes SAE

method much more complicated and prevents it from being developed for commercial applications.

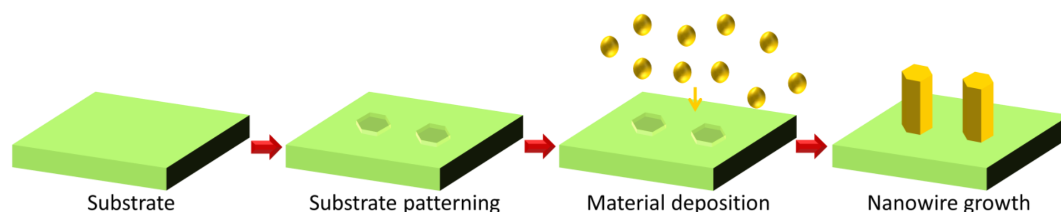


Fig. 2.4 Diagram of nanowire growth by selective area epitaxy

2.3.2 Au-catalyzed Vapor Solid Liquid (VLS) method

This method was first proposed by Wagner and Ellis in 1964[19]. In their experiment, they put a droplet of Au on Silicon substrate surface and performed Chemical Vapor Deposition (CVD) growth of Si, this resulted in the growth of Si whisker instead of typical Si buffer layer. Wagner explained that an Au droplet acted as a sink for incoming Si atoms. Most Si atoms are trapped in the droplet due to higher accommodation coefficient of liquid[20] compared to the solid substrate. After that the droplet becomes saturated with Si atoms, then Si atoms precipitate and Si wire begins to form from the bottom of a droplet as displayed in Fig. 2.5.

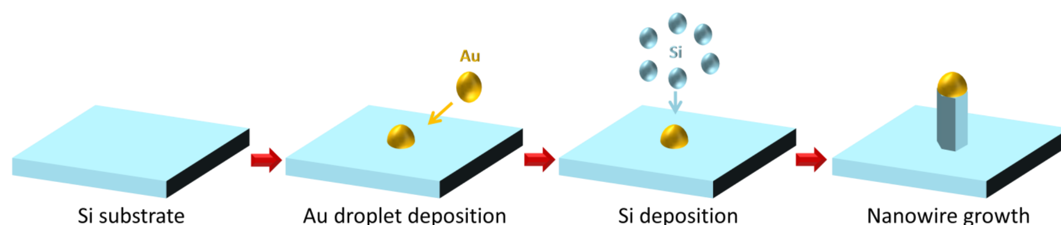


Fig. 2.5 Diagram of Si nanowire growth by Au-catalyzed VLS

according to Wagner's experiment

Since the introduction, the Au-catalyzed VLS method has been developed to grow nanowires with various kinds of materials including III-V and II-VI

semiconductor on many types of substrates[21]. This method is regarded as one of the most well-known technique to grow nanowires due to its simplicity and compatibility with many fabrication techniques. However due to utilization of Au seed particles, nanowires grown by this method suffer from unintentional incorporation of Au atoms which is the cause of deep-level traps[22]. These deep-level traps result in degradation of optical and electrical properties of nanowires due to the higher recombination rate which shortens the carrier lifetime and renders Au-catalyzed nanowires unsuitable for many applications[22].

2.3.3 Oxide-assisted VLS method

It was discovered later that for III-V and II-VI semiconductor nanowires, internal metals which are group II and III elements can be used as seed particles for nanowire growth initiation instead of Au. Foncuberta et al. proposed oxide-assisted VLS method in 2007[23]. In their process Ga droplets were deposited as seed particles on GaAs substrate that covered with ultrathin SiO_2 layer before the deposition of Ga and As and the growth of nanowires occurred from seed particles similar to Au-catalyzed VLS. The addition of ultrathin SiO_2 layer is to prevent Ga atoms from sticking onto substrate surface due to the lower surface energy of SiO_2 compared to bare GaAs[17]. Growth mechanism is quite similar to Au-catalyzed VLS with the exception that Ga droplets are stuck in pinholes[24], small hole-like structures existing in the SiO_2 layer, then incoming Ga atoms are collected in droplets due to the higher accommodation coefficient of liquid[20] after that droplets start to crystallize under As flux and nanowires are formed. This method introduced the term “self-catalyzed VLS” since it uses one of the composition of nanowire itself to initiate the growth. Oxide-assisted VLS mehod is displayed in Fig. 2.6.

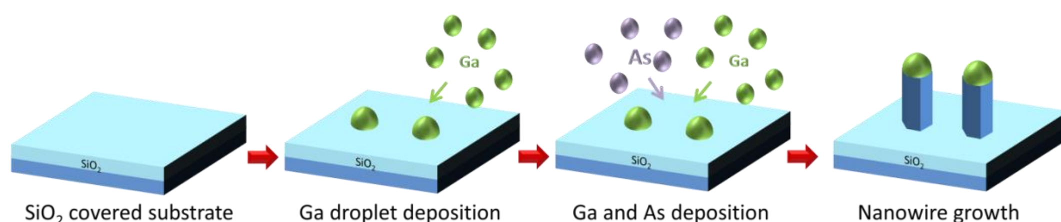


Fig. 2.6 Diagram of GaAs nanowires grown by oxide-assisted VLS method

As this method is Au-free, the issue of unintentional Au incorporation can be completely avoided. Breuer found that the minority carrier lifetime in GaAs nanowires grown by oxide-assisted VLS was almost three magnitudes higher than that of Au-catalyzed GaAs nanowires[10], this shows that without the presence of Au in the process, optical and electrical properties of nanowires are substantially improved.

Even though oxide-assisted VLS can eliminate the problem from Au contamination in nanowires, there are some issues that need to be addressed. First nanowires grown by oxide-assisted VLS as shown in Fig. 2.7 generally suffer from tilted or non-directional growth issues due to non-uniformity of SiO_2 thickness[24]. Straight and vertical nanowires are essential for many applications such as photovoltaic cells[9], the tilted nanowires can bring down efficiency of device or make it unusable. Matteini found that in order to grow oxide-assisted nanowires vertically, morphology, thickness, and roughness of fabricated SiO_2 layer needs to be precisely controlled[24] which is proved to be difficult to achieve. Moreover according to Breuer et al[10], the presence of SiO_2 layer seems to be the cause of parasitic growth, a cluster of leftover materials growing on SiO_2. As previously mentioned, oxide-assisted nanowires initiate from pinholes, materials that are unable to reach pinholes will gather and form bulk structures scattering on substrate surface. This parasitic growth is non-epitaxial and contains many structural defects which can cause the negative effects in nanowire properties and can be problematic for device implementation.

CHULALONGKORN UNIVERSITY

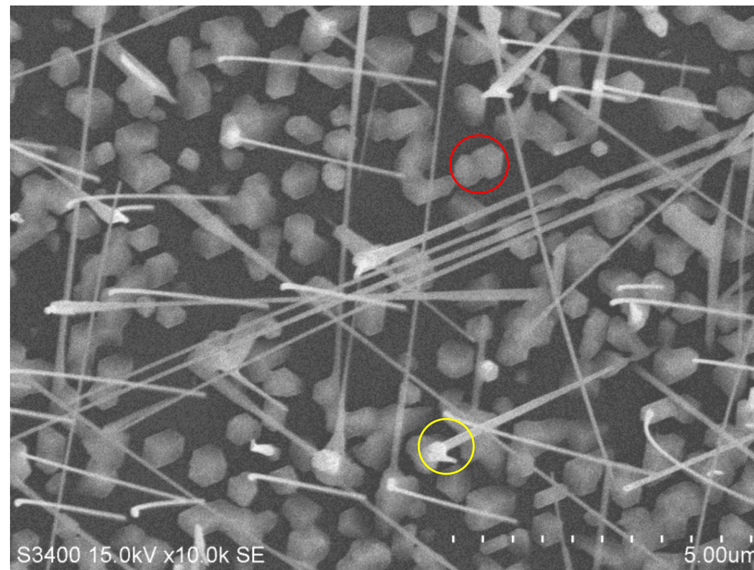


Fig. 2.7 SEM images of GaAs nanowires grown on Si(111) substrate, parasitic growth is highlighted with ○ and non-directional growth of nanowire is highlighted with ○

2.3.4 Self-catalyzed VLS growth of GaAs nanowires without SiO_2

All concerned issues mentioned in the previous sections occur inherently in the process which makes them really difficult to be eliminated. Our previous works in self-catalyzed GaAs nanowire growth on Si(111) covered with SiO_2 substrates also suffer with identical problems[1]. Hence we decided to propose a new idea to grow self-catalyzed GaAs nanowires directly on GaAs substrates. By this method, the problem of unintentional Au incorporation can be completely avoided as well as issues related to SiO_2 layer such as tilted nanowires and parasitic growth.

Since this was the first time that growth of self-catalyzed GaAs nanowires was performed on bare GaAs substrate, we used our experience in growing self-catalyzed GaAs nanowires on Si as a guideline for this research. The nanowire growth was performed with similar process to the conventional self-catalyzed VLS but with small adjustments. GaAs substrates covered with SiO_2 layer was replaced with bare GaAs substrates. After seed particles were created by deposition of Ga droplets, the substrates were then exposed to Ga and As to perform the growth with an identical process to the conventional self-catalyzed VLS. The Ga beam pressure and subtrate

temperature were varied as growth parameters to achieve intended results. Diagram of the growth process is displayed in Fig. 2.8

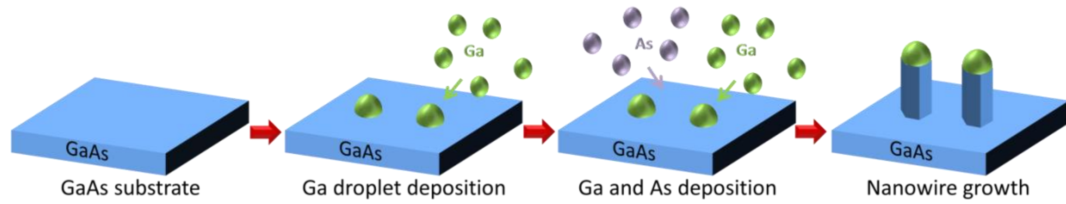


Fig. 2.8 Diagram of GaAs nanowires growth by self-catalyzed VLS without SiO_2

จุฬาลงกรณ์มหาวิทยาลัย
CHULALONGKORN UNIVERSITY

Chapter 3
Experimental procedure

This chapter explains the basics of all techniques and equipment related with the experiments. All samples were fabricated using Molecular Beam Epitaxy (MBE) while being in-situ characterized by Reflection High-Energy Electron Diffraction (RHEED). Scanning Electron Microscope (SEM) was utilized to investigate the surface morphology of samples as well as X-Ray Diffraction (XRD) for crystal structure analysis. All data were collected and will be analyzed extensively in the following chapters.

3.1 Molecular Beam Epitaxy (MBE)

Molecular Beam Epitaxy is one of the most well-known crystal deposition or also known as epitaxial growth technique. What makes MBE different from other epitaxial growth such as Liquid Phase Epitaxy (LPE) or Vapor Phase Epitaxy (VPE) is the use of molecular beam which is generated by sublimation or evaporation with heating of effusion cells to deposit epitaxial materials on substrates. The MBE system requires ultra-high vacuum condition to occur as it increases deposition rate due to longer mean free path of epitaxial atoms from molecular beam[25] and clean ambient in the growth process. The molecular beam epitaxy system in this thesis is shown in Fig.3.1.

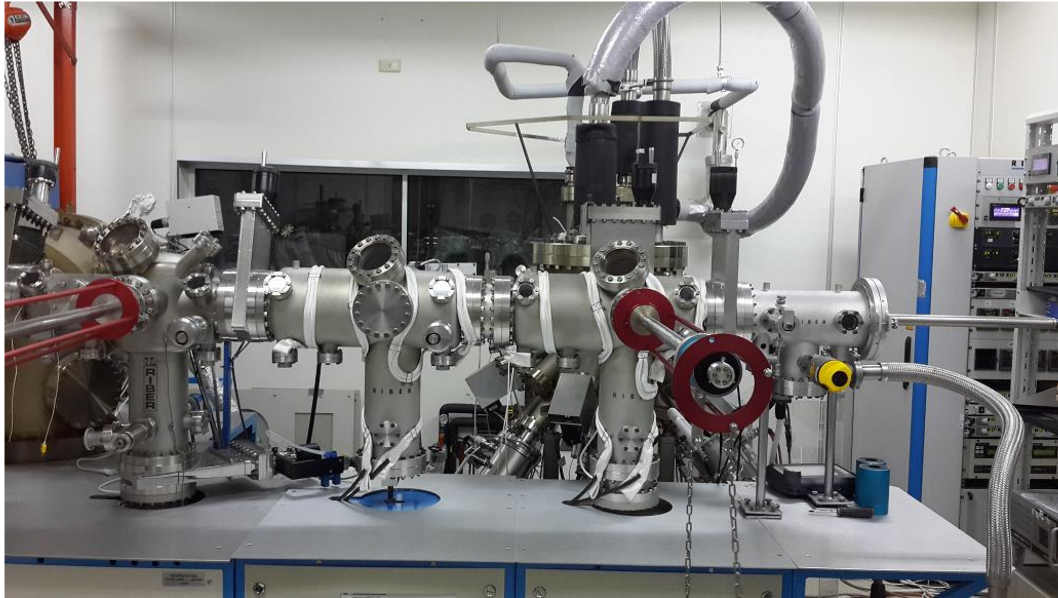


Fig. 3.1 COMPACT-21 MBE system at Semiconductor Development Research Laboratory, Chulalongkorn University

จุฬาลงกรณ์มหาวิทยาลัย
Chulalongkorn University

As shown in schematic diagram in Fig. 3.2, the MBE growth process performs in ultra-high vacuum chamber which has a background pressure around 10^{-9} to 10^{-10} Torr or lower, this chamber is usually cooled by liquid N_2 to adsorb or tap impurities[25] and reduce the heat from effusion cells. A sample or substrate is placed in holder which is able to rotate to provide more uniform epitaxial layer. Molecular beams are produced by heating effusion cells which are on the opposite side of sample holder. Integral shutters at the front of effusion cells are used to switch on and off the beams. In some MBE systems, the effusion cells are integrated with valves cracker source(s) which enable users to precisely control molecular beam fluxes by changing positions of the valves. Beam fluxes, which represent concentration of molecular beam, are measured by pressure gauges. In-situ characterization devices such as Reflection High-Energy Electron Diffraction (RHEED) can be installed into MBE system for real-time monitoring during the growth process, this will be elaborated in detail in the next section.

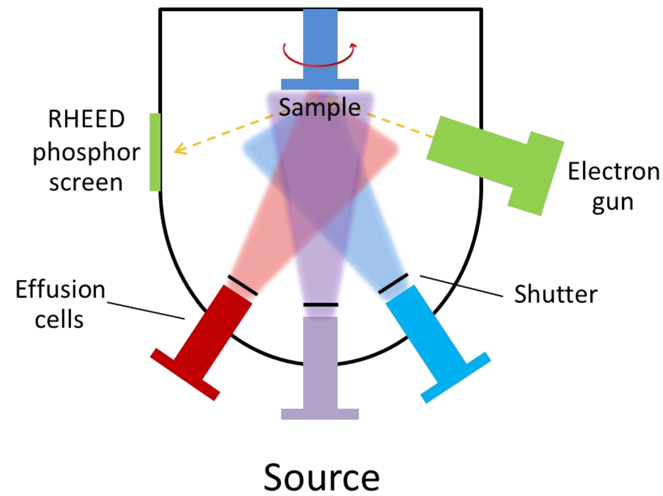


Fig. 3.2 Schematic diagram of MBE growth chamber

3.2 Reflection High-Energy Electron Diffraction (RHEED)

Reflection High-Energy Electron Diffraction is a technique to characterize surface of sample by acquiring information from diffraction of reflected electron beams. A RHEED system consists of electron gun to produce electron beam, phosphor screen to display diffraction pattern from reflected beams, moreover as electron gun only works under high vacuum or Ultra-High Vacuum (UHV) is required for this system.

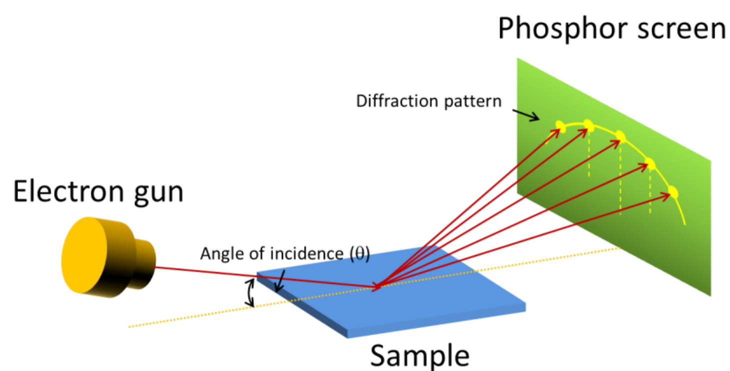


Fig. 3.3 Schematic diagram of RHEED system

RHEED system operates by striking electron beam on sample surface with lowest possible angle of incidence (θ) at around 0.1-5° to prevent electron beam from penetrating into sample[26]. Reflected beams interfere each other and create diffraction pattern displayed on phosphor screen as seen in Fig. 3.3. By observing RHEED patterns and intensity, it is possible to study growth rate, surface structure, growth mode, as well as lattice constant of sample in real-time during the fabrication process[27]. The RHEED is also used to monitor the substrate temperature via the temperature dependent of RHEED pattern[28].

3.3 Scanning Electron Microscope (SEM)

Scanning electron microscope is a microscope that uses focused beam of electron to generate images instead of light in optical microscope. SEM was first developed in late 1930s to overcome the limitation of optical microscope. Under visible light, resolution of conventional optical microscope is around 100 nm[29] which make it unsuitable for nanostructure characterization. By replacing light with electron beam, resolution can go down to the order of 10 Å[29]. The basic setup of SEM is displayed in Fig. 3.3

จุฬาลงกรณ์มหาวิทยาลัย
CHULALONGKORN UNIVERSITY

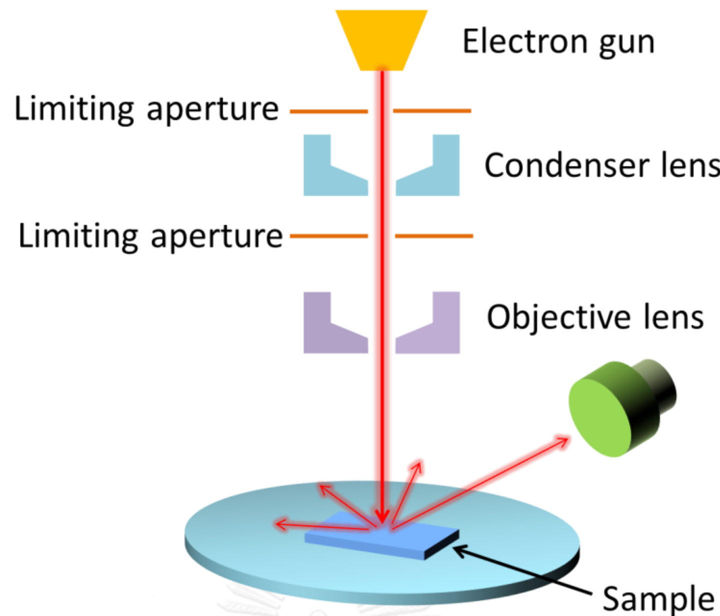


Fig. 3.3 Diagram of SEM operation

First, electrons are accelerated and emitted as a beam from electron gun. Electron beam moves past limiting aperture and is converged by condenser lens. After that the beam is focused by objective lens onto sample. The electron beam that reaches sample will scatter and produce reflected electrons which can be detected by electron detector. Data from reflected electrons are collected and used to generate SEM images.

Some SEMs are also equipped with Energy-dispersive X-ray spectroscopy (EDX) which can be used to analyze elemental composition of materials by detecting the emission of X-ray from stimulated electrons.

3.4 X-Ray Diffraction (XRD) analysis

XRD is a technique to investigate crystal structure of materials by detecting diffraction of reflecting X-ray. Due to the fact that when exposing X-ray on atoms, electrons orbiting around nucleus will cause the beam to scatter by the effect of

absorption and radiation[30], for crystal structure which consists of ordered and periodically aligned atoms, the incident beam will scatter in certain direction which can be detected and used for lattice spacing calculation which follows Bragg's law (see Fig. 3.5)

$$2d\sin\theta = n\lambda \qquad (3.1)$$

where d = lattice constant or lattice spacing

θ = angle of incidence

and λ = wavelength of X-ray

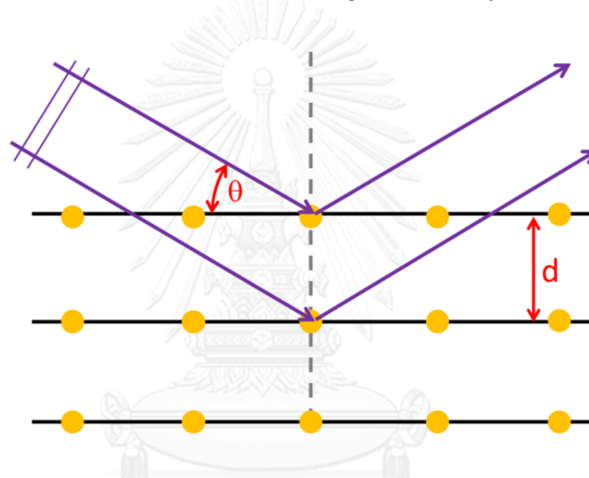


Fig. 3.4 Diagram of Bragg diffraction shows X-ray beam scattered by atoms in crystal structure that has lattice constant of d at angle of incidence of θ

In the measurement process, the sample is mounted on a sample holder which is exposed to X-ray from X-ray source at certain angle of incidence (θ) (see Fig. 3.5). After the X-ray beam reaching sample, it will be reflected and scattered, this signal can be detected by X-ray detector. After that the holder and the detector are rotated to test the sample while varying angles of incidence. Data from X-ray detector will be collected and plotted into a graph. "Peaks" in the plotted graph represent strong signal at specific angle which can be used to calculate the lattice constant as previously mentioned. Data from XRD can be used to analyze or evaluate crystal structure of the sample and lattice parameters.

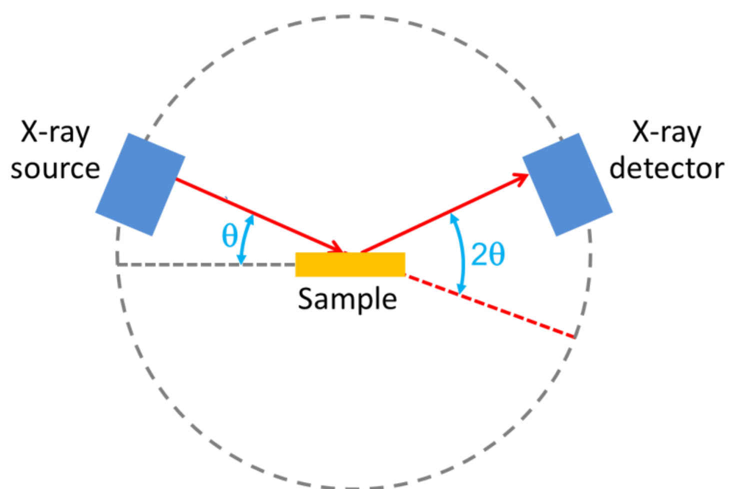


Fig. 3.5 Diagram of XRD measurement process

จุฬาลงกรณ์มหาวิทยาลัย
Chulalongkorn University

Chapter 4
Effect of Ga flux on self-catalyzed GaAs nanowires without SiO_2

Since this was the first time that GaAs nanowire growth was performed directly on GaAs (111)B substrates by MBE using self-catalyzed VLS process and Ga droplets as seed particles, it was necessary to find proper the growth conditions before continuing the next experiment. Due to the fact that we have experience with growing GaAs nanowires on Si (111) substrates, we used process details and experimental data from our previous work[1] as a guideline for this experiment. The growth process was similar to conventional self-catalyzed VLS except the bare GaAs (111)B were used as substrates instead of Si (111). Data of controlled parameters were derived from the previous works while Ga flux was varied as a growth parameter to find an optimal condition to obtain nanowires. Finally, the nanowire samples were characterized by SEM and XRD for the study of surface morphology and crystal structure respectively.

4.1 Experimental detail

In this experiment, the nanowire growth was performed on n-type (Si-doped) GaAs (111)B substrates by Molecular Beam Epitaxy (MBE) using COMPACT-21 system. All substrates were prepared by degassing in a pre-heat chamber at 400ºC for 1 hour without any surface modification and chemical treatment prior to this step. After preparation had finished, the substrates were loaded into growth chamber and the substrate temperature was ramped up to 450°C. To form seed particles on the substrate surface for growth initiation, Ga droplets were deposited on substrates with flux pressure of 1.6×10^{-6} Torr for 40 seconds. The nanowires were grown under As_4 pressure of 8×10^{-6} Torr and the substrate temperature was kept at constant temperature of 450°C. Ga flux as a growth parameter was varied from 4×10^{-7} to 2×10^{-6} Torr. The nanowire growth continued for 30 minutes before the Ga supply was cut off to terminate the growth. Then substrate temperature was ramped down to 240°C

before As_4 supply was cut off. After finishing the growth process, samples were unloaded from the chamber and cut into pieces for characterization.

4.2 Results and discussions

4.2.1 Surface morphology

SEM images with ×10,000 magnification at 45° tilted angle show that no nanowire growth occurred at low Ga flux of 4×10^{-7} Torr, this was probably a result from insufficient Ga supply to maintain the growth. Since GaAs surface has higher sticking coefficient than SiO_2 surface[31], the growth of GaAs nanowires on GaAs substrate probably requires higher Ga flux than on Si-covered GaAs substrate to prevent Ga droplets from crystallization. When Ga flux pressure was increased from 4×10^{-7} to 8×10^{-7} Torr, there were holes occurred all over surface of the substrates. We believe that these are shape of crystallized Ga droplets before getting buried by buffer layer. The nanowires started emerging under Ga flux of 1.2×10^{-6} Torr with vertically alignment along [111] direction. After the Ga flux pressure was increased to 1.6×10^{-6} Torr, nanowires displayed signs of higher radial growth and lower axial growth as seen from larger diameter and shorter length of nanowires. There is no parasitic growth visible on the substrate surfaces since GaAs bulks were already buried and merged with GaAs buffer layer. Under Ga flux of 2.0×10^{-6} Torr, the nanowire growth was heavily suppressed, only few nanowires appear and many large chunks of structures can be observed all across on the substrate.

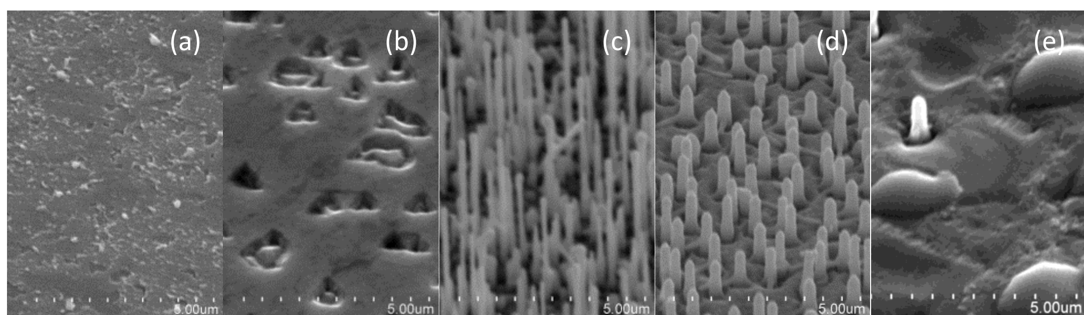


Fig. 4.1 SEM images of GaAs nanowire samples grown under Ga flux of 4×10^{-7}(a), 8×10^{-7}(b), 1.2×10^{-6}(c), 1.6×10^{-6}(d), and 2.0×10^{-6}(e)

4.2.2 Growth rate

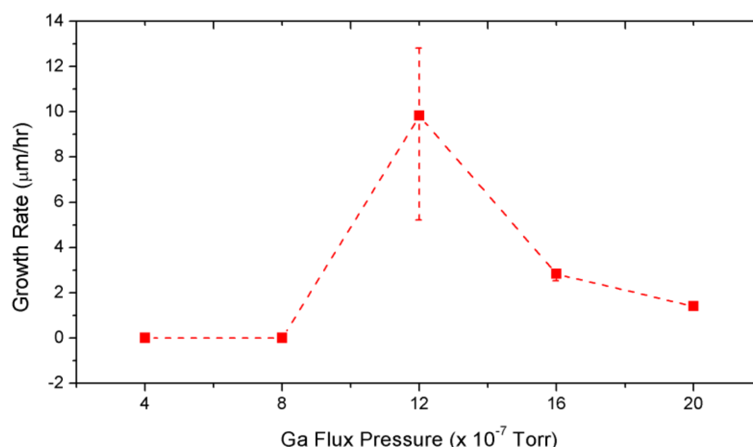


Fig. 4.2 Growth rate with error bars of GaAs nanowires as a function of Ga flux pressure

Nanowires started growing on substrates when Ga flux pressure reached 1.2×10^{-6} Torr with an average growth rate of 9.82 μm/hr. The growth rate of nanowires at this pressure deviates from 5.19 to 12.82 μm/hr as represented by an error bar in Fig. 4.2.

When increasing Ga flux from 1.2×10^{-6} Torr to 1.6×10^{-6} Torr, the average growth rate of nanowires drops down to 2.83 μm/hr with nearly no deviation. We suspect that the reduction in the growth rate is probably due to the excessive deposited Ga atoms that prevent the droplets from reaching saturation. As discussed in the previous chapter, self-catalyzed nanowires formed by precipitation of atoms after seed droplets became saturated however under high Ga flux pressure, composition of droplets is heavily Ga-dominated thus slower crystallization rate due to insufficiency of As atoms and decrease in growth rate as a result. Moreover there is a strong indication of higher radial or lateral growth as seen from increasing diameters of nanowires grown under Ga flux pressure of 1.6×10^{-6} Torr. Since at higher pressure, Ga atoms have to travel under denser atmosphere, all of them have higher probability to collide with each other. This contributes to the accumulation of Ga atoms at nanowire sidewalls as displayed in Fig. 4.3, the accumulated Ga atoms will later be

crystallized and cause the radius of nanowire to grow which also known as radial growth.

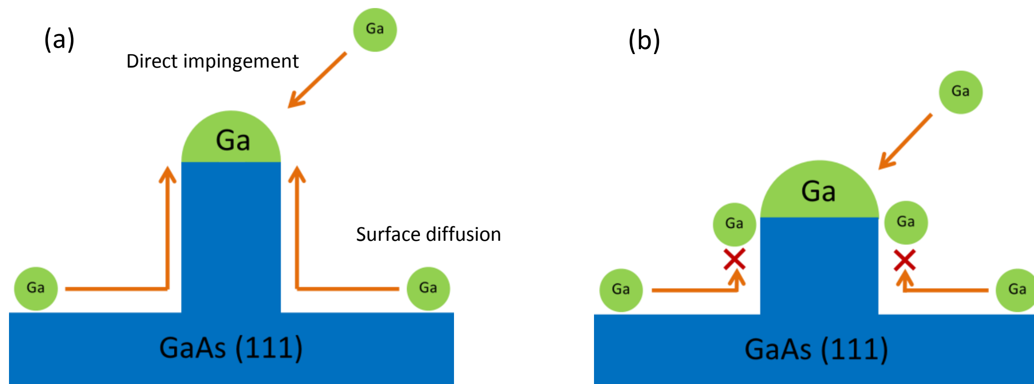


Fig. 4.3 Growth model of GaAs nanowire (a) blocking of Ga atoms at nanowire sidewalls causes decrease in growth rate and radial growth (b)

Nanowire growth rate drops even further after increasing Ga flux to 2.0×10^{-6} Torr. This is probably a result from higher atom collision rate under high pressure as well.

4.2.3 Nanowire density

Nanowire density is determined by density of initial droplets[32] which are deposited on substrates to create seed particles at the beginning of growth process. As seen in Fig. 4.4, density of nanowires at Ga flux of 1.2×10^{-6} and 1.6×10^{-6} Torr is quite similar at 1.71 and 1.80 nanowires per μm^2 respectively despite having significant difference in the growth rate. This can be explained by nucleation theory[33]. Since the Ga droplet density strongly depends on Ga flux and substrate temperature[34] and we created seed particles on sample surface by depositing Ga at the same flux pressure and substrate temperature, the nanowires grew with similar density as a consequence.

จุฬาลงกรณ์มหาวิทยาลัย
Chulalongkorn University

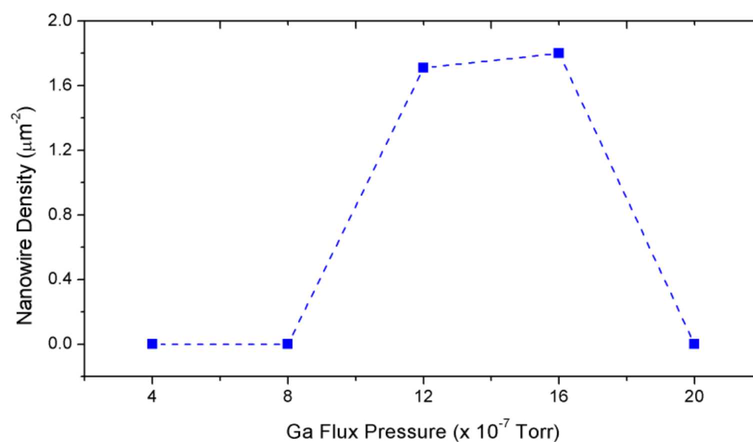


Fig. 4.4 Density of GaAs nanowires as a function of Ga flux pressure

4.2.4 Elemental composition

EDX data show that the samples grown under Ga flux of 4×10^{-7} to 1.6×10^{-6} Torr are consisted of Ga and As at ratio of 1.05 to 1.14 which is almost stoichiometry. At Ga flux of 2.0×10^{-6} Torr, Ga/As ratio tremendously increases to 1.95, this suggests that the large structures spreading all across the substrate surface are Ga chunks.

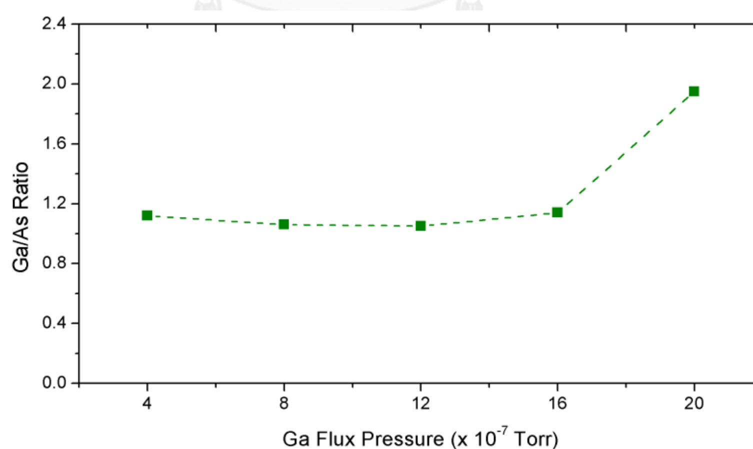


Fig. 4.5 Ga/As ratio of GaAs nanowires as a function of Ga flux pressure

4.2.5 Vertical yield

For better evaluation of nanowire quality, we introduced "vertical yield" which is a percentage of nanowires that grow vertically on samples as given by

$$\text{Vertical yield} = (\%) = \frac{\text{Number of vertical nanowires}}{\text{Number of all nanowires on samples}} \quad (4.1)$$

Higher vertical yield means more proportion of the vertical nanowires to all nanowires can be obtained on sample which makes it appropriate for optical device like solar cell[9]. As seen from Fig. 4.6 almost all nanowires grew vertically along [111] direction, the vertical yield is outstanding at nearly 100%. Normally nanowires preferentially grow on [111] direction to minimize the surface free energy[35], however in some cases such as VLS growth of nanowires on (111) substrate surface covered with SiO_2, there is a probability of tilted or non-directional growth nanowires occurring due to non-uniformity oxide layer[24] which can bring down the overall vertical yield. Results from this experiment show that this issue can be mostly avoided in our process since our process involves preforming nanowire growth directly on the substrates without oxide layer.

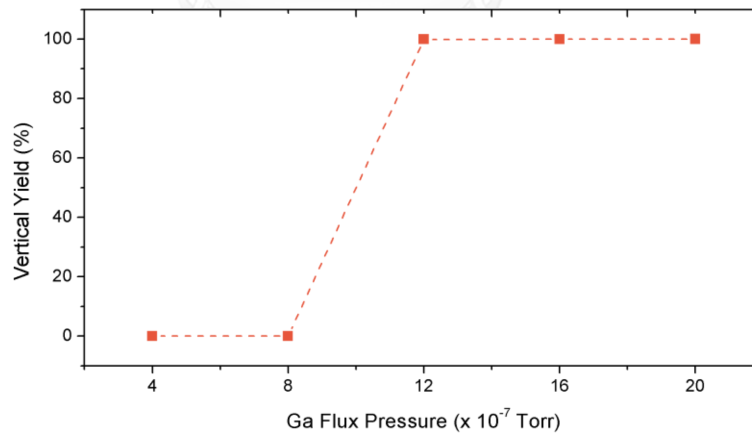
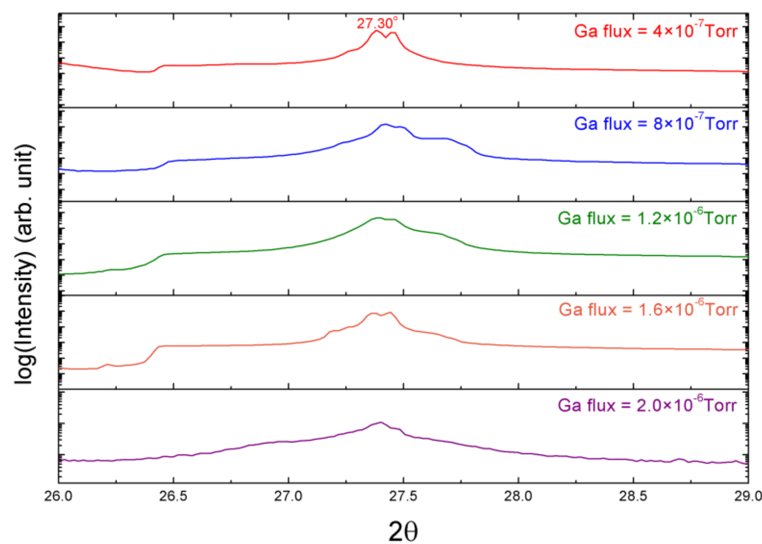


Fig. 4.6 Vertical yield of GaAs nanowires as a function of Ga flux pressure

4.2.6 Crystal structure

As seen from XRD graph in Fig. 4.7, the highest peak occurs at 27.30° which corresponds with Zincblend (ZB) GaAs(111) structure[10]. This peak is probably a shared structure of GaAs (111)B substrate, GaAs buffer layer, and GaAs nanowires. The shoulder of ZB GaAs peak at 26.50° to 27.00° may correspond to Wurtzite (WZ) GaAs as these 2 structures have very close lattice constant. Data from XRD and EDX suggest that our nanowire samples are consisted of mixed structure of ZB and WZ GaAs.



จุฬาลงกรณ์มหาวิทยาลัย
CHULALONGKORN UNIVERSITY

Fig. 4.7 XRD scans of samples that fabricated under varied growth temperature

4.3 Summary

GaAs nanowires were successfully grown on GaAs (111)B substrates using VLS technique without utilization of SiO_2 cover layer. Due to the absence of SiO_2 layer, the stickiness of GaAs substrates could be overcome by increasing Ga flux. No parasitic growth was found on the substrates since all GaAs bulks were buried by buffer layer. Very few non-directional growth of nanowires were found on samples which matched our expectation as the growth was performed directly on GaAs (111)B substrates, the problems of non-uniformity of SiO_2 covered-layer could be avoided. This results in excellent vertical yield of almost 100%.

Dependence of growth rate and density of nanowires on Ga flux followed the same trends as the conventional VLS on SiO_2. Increasing Ga flux caused nanowires to increase in the radial growth but decrease in the axial growth. Nanowire density for samples that grown under different Ga flux was rather identical as it was pre-determined by the density of initial seed particles which was created at the beginning of growth process at the same temperature and flux pressure.

Crystal structure of our nanowires was different from nanowires that grown on SiO_2 since they were mixed structures of ZB and WZ GaAs as opposed to conventional self-catalyzed GaAs nanowires which are dominated by ZB structure. This result is very interesting and will be discussed in the following chapters.

Chapter 5

Effect of growth temperature on self-catalyzed GaAs nanowires without SiO_2

This chapter focuses on the effect of substrate temperature on the growth of GaAs nanowires. To study this effect, the GaAs nanowire growth was performed under identical conditions except the substrate temperature which was varied as a growth parameter. We decided to choose GaAs nanowire sample that grown under Ga flux of 1.6×10^{-6} Torr from the previous chapter as a reference sample as it provided nanowires with the most size and shape uniformity, other samples were performed under different Ga flux pressure as mentioned. Results from SEM and XRD were also investigated and discussed.

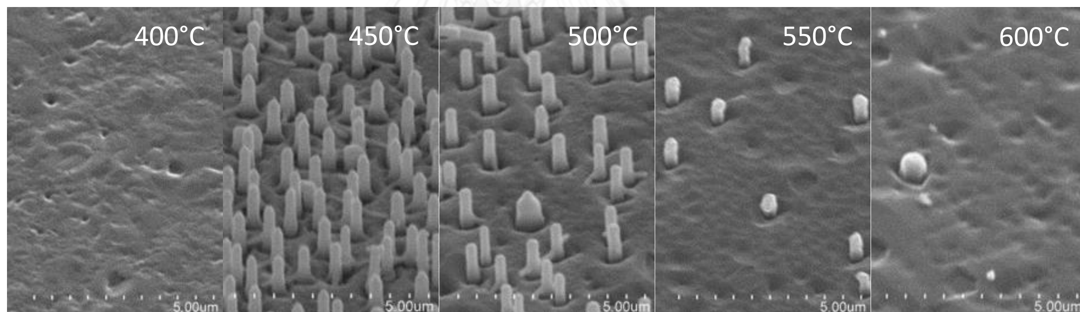
5.1 Experimental detail

In this experiment, the nanowire growth was performed on n-type (Si-doped) GaAs (111)B substrates by Molecular Beam Epitaxy (MBE) using COMPACT-21 system. All substrates were prepared by degassing in a pre-heat chamber at 400ºC for 1 hour without any surface modification and chemical treatment prior to this step. After preparation had finished, the substrates were loaded into growth chamber and the substrate temperature was ramped up to 450°C. To form seed particles on the substrate surface for growth initiation, Ga droplets were deposited on substrates with flux pressure of 1.6×10^{-6} Torr for 40 seconds. The nanowires were grown under constant Ga and As flux pressure of 1.6×10^{-6} Torr and 8×10^{-6} Torr respectively. This time substrate temperature was varied from 400 to 600°C as a growth parameter with an incremental of 50°C. Nanowire growth continued for 30 minutes before Ga supply was cut off to terminate the growth. Then substrate temperature was ramped down to 240°C before As supply was cut off. After finishing the growth process, samples were unloaded from the chamber and cut into pieces for characterization.

5.2 Results and discussions

5.2.1 Surface morphology

As seen from SEM images ×10,000 magnification at 45° tilted in Fig. 5.1, there is no nanowire existing on samples grown at 400°C, this was probably due to insufficient chemical potential difference between adatoms in solid, liquid, and vapor phase at low temperature[35]. Nanowires started growing at 450°C which is our reference sample. No parasitic growth and non-directional growth of nanowires were observed since the growth was performed directly on GaAs substrates as explained in the last chapter. Density of nanowires seems to decrease at higher growth temperature, this will be discussed in the next section. Shape and diameter of nanowires appear to be similar for all substrates. The nanowire growth was greatly suppressed at growth temperature of 600°C, this was probably a result from insufficient chemical potential difference as well.



CHULALONGKORN UNIVERSITY

Fig. 5.1 SEM images of nanowire samples grown at

varied temperature from 400°C to 600°C.

5.2.2 Growth rate

Growth rate as a function of growth temperature in Fig. 5.2 shows that nanowire growth rate increases with growth temperature and reaches the maximum of 2.97 µm/hr at 500°C before slightly decline at higher temperature. Normally growth rate of nanowires depends on the diffusion length of incoming adatoms, this relationship can be explained by Fröberg's growth model[36] as shown in following equation

$$R_{axial} = R_{dep}\lambda_s[1-\gamma(r_w)]\frac{2\Omega_{GaAs}K_1\left(\frac{r_w}{\lambda_s}\right)}{r_w K_{01}\left(\frac{r_w}{\lambda_s}\right)} + R_{dep}\Omega_{GaAs} \quad (5.1)$$

where R_{axial} is the growth rate of nanowires along axial direction

R_{dep} is the deposition rate of incoming adatoms on surface of substrate

λ_s is diffusion length of Ga

Ω_{GaAs} is the atomic volume of ZB GaAs which is equal to 0.0451 nm3

$\gamma(r_w)$ is the dimensionless parameter

and K_1 and K_0 are zero and first order modified Bessel function

According to the equation 5.1, nanowire axial growth rate (R_{axial}) is directly proportional to diffusion length (λ_s) of adatoms. Giang et al. also found that diffusion length usually went up with increasing the growth temperature due to higher kinetic energy of adatoms[34]. Hence an increase in the growth rate from the temperature of 400°C to 500°C is likely to be a result from raising growth rate. However, the growth rate of our nanowires seems to be saturated at growth temperature between 500°C to 600°C, this can be explained by the fact that our nanowire growth was performed under unusually high Ga flux rate at 1.6×10^{-6} Torr, almost 10 times higher than conventional VLS[37], to overcome the stickiness of bare GaAs substrates, a large number of adatoms presenting in high flux pressure can obstruct each other[34], outweigh the effect of growth temperature, and cause the overall growth rate to slightly decline and begin to stabilize.

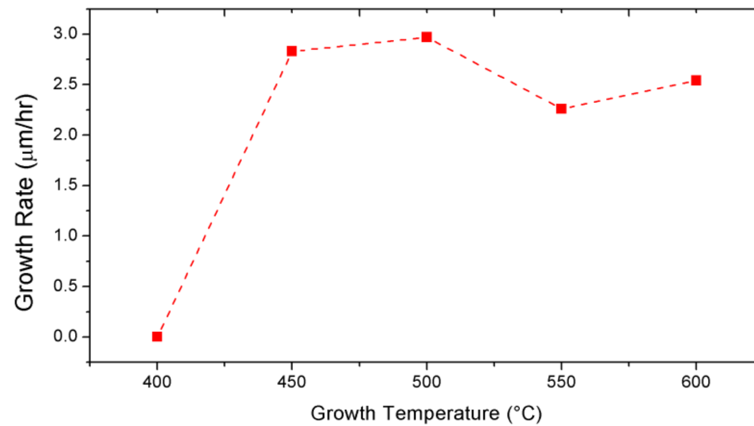


Fig. 5.2 Graph of growth rate of nanowires as a function of growth temperature

5.2.3 Nanowire density

As shown in Fig. 5.3, nanowire density reaches the highest point of 1.8 μm^{-2} at growth temperature of 450°C and starts to decline with increasing growth temperature. This agrees with a normal relation of nanowire density and substrate temperature[32]. As discussed in the previous chapter, under VLS mechanism, nanowire density is determined by density of droplets which acts as seed particles. Since droplet density is inversely proportional to the substrate temperature, raising the temperature causes Ga droplets on substrate to diffuse and gather together to form larger droplets which results in reduction of droplet density hence nanowire density to drop down. However final nanowire diameter does not seem to grow up with the increase of initial droplet size as it supposed to be. This was probably a result from radial growth of nanowires. As discussed in last chapter, our nanowire growth process was performed at high Ga flux pressure, 1.6×10^{-6} Torr which was more than an order of magnitude higher than the growth GaAs nanowires by conventional VLS growth on SiO_2 covered substrate [22]. High Ga flux induced radial growth[38] which could outweigh the effect from larger initial droplets on nanowire diameter.

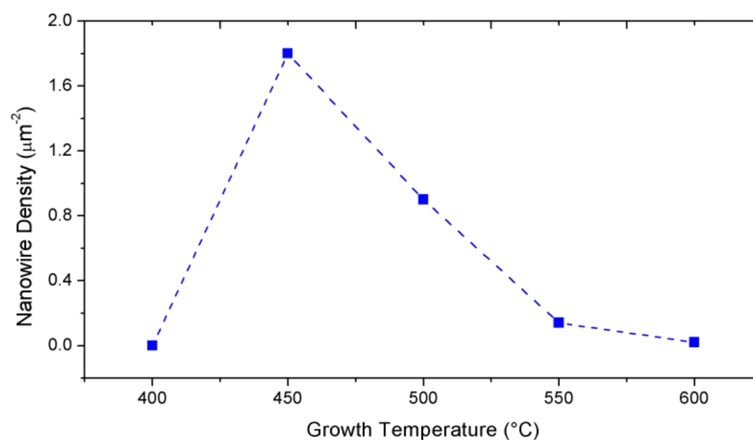


Fig. 5.3 Graph of nanowire density as a function of growth temperature

5.2.4 Elemental composition

Elemental composition data taken from EDX show that Ga/As ratio of nanowire samples are in the range of 1.04 to 1.14 as seen in Fig. 5.4. Growth temperature has barely effect on the elemental composition of nanowires.

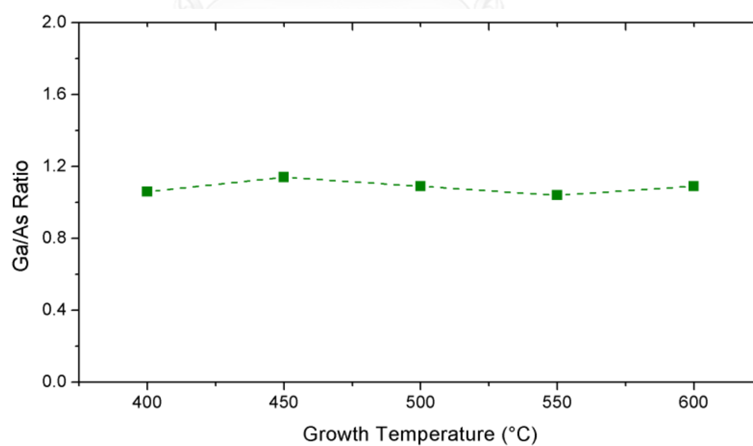


Fig. 5.4 Graph of Ga/As ratio of nanowires as a function of growth temperature

5.2.5 Vertical yield

Vertical yield follows the same trend as in the previous chapter, almost all nanowires grew straight up with excellent vertical yield approaching 100% as displayed in Fig. 5.5. Since all growth was performed on exactly same type of substrates, similar results can be expected.

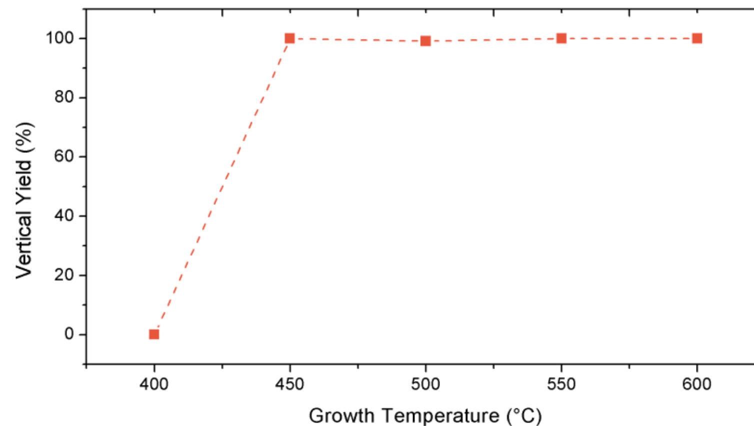


Fig. 5.5 Graph of vertical yield of nanowires as a function of growth temperature

5.2.6 Crystal structure

XRD graph in Fig. 5.6 displays the highest peaks occur at 27.30°, this peak matches ZB GaAs structure[10] which is supposed to be a mixed structure of GaAs (111)B substrate, GaAs buffer layer, and GaAs nanowires. The shoulder of ZB GaAs(111) peak at 26.50° to 27.00° may correspond to WZ GaAs as these 2 structures have very close lattice constant. This data along with EDX suggests that our nanowires are consisted of GaAs and may have mixed structure of ZB and WZ.

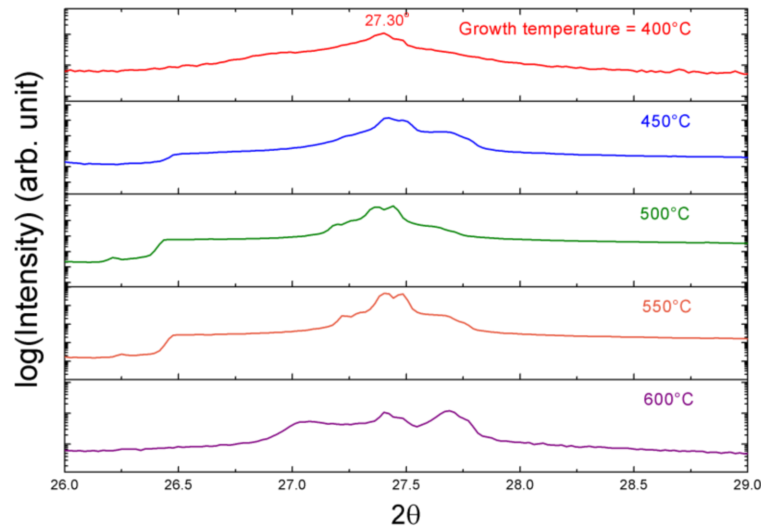


Fig. 5.6 XRD scans of nanowire samples grown at varied temperature

5.3 Summary

With the data from effect of Ga flux pressure and growth temperature, we can see a small growth window of GaAs nanowire on bare GaAs (111)B substrates. A high Ga flux is required in the growth process to overcome the stickiness of GaAs surface which is more than that of SiO_2 layer, however this is a trade-off since the high Ga flux can produce the negative effect to overall growth rate of nanowire as well.

The nanowire density falls down at high temperature as increasing temperature causes small Ga droplets to gather and form larger droplets with lower density. The vertical yield is still outstanding which meets our expectation since every growth were performed on the same bare GaAs (111)B substrates.

XRD result is still astounding as it shows a large portion of WZ GaAs unlike conventional self-catalyzed GaAs nanowires that have ZB dominated structure. In-depth study is necessary in order to explain the causation of different crystal structures.

Chapter 6
Comparison of self-catalyzed GaAs nanowire grown directly on GaAs substrate and on Si substrate with native SiO_2

For better understanding of the difference between nanowire growth by self-catalyzed VLS without SiO_2 layer and conventional self-catalyzed VLS, GaAs nanowire growth were performed on both GaAs (111)B and Si (111) substrates. Sample grown on GaAs (111)B represents our growth process while the growth performed on untreated Si (111) which usually has an ultrathin layer of native SiO_2 remaining on the surface represents conventional self-catalyzed VLS. Nanowires were grown on both substrates with the exactly same growth parameters including Ga and As flux, growth temperature, and growth time. In-situ RHEED characterization was utilized in addition to SEM and XRD for more in-depth knowledge during the growth process. Results from characterization of both samples were analyzed and compared.

6.1 Experimental detail

In this experiment, the nanowire growth was performed on n-type (Si-doped) GaAs (111)B substrates by Molecular Beam Epitaxy (MBE) using COMPACT-21 system. All substrates were prepared by degassing in a pre-heat chamber at 400ºC for 1 hour without any surface modification and chemical treatment prior to this step. After preparation had finished, the substrates were loaded into growth chamber and the substrate temperature was ramped up to 450°C. To form seed particles on the substrate surface for growth initiation, Ga droplets were deposited on substrates with flux pressure of 1.6×10^{-6} Torr for 40 seconds. The nanowires were grown under constant Ga and As flux pressure of 1.6×10^{-6} Torr and 8×10^{-6} Torr respectively. During the growth process, surface morphology of substrates were investigated by Reflection high-energy electron diffraction (RHEED) patterns observation. Nanowire growth continued for 30 minutes before Ga supply was cut off to terminate the growth. Then substrate temperature was ramped down to 240°C before As supply was

cut off. After finishing the process, samples were unloaded from the chamber and cut into pieces for characterization.

6.2 Results and discussions

6.2.1 Surface morphology

There is a huge difference between nanowires grown on GaAs (111) and on Si (111) substrates as shown in SEM images ×10,000 magnification at 45° tilted in Fig. 6.1. On GaAs (111)B, the majority of nanowires grew perpendicular to the substrate along [111] direction with only few tilted, no parasitic growth or bulk structure exists on the substrate while on Si (111) substrate, non-directional growth of nanowires and parasitic growth are clearly visible.

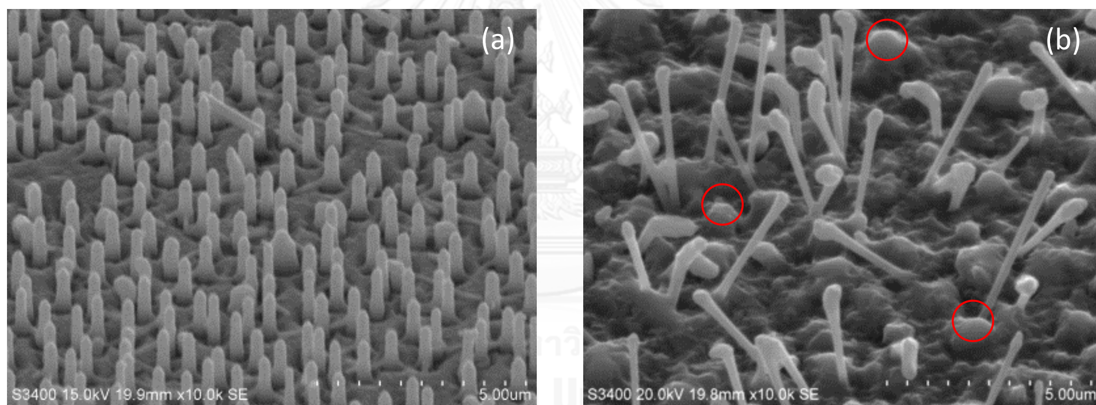


Fig. 6.1 SEM images of GaAs nanowires grown on GaAs (111) substrate (a) and Si (111) substrate (b) parasitic growths are hilighted with ○

6.2.2 Growth rate, density, vertical yield, and elemental composition

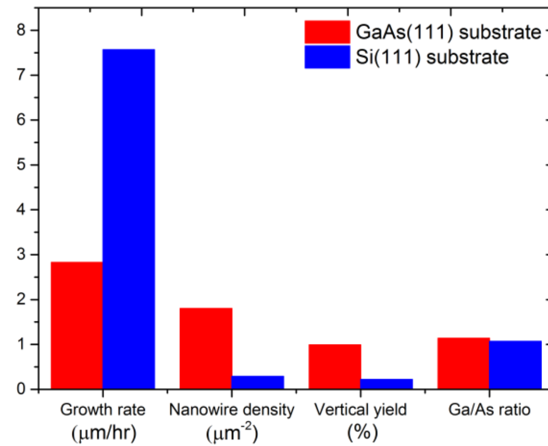


Fig. 6.2 Chart of growth rate, density, vertical yield, and Ga/As ratio of nanowires grown on GaAs (111) substrate compared to grown on Si (111) substrates

As clearly seen in SEM images Fig. 6.1, nanowires grown on Si (111) are noticeably longer than on GaAs (111)B substrate. The growth rate of nanowires, according to Fig. 6.2, measures 7.53 μm/hr on Si (111) which is almost 3 times higher than 2.83 μm/hr of nanowires on GaAs (111)B. Lower sticking coefficient of Ga on Si substrate that covered with native SiO_2 than on bare GaAs is likely to be the cause of this incident since Ga atoms have higher diffusion length and higher tendency to reach seed particles to incorporate the growth on Si than on GaAs substrate[31].

Nanowires grew on GaAs (111)B substrate with much superior in density at 1.8 $(\mu m)^{-2}$ compared to 0.29 $(\mu m)^{-2}$ on Si (111). As previously discussed in chapter 4 and 5, density of nanowires grown by VLS is determined by density of initial droplets which act as seed particles, however this explanation is slightly different on Si (111) substrate as the nanowire growth on SiO_2 need to nucleate from pinholes.

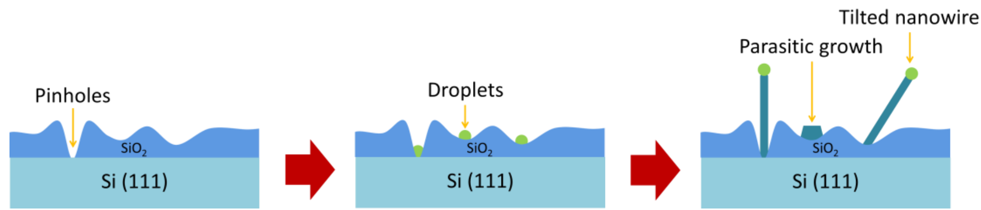


Fig. 6.3 Diagram of self-catalyzed VLS nanowire nucleation on Si (111) substrate covered with native SiO_2 layer

As seen in diagram in Fig. 6.3, Ga droplets need to reach the pinholes in order to form vertical nanowires. However, since our substrate is covered with native SiO_2 layer, non-uniformity of thickness and roughness of native oxide can affect the presence of pinholes and cause some droplets unable to nucleate properly inside the pinholes[24]. Droplets that unable to reach pinholes and nucleate at the wrong sites will result in parasitic growth and non-directional or tilted nanowires. This means in addition to density of initial droplets, the overall nanowire density on Si (111) is also determined by morphology of SiO_2 layer. In order to obtain nanowires on Si (111) substrate with the highest density possible, native oxide layer has to be precisely tailored to get the optimal roughness and thickness which is a difficult task to achieve[24].

จุฬาลงกรณ์มหาวิทยาลัย
Chulalongkorn University

Moreover the growth rate of nanowires also correlates with the density as each nanowire has to compete for resources which are controlled to be identically for both samples as stated in the experimental detail section. Due to mass conservation, materials from Ga and As sources are divided equally amongst the nanowires, this makes nanowire growth with a lower density has higher chance to grow longer than nanowire growth with a higher density in the same period of time[39]. Result from lower resource competition at lower nanowire density on Si (111) substrate can outweigh the losses from parasitic growth hence the higher overall growth rate.

For vertical yield, as discussed in last paragraph, the non-uniform thickness and roughness of the native SiO_2 layer lead to tilted nanowires and parasitic growth.

Thus, the vertical yield of nanowires grown on GaAs (111)B is considerably higher than on Si (111) substrate.

Ga/As ratio is similar for both substrates at close to 1. This suggests that our nanowires are GaAs nanowires with nearly stoichiometric composition.

6.2.3 Crystal structure

XRD results of nanowires grown on GaAs (111) substrate shows the highest peak at 27.4° which corresponds to ZB GaAs (111) structure as seen in Fig. 6.4. There is shoulder peak at 26.5° to 27.0°, this peak probably represents WZ GaAs as discussed in previous chapter. This implies that nanowires grown on GaAs (111) substrate have mixed structure of ZB and WZ GaAs.

For Si (111) substrate, the main peak at 28.6° is likely to originate from Si (111) substrate. The shoulder peak exists at around the same position as ZB GaAs (111) peak. A slight peak shift and broad FWHM is likely to result from defects in crystal structure. There is no WZ GaAs peak exists for Si (111) substrate.

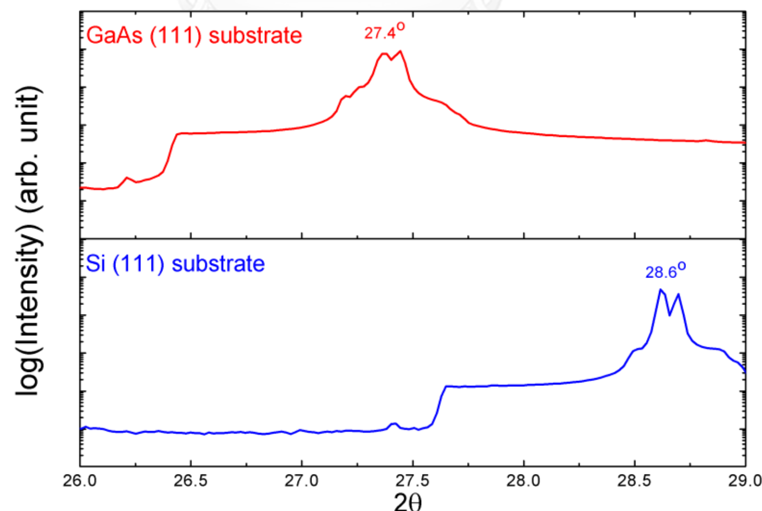


Fig. 6.4 XRD scans of nanowire samples grown on GaAs (111) and Si (111) substrates

6.2.4 RHEED patterns analysis

Observation of in-situ RHEED confirms the results from XRD characterization. Normally RHEED pattern can be used to identify 2-D reciprocal lattice of each structure as shown in Fig. 6.5 (a) for WZ and (b) for ZB structure. According to Fig. 6.6, RHEED pattern along [1-10] azimuth of the nanowire growth on GaAs (111)B substrate has bright bars aligned horizontally as pointed by ↗, this matches diffraction pattern of WZ structure[40] while the pattern of Si (111) sample has bright bars aligned diagonally with ↘ as indicator which corresponds with ZB structure[40], moreover horizontal lines of dim spots on Si (111) pattern also suggests a weak signal from WZ. These results imply that nanowires grown on GaAs (111)B substrate have a strongly WZ dominated structure whereas the nanowires grown on Si (111) have a twinned ZB/WZ with ZB dominant structure.

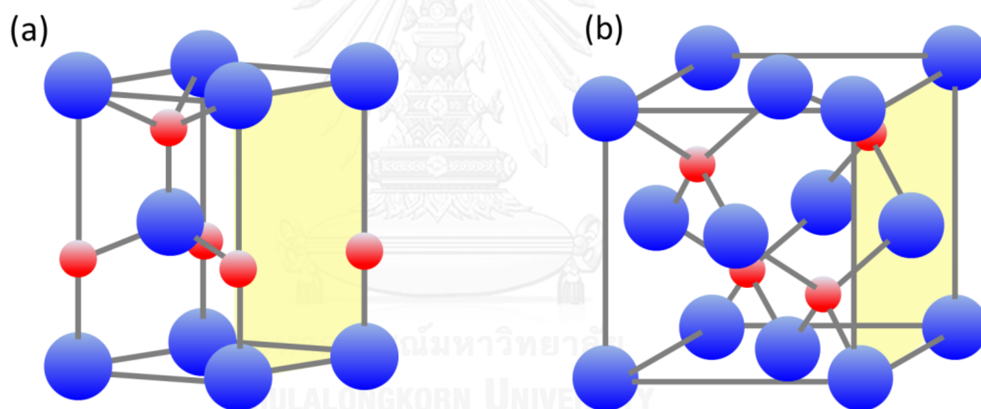


Fig. 6.5 shows hilighted planes of 2-D reciprocal lattice of WZ structure (a)

and ZB structure (b)

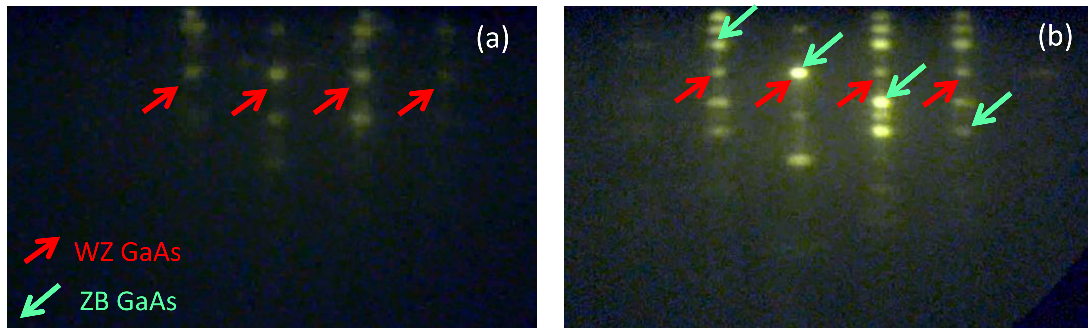


Fig. 6.6 RHEED patterns along [1-10] azimuth of nanowire sample grown on GaAs (111)B (a) and on Si (111) (b)

XRD results along with RHEED pattern analysis are very interesting since GaAs in bulk form and nanowire grown by conventional self-catalyzed VLS normally adopt ZB structure[41] since WZ is a less stable phase. However WZ can be the dominating structure of nanowires under certain circumstance[42].

Crystal structure of nanowires is determined by the crystal phase of nucleus, a small crystallized segment forming at the interface of nanowire and seed droplet. Shortly after formed, the nucleus spreads throughout the whole interface, and nanowire starts growing layer by layer. Nucleus can nucleate in both ZB and WZ phase structure depending on which structure is able to minimize the Gibbs free energy (ΔG) of the system which can be explained by the following equation[43].

$$\Delta G = -Ah\Delta\mu + Ph\gamma_{IL} + A(\gamma_{NL} - \gamma_{SL} + \gamma_{SN}) \quad (6.1)$$

where A is the upper surface area of nucleus

h is the height of nucleus

$\Delta\mu$ is the difference of chemical potential between liquid and solid phase

P is the perimeter length

and γ_{IL}, γ_{NL}, γ_{SL}, and γ_{SN} are the energy per unit area between lateral surface of nucleus-liquid, upper of nucleus-liquid, soild-liquid, and solid-nucleus respectively. All interfaces are shown in Fig. 6.7

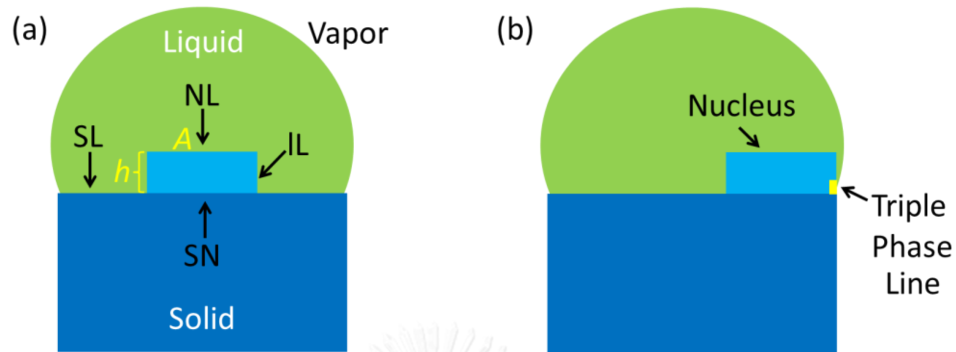


Fig. 6.7 shows all interfaces between upper of nucleus, solid, and liquid (a), and triple phase line (b)

As seen in Fig. 6.7, under the same growth conditions, γ_{IL}, γ_{NL}, and γ_{SL} are identical for both ZB and WZ nucleation since both have the same atomic configuration[43]. On the other hand nucleation of WZ nucleus and ZB GaAs costs energy which equals to γ_{SN} while nucleation of ZB nucleus and ZB GaAs does not, therefore nucleation of GaAs at the middle of droplet usually adopts ZB structure[43]. However if nucleation occurs at the edge of the droplet which causes the lateral surface of nucleus to expose to liquid and vapor surface, this interface is also known as "Triple Phase Line" (TPL), in this case WZ nucleation can be favorable due to the lower interface energies[42].

To understand why our GaAs nanowires grown by self-catalyzed VLS without SiO_2 tend to adopt WZ structure which is different from the conventional self-catalyzed GaAs nanowires that dominated by ZB structure, we need to understand the effect of seed particle shape to nanowire crystal structure. According to the work of Walletin, et al.[44], the shape of liquid seed particle can affect the crystal structure of nanowires due to the changes in contact angle (θ_c). As seen in Fig 6.8 (a), a seed

particle with large contact angle which occurs when depositing a liquid droplet on surface with higher surface energy such as Ga droplets on SiO_2 surface initiates the growth of ZB nanowire since nucleus is unable to occur at TPL since it is fully covered by liquid surface. This result is similar to Munshi's work[45]. However if the surface energy of seed particles is lower than surface energy of substrate which is similar to our case of direct Ga droplet deposition on GaAs substrate, the contact angle of seed particle is small which enables TPL nucleation possible as shown in Fig. 6.8 (b). As seen from SEM images in Fig 6.8 (c), nanowires grown by self-catalyzed VLS without SiO_2 also have small contact angle shaped seed particles at the top, hence the nanowires are likely to adopt WZ structure.

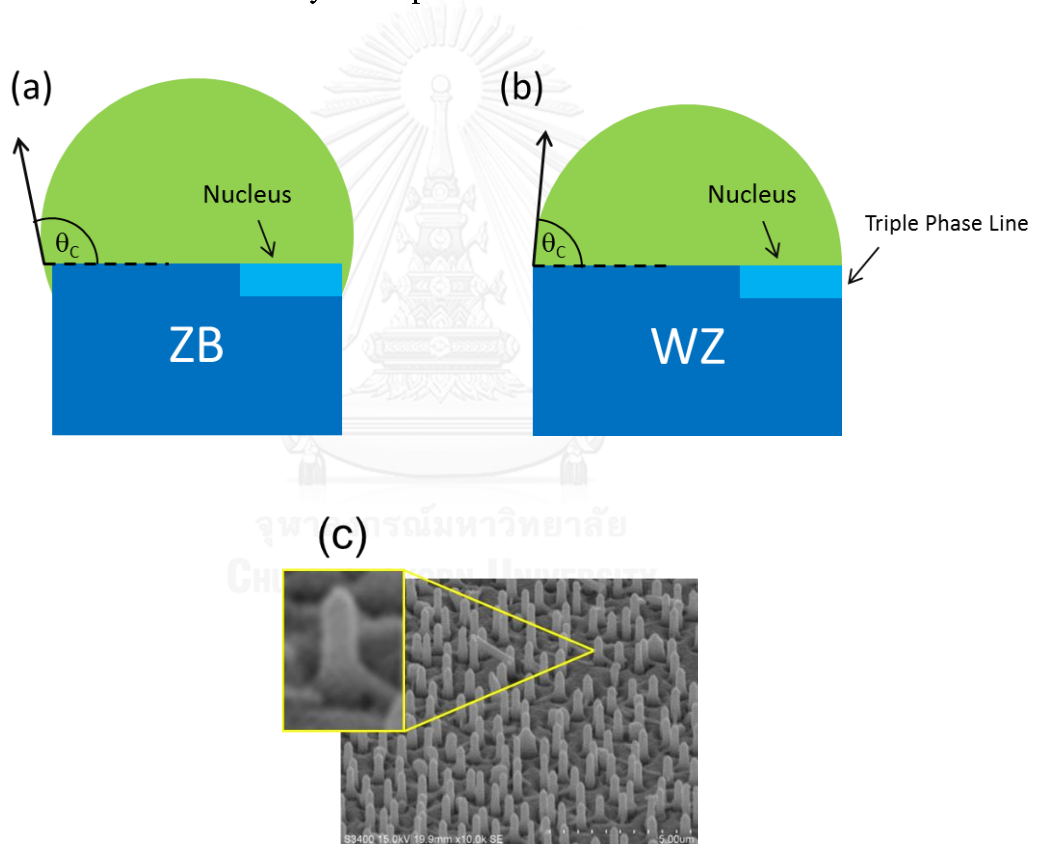


Fig. 6.8 Diagram shows nanowire that adopts ZB structure has a seed particle with large contact angle (θ_c) at the top (a) while nanowire that adopts WZ structure has a seed particle with θ_c which enables nucleation to occur at TPL (b) SEM images shows nanowires grown by self-catalyzed VLS without SiO_2 also possess seed particles with small θ_c (c)

6.3 Summary

Growing GaAs nanowires by self-catalyzed VLS on GaAs (111)B substrate without SiO_2 layer and by conventional VLS on Si covered with native SiO_2 resulted in nanowires with substantial difference in morphology and crystal structure.

Vertical nanowires thrived on GaAs (111)B substrate with rarely tilted or non-directional growth and non-existent parasitic growth however on Si (111), non-directional nanowires grew normally and the parasitic growths are clearly visible. We believe that this is a result from non-uniformity of ultrathin oxide layer on Si (111) surface.

Presence of SiO_2 layer also affects growth rate and density of nanowires. Lower sticking coefficient of SiO_2 boosts the growth rate of nanowire on Si (111) to be higher than on GaAs (111)B, however obtaining nanowires at high density seems to be more difficult on Si (111) than on GaAs (111)B substrate since it involves precise fabrication of the covered oxide layer.

XRD results and RHEED pattern analysis shows that GaAs nanowires grown on GaAs (111)B mainly adopted WZ structure as opposed to crystal structure of nanowires grown on Si (111) which is dominated by ZB. Crystal structure of nanowires strongly depends on the contact angle of seed particles which enables nucleation to occur at the triple phase line or at the middle of droplets.

Chapter 7
Growth mechanism of GaAs nanowires on GaAs (111)B susbtrates without SiO_2 layer

After finishing all the works in previous chapters, we were really interested in growth mechanism of nanowires therefore we designed an experiment to investigate the development of nanowires during the growth process. In this experiment nanowire growth for all samples were performed at identical Ga flux, As flux, as well as substrate temperature while growth time was varied. RHEED was utilized along with SEM characterization to indicate the changes in morphology and crystal structure of nanowires over time. After that we decided to propose a simple growth model using all gathered data. We believe that all of our data and proposition will be benefit for extensive studies of the nanowire growth without the assistance of SiO_2 in the future.

7.1 Experimental detail

In this experiment, the nanowire growth was performed on n-type (Si-doped) GaAs (111)B substrates by Molecular Beam Epitaxy (MBE) using COMPACT-21 system. All substrates were prepared by degassing in a pre-heat chamber at 400ºC for 1 hour without any surface modification and chemical treatment prior to this step. After preparation had finished, the substrates were loaded into growth chamber and the substrate temperature was ramped up to 450°C. To form seed particles on the substrate surface for growth initiation, Ga droplets were deposited on substrates with flux pressure of 1.6×10^{-6} Torr for 40 seconds. The nanowires were grown under constant Ga and As flux pressure of 1.6×10^{-6} Torr and 8×10^{-6} Torr, respectively, at a constant temperature of 450°C. Growth time was set to 10 s, 60 s, 180 s, 600 s, and 1800 s. The evolution of RHEED patterns at different growth time were observed in addition with the change of RHEED intensity throughout the process. After the growth was finished, the substrate temperature was ramped down to 240°C before As

supply was cut off. After finishing the growth process, samples were unloaded from the MBE system and cut into pieces for characterization.

7.2 Results and discussions

7.2.1 Growth evolution

SEM images of all samples were taken with ×10,000 magnification at 45° tilted angle. RHEED pattern along [11-0] azimuth was captured when each growth process was finished. Changes in surface morphology along with RHEED pattern can give an important clue to understand the formation of nanowires.

At growth time (T_{growth}) = 10 s, only small dot structures formed all over substrate surface. RHEED patterns showed streaky pattern with only few spots (arrow) which indicated that the surface was mostly flat as seen in Fig. 7.1.

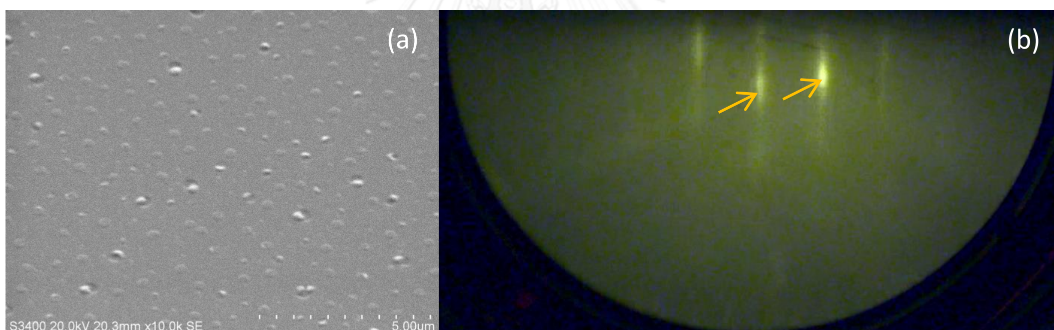


Fig.7.1 SEM images (a) and RHEED pattern (b) of sample at T_{growth} = 10 s

At T_{growth} = 60 s, the dots became larger and there were holes (↗) occurring simultaneously with dots via nano-drilling effect[46]. We believed that these structures were result of imperfect crystallization of Ga droplets or As-unsaturation of Ga droplets. According to many studies on the growth of GaAs quantum ring[47, 48], the Ga droplets deposited on the substrate under low As flux condition [66] will be crystallized and transform to ring-like structures or nanoholes instead of normal quantum dots, this is caused by the migration of Ga atoms from center to vicinity of droplets[49] and soaking process of liquid Ga droplets as shown in Fig. 7.3.

Since our nanowires were grown under unusually high Ga flux, around 1.6×10^{-6} Torr which is more than order of magnitude higher than Ga flux of conventional VLS[50], it is likely that Ga droplets are crystallized under low As pressure ratio hence the final shape of crystallized droplets transform nanohole structures. RHEED pattern completely turned to spotty which corresponded to transition from 2D flat surface to 3D structure.

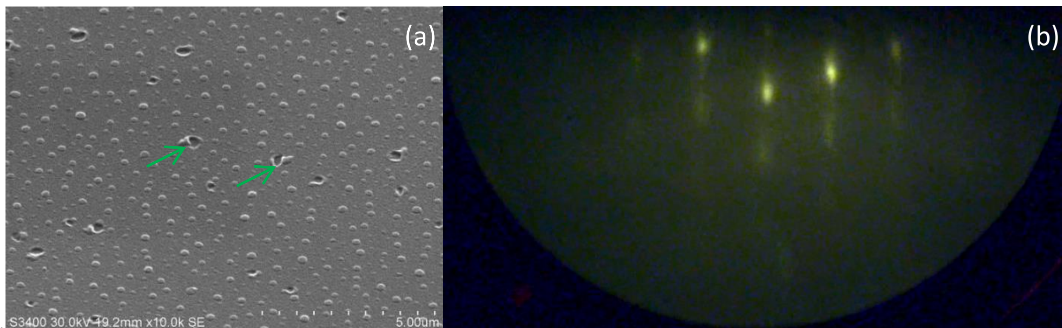


Fig.7.2 SEM images (a) and RHEED pattern (b) of sample at T_{growth} = 60 s

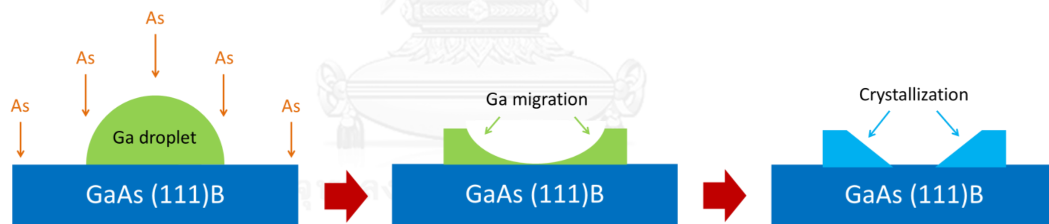


Fig. 7.3 Schematic diagram of how nanoholes form from Ga droplets

At T_{growth} = 180 s, the dots still became larger in size, however its density started dropping down. Shape of hole was much more noticeable. RHEED intensity decreased dramatically which was probably because the substrate surface was under Ga-rich condition[40].

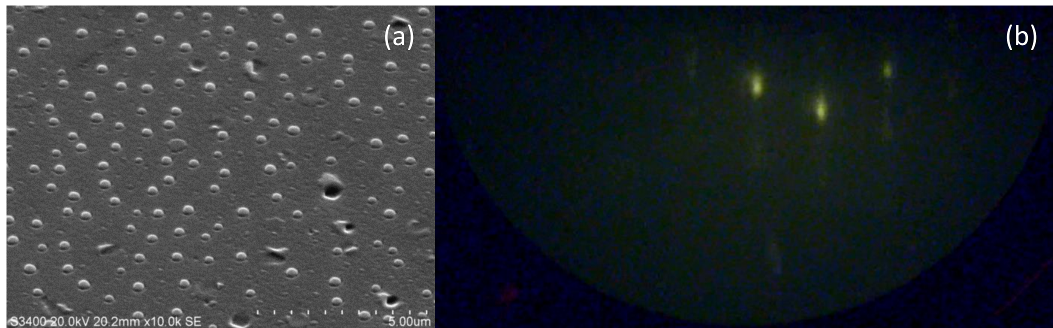


Fig.7.4 SEM images (a) and RHEED pattern (b) of sample at T_{growth} = 180 s

At T_{growth} = 300 s, the shape of dots began to elongate vertically and looked more like nanowire structures. Holes became deeper and had considerable increase in density. RHEED pattern was similar to previous sample with lower intensity.

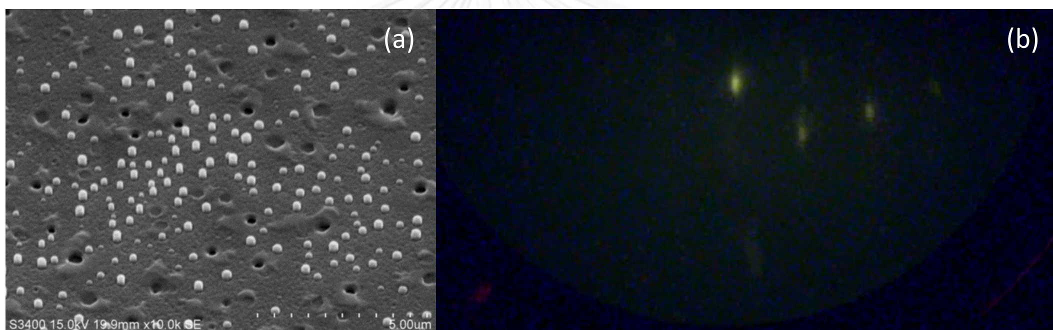


Fig.7.5 SEM images (a) and RHEED pattern (b) of sample at T_{growth} = 300 s

CHULALONGKORN UNIVERSITY

At T_{growth} = 600 s, short nanowires were formed and surrounded by shallow holes. The nanowire density dropped along with hole density. RHEED pattern was almost unobservable, only dimly spots remained.

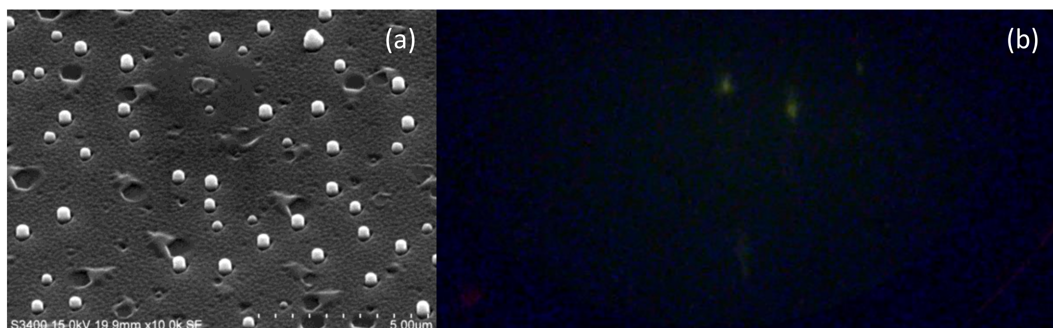


Fig.7.6 SEM images (a) and RHEED pattern (b) of sample at T_{growth} = 600 s

At T_{growth} = 1800 s, all nanowires grew vertically along (111) directsion as they formed directly from GaAs substrate. Holes became shallower with increasing growth time and started to get buried. No parasitic growth is observable since it was already merged with GaAs buffer layer. RHEED intensity increased from previous sample and displayed a sign of Wurtzite (WZ) with twinned structures[40] which is opposed to the conventional growth of self-catalyzed GaAs nanowires with SiO_2 which mostly adopt Zincblende (ZB) structure[41]. This was probably due to the lower surface energy of GaAs (111)B surface compared to SiO_2 surface in the conventional self-catalyzed VLS that causes nucleation to occur at triple phase line hence nanowires with WZ structure[37].

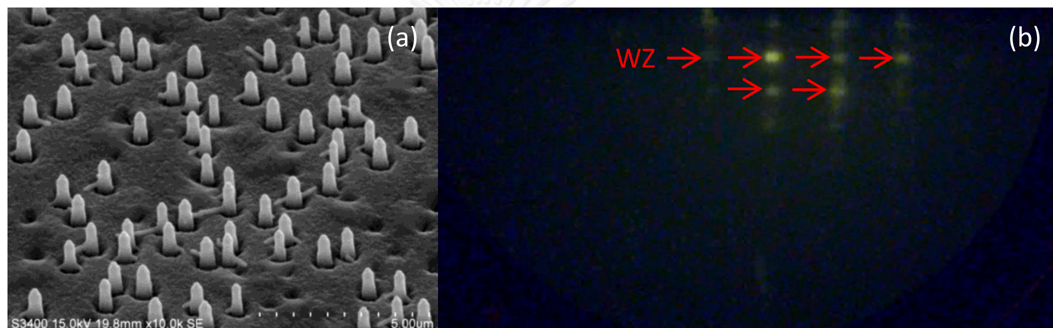


Fig.7.7 SEM images (a) and RHEED pattern (b) of sample at T_{growth} = 1800 s

จุฬาลงกรณ์มหาวิทยาลัย
Chulalongkorn University

7.2.2 Surface morphology analysis

Changes in nanowire/dot density, hole density, and length of nanowire/dot over time were examined via SEM images for better understanding of what occurred during the growth process.

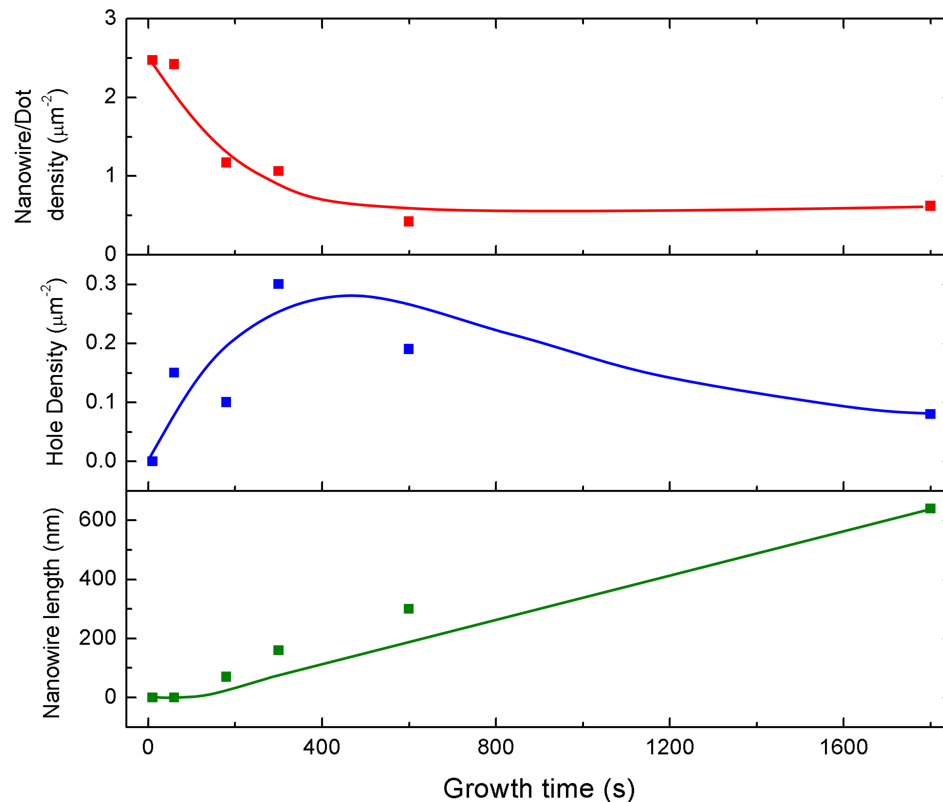


Fig. 7.8 Graph of nanowire density, hole density, and nanowire length as functions of growth time

As seen from graphs in Fig.7.8, the density of nanowires and dots reached the highest point at 2.42 $(\mu m)^{-2}$ just after Ga droplets were deposited on substrate at growth time of 10 s. Density of nanowires and dots became lower from then on and seemed to be stable when the growth time was more than 600 s. On the other hand, hole density rose sharply when the growth time increased from 10 s to 300 s and started to decline at more than 300 s growth time. We can see the correlation between change in nanowire/dot density and hole density, the density of holes increased with a decrease in density of nanowires and dots when growth time was between 10 s and 300 s. The nanowire growth seemed to be suppressed at the beginning as seen from unchanged length during the growth time of 10 s to 60 s before steadily went up after that.

7.2.3 RHEED intensity evolution

Evolution of RHEED intensity was investigated by measuring intensity of a Bragg spot on [11-0] azimuth throughout the whole growth process. Intensity oscillation shown in Fig.7.9 was caused by rotation of substrate. With data from RHEED analysis, we can determine growth mode and nucleation time of nanowires.

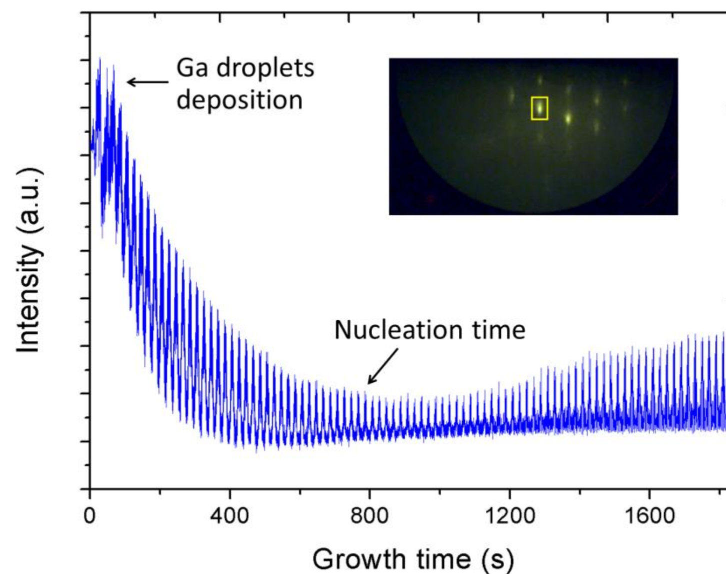


Fig. 7.9 Graph of time evolution of RHEED intensity,

yellow square mark in the inset is region of interest

Chulalongkorn University

There was slightly bump in RHEED intensity just after Ga droplets were deposited on substrate as RHEED pattern transformed from 2D to 3D spotty pattern. The intensity dropped down drastically after that, this implied that the substrate surface was under Ga rich condition. Ga liquid droplets could obscure reflection of electron beam[37] same as displayed in Fig. 7.10. The intensity recovered when the growth process was carried on for 800 s and kept increasing until the end of the process. This trend of RHEED intensity dropping before recovering up to the end of the process corresponds to nucleation time of self-catalyzed VLS growth[51]. This suggests that our nanowires were grown by self-catalyzed VLS mode with very long nucleation time (> 10 minutes).

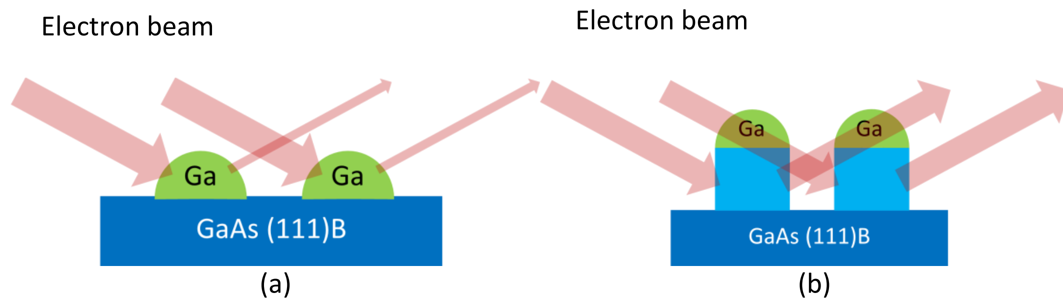


Fig. 7.10 Ga droplets can obscure diffraction signal from electron beam (a) Reflection signal gets better as nanowire growth progresses (b)

7.2.4 Growth model

With data taken from morphological evolution of nanowires and RHEED analysis, we decided to propose a simple growth model of GaAs nanowires grown by self-catalyzed VLS on GaAs (111)B substrate without SiO_2 layer. According to Fig. 7.11 (a) shows the droplet deposition process which is similar to the conventional self-catalyzed VLS. Ga droples are deposited on substrate as initial seed particles with size distribution that can be controlled by deposition rate and substrate temperature[52]. Fig. 7.11 (b) The nanowire growth begins when the substrate is exposed to Ga and As sources. Since this growth is performed on bare GaAs substrate which has much higher sticking coefficient than on SiO_2, Ga atoms have to overcome the stickiness of substrate surface and reach Ga droplets to form nanowires which is the cause of slower growth rate and longer nucleation time than conventional VLS growth[51]. Ga adatoms that are unable to reach Ga seeds are left on substrate surface and start forming GaAs buffer layer simultaneously with the growth of nanowires Fig. 7.11 (c) as nanowire growth continues, some of Ga seeds start to be crystallized and transform to ring-like structures. This result resembles the growth of GaAs quantum ring[49] which is normally performed under unusually low V/III ratio similar to our nanowire growth which were also performed under V/III ratio of 5, almost an order of magnitude higher than typical conventional VLS growth. Fig. 7.11 (d) the majority of nanowires grow vertically. Rings start to become shallower and eventually get

buried as GaAs buffer layer grows thicker. Other bulk or parasitic structures are merged with the buffer layer as previously mentioned.

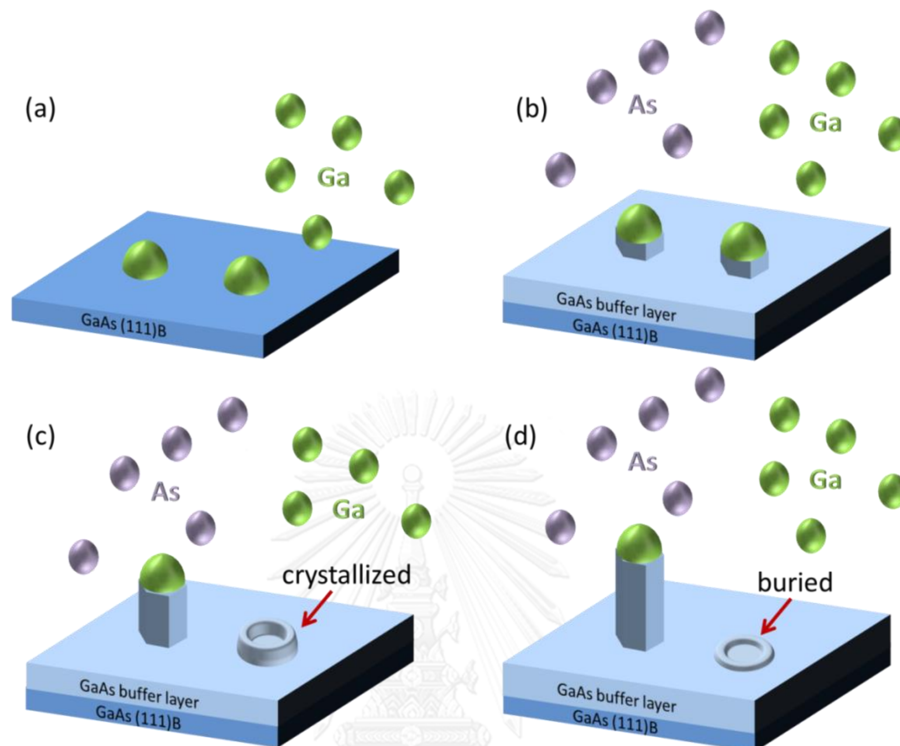


Fig. 7.11 Growth model of self-catalyzed GaAs nanowire growth on GaAs (111)B without SiO_2 layer

Chulalongkorn University

7.3 Summary

A simple growth model of self-catalyzed GaAs nanowires on GaAs (111)B substrate without SiO_2 was proposed. According to the growth model, nanowires originate from dot structures spreading all across substrate surface. Dots collect materials from Ga and As sources and start elongating to become nanowires. RHEED data suggested that these nanowires were actually grown under VLS mode since RHEED intensity became dimmer at the start before recovering after a period of time. However, the nucleation time is determined by recovering time of RHEED intensity from our growth process was unusually high compared to conventional VLS growth from other studies. However some dots are unable to fully develop and transform to

nanohole structures instead. These nanohole structures will become shallower with time and start to get buried when GaAs buffer layer grows thicker. At the end of process, only nanowires are left on the surface while some other structures like nanoholes and parasitic growths are completely buried by buffer layer.

จุฬาลงกรณ์มหาวิทยาลัย
Chulalongkorn University

Chapter 8
Conclusion

We have demonstrated the growth of self-catalyzed GaAs nanowires directly on GaAs (111)B substrates without SiO_2 layer by molecular beam epitaxy technique using Ga droplets as seed particles.

Due to the stickiness of GaAs surface, our nanowires grew under considerably higher Ga flux rate around an order of magnitude higher than under conventional VLS growth to maintain Ga supply to seed particles. However under extensively high Ga flux, the nanowire growth was greatly suppressed and there are Ga chunks emerging on the substrate surface instead of the nanowires. The density of nanowires seems to be unaffected by Ga flux since it is already determined by density of Ga droplets.

The nanowires are grown at temperature range between 400°C to 600°C. Non-optimal growth temperature suppresses the growth of nanowires due to insufficient difference of chemical potential between materials in different states. The growth rate of nanowires does not increase with increasing the substrate temperature as much as it supposed to, we suspect the unusual high Ga flux rate to be the cause as the effect from high Ga flux overcome the effect of growth temperature. The nanowire density increases with increasing growth temperature due to accumulation of Ga droplets at high temperature.

There is a vast difference between GaAs nanowires grown directly on GaAs (111)B substrate and on Si (111) substrate covered with native SiO_2 layer. The parasitic structures are clearly visible on SiO_2 covered substrate while non-existent on bare GaAs as they already merged with buffer layer. The vertical yield is substantially better on bare GaAs since all nanowires are able to grow directly on substrate instead of pinholes which only occur uniformly on precisely crafted SiO_2 layer. Under similar growth parameters, the nanowire growth rate on GaAs (111)B substrate without SiO_2 is lower than on SiO_2-covered substrate however the density seems to be opposite. It is very interesting that nanowire structure transform from ZB-dominated in

conventional self-catalyzed VLS to WZ-dominated in our growth without SiO_2, the difference between surface energy on both substrates is likely to be the cause of this transformation.

By in-situ observation along with SEM, we can see that our nanowires started growing from small dots originated from Ga droplets. Dots elongated with time and became nanowires however there are some dots that unable to obtain enough Ga supply crystalized to ring-shaped or nanohole structures which were later buried by GaAs buffer layer. RHEED intensity data show that the nanowires still grew under VLS mechanism as the intensity dropped down initially but recovered after the growth already initiated. However, the nucleation time of nanowires grown under our method is much longer than under conventional VLS.

With the current state of nanotechnology, nanowire is one of nanostructure with the highest potential however some issues in the fabrication process can prevent it from being a candidate in many novel applications. Hence we proposed this growth method in order to overcome some technical difficulties and simplify the growth process of nanowires. We believe that this dissertation will provide the useful information and thought-provoking idea for nanowire development in the future.

จุฬาลงกรณ์มหาวิทยาลัย
Chulalongkorn University

REFERENCES

1. Vorathamrong, S., et al., Advanced Materials Research, 2016. **1131**: p. 12-15.
2. Vorathamrong, S., et al. *Growth of GaSb nanowires on Si (111) substrates by molecular beam epitaxy*. in *ICMAT*. 2015.
3. Lieber, C.M. and Z.L. Wang, MRS Bulletin, 2007. **32**(2): p. 99-108.
4. Yao, M., P.D. Kapus, and C.W. Zhou, Nano Letters, 2014. **14**(6): p. 3293-3303.
5. Cui, Y., et al., Nano Letters, 2003. **3**(2): p. 149-152.
6. Yi, K.S. and M.J. Kim, Nano Letters, 2011. **11**(12): p. 5465-5470.
7. Gutschea, C., et al., Journal of Applied Physics, 2009. **105**(024305).
8. Cao, L., et al., Nature Materials, 2009. **8**: p. 643-647.
9. Krogstrup, P., et al., Nature Photonics, 2013. **7**: p. 306-310.
10. Breuer, S., *Molecular Beam Epitaxy of GaAs Nanowires and their Suitability for Optoelectronic Applications*. 2011.
11. Filippov, S., et al., Nano Letters, 2014. **14**(9): p. 5264-5269.
12. Yousefi, R. and B. Kamaluddin, Journal of Alloys and Compounds, 2009. **479**(1-2): p. 11-14.
13. Saxena, D., et al., Nature Photonics, 2013. **7**: p. 963-968.
14. Zhao, S., et al., Applied Physics Letter, 2016. **109**(191106).
15. Li, L., et al., The Journal of Physical Chemistry C, 2013. **117**(8): p. 4253-4259.
16. Zhang, M.-L., et al., The Journal of Physical Chemistry C, 2008. **112**(12): p. 4444-4450.
17. Tomioka, K., et al., IEEE Journal of Selected Topics in Quantum Electronics, 2011. **17**(4).
18. Rahman, S.F.A., et al. in *AIP Conference*. 2009.
19. S., W.R. and E.W. C., Applied Physics Letter, 1964. **4**(5): p. 89.
20. Levitt, A.P., *Whisker Technology*. 1970.
21. Tchernycheva, M., et al., Journal of Applied Physics, 2007. **102**(094313).
22. Breuer, S., et al., Nano Letters, 2011. **11**(3): p. 1276-1279.
23. Morral, A.F.i., C. Colombo, and G. Abstreiter, Applied Physics Letter, 2008. **92**(063112).
24. Matteini, F., et al., Journal of Crystal Growth, 2014. **404**: p. 246-255.
25. Herman, M.A. and H. Sitter, *Molecular Beam Epitaxy Fundamentals and Current Status*. 1989.
26. Braun, W., *Applied RHEED : Reflection High-Energy Electron Diffraction during Crystal Growth*. 1999.
27. Koster, G. and G. Rijinders, *In Situ Characterization of Thin Film Growth*. 2011.
28. Mazurek, P., A. Daniluk, and K. Paprocki, Vacuum, 2004. **72**(4): p. 363-367.
29. Reimer, L., *Scanning Electron Microscopy : Physics of Image Formation and Microanalysis*. 1998.
30. Zolotoyabko, E., *Basic Concepts of X-Ray Diffraction*. 2014.
31. Spirovska, D., et al., *Advanced in Solid State Physics*. Vol. 48. 2009. 13-26.
32. Detz, H., et al., Nanotechnology, 2015. **26**(315601).

33. Venables, J.A., et al., Journal of Physics and Chemistry of Solids, 1994. **55**: p. 955.
34. Giang, L.T.T., et al., Journal of Crystal Growth, 2013. **364**: p. 118-122.
35. Harmand, J.C., et al., Journal of Crystal Growth, 2007. **301-302**: p. 853-856.
36. Froberg, L.E., W. Seifert, and J. Johansson, Physical Review B, 2007. **76**(153401).
37. Herterberger, S., *Growth and Properties of In(Ga)As Nanowires on Silicon*. 2012.
38. Chen, X.L., et al., Journal of Crystal Growth, 2001. **222**(586-590).
39. Borgstrom, M.T., et al., Nature Nanotechnology, 2007. **2**.
40. Breuer, S., et al., Physical Review B, 2010. **82**(075406).
41. Cirlin, G.E., V.G. Dubrovskii, and Y.B. Samsonenko, Physical Review B, 2010. **82**(035302).
42. Ambrosini, S.F., *MBE Growth of self-assisted GaAs nanowires and their characterization*. 2012.
43. Glas, F., J.C. Harmand, and G. Patriarche, Physical Review Letters, 2007. **99**(146101).
44. Walletin, J., et al., Nano Letters, 2010. **10**(12): p. 4807-4812.
45. Munshi, A.M., et al., Journal of Crystal Growth, 2013. **372**: p. 163-169.
46. Wang, Z.M., et al., Applied Physics Letter, 2007. **90**(113120).
47. Mano, T., T. Kuroda, and S. Sanguinetti, Nano Letters, 2005. **5**(3): p. 425-428.
48. Mano, T., K. Watanabe, and S. Tsukamoto, Journal of Crystal Growth, 2000. **209**: p. 504-508.
49. Stavrou, V.N., *Quantum Dots - Theory and Applications*. 2015.
50. Plissard, S., K.A. Dick, and G. Larrieu, Nanotechnology, 2010. **21**(385602).
51. Rudolph, D., S. Hertenberger, and S. Bolte, Nano Letters, 2011. **11**: p. 3848-3854.
52. Somaschini, C., et al., Nano Letters, 2013. **13**: p. 3607-3613.

จุฬาลงกรณ์มหาวิทยาลัย
Chulalongkorn University

APPENDIX

จุฬาลงกรณ์มหาวิทยาลัย
CHULALONGKORN UNIVERSITY

List of publications

1. S. Vorathamrong, P. Prongjit, S. Panyakeow, S. Ratanathammaphan, P. Praserthdam, and C. Tongyam, *"Effect of Ga Pre-Deposition Rate on GaAs Nanowires Grown by Self-Assisted VLS Method Using MBE on SiO_2/Si(111) Substrates"* Advanced Materials Research 1131, 12-15 (2016)

2. P. Prongjit, S. Vorathamrong, S. Panyakeow, C. Tongyam, P. Prasertthdam, S. Ratanathammaphan, *"Effect of SiO_2 Thickness on GaAs Nanowires on Si (111) Substrates Grown by Molecular Beam Epitaxy"* Advanced Materials Research, Vol. 1131, 16-19 (2016)

3. Samatcha Vorathamrong, Somchai Ratanathammaphan, Somsak Panyakeow, Piyasan Praserthdam, Chiraporn Tongyam, *"Effect of substrate temperature on self-assisted GaAs nanowires grown by Molecular Beam Epitaxy on GaAs (111)B substrates without SiO_2 layer"* Journal of Crystal Growth 2017 (In progress)

4. Samatcha Vorathamrong, Somchai Ratanathammaphan, Somsak Panyakeow, Piyasan Praserthdam, Chiraporn Tongyam, *"Comparison of self-assisted VLS GaAs nanowires grown by MBE on Si (111) and GaAs (111)B substrates"* proceeding, IOP Conference series 2017 (In progress)

5. Samatcha Vorathamrong, Somchai Ratanathammaphan, Somsak Panyakeow, Piyasan Praserthdam, Chiraporn Tongyam, *"Observation of self-assisted GaAs nanowire growth by molecular beam epitaxy on GaAs (111)B without SiO_2 layer"* Materials Research Express 2017 (Submitted)

List of presentations

1. S. Vorathamrong, P. Prongjit, S. Panyakeow, S. Ratanathammaphan, P. Praserthdam, and C. Tongyam, *"Effect of Ga Pre-Deposition Rate on GaAs Nanowires Grown by Self-Assisted VLS Method Using MBE on SiO_2/Si(111) Substrates"*, The 4th Thailand International Nanotechnology Conference, Nov 25-28 2014 (Poster)

2. Samatcha Vorathamrong, Somchai Ratanathammaphan, Somsak Panyakeow, Piyasan Praserthdam, Chiraporn Tongyam, *"Growth of Gasb Nanowires on Si (111) Substrate by Molecular Beam Epitaxy"*, 8th International Conference on Materials for Advanced Technologies, June 28 – July 3 2015 (Poster)

3. Samatcha Vorathamrong, Somchai Ratanathammaphan, Somsak Panyakeow, Piyasan Praserthdam, Chiraporn Tongyam *"Growth of Self-Assisted GaAs nanowires on GaAs(111) substrates by Molecular Beam Epitaxy"* International Conference on Nanoscience and Nanotechnology, Feb 7-11 2016 (Poster)

4. Samatcha Vorathamrong, Somchai Ratanathammaphan, Somsak Panyakeow, Piyasan Praserthdam, Chiraporn Tongyam, *"Comparison of self-assisted VLS GaAs nanowires grown by MBE on Si (111) and GaAs (111)B substrates"*, 33rd International Conference on the Physics of Semiconductors, Jun 31 – Aug 5 2016 (Poster)

5. Samatcha Vorathamrong, Somchai Ratanathammaphan, Somsak Panyakeow, Piyasan Praserthdam, Chiraporn Tongyam, *"Effect of substrate temperature on self-assisted GaAs nanowires grown by Molecular Beam Epitaxy on GaAs (111)B substrates without SiO_2 layer"* 19th International Conference on Molecular-Beam Epitaxy, Sep 4-9 2016 (Poster)

จุฬาลงกรณ์มหาวิทยาลัย
Chulalongkorn University

VITA

Mr. Samatcha Vorathamrong was born on December 27, 1984 in Bangkok, Thailand. He finished his elementary and middle school from Assumption College before moving to Triam Udom Suksa school for his high school diploma. After graduation from Triam Udom Suksa school, Samatcha went to Chulalongkorn University for his Bachelor's Degree in Engineering. He joined Semiconductor Device Research Laboratory (SDRL) to do his research project in semiconductor and nanoelectronics for the first time as the 4th year bachelor student. After that he continued his studying in Chulalongkorn University for Master's Degree in Electrical Engineering. He enrolled at Chulalongkorn University for the 3rd time to pursuit his Ph.D. in Electrical Engineering under the guidance of Assoc.Prof. Dr.Somchai Ratanathammaphan. During Ph.D. study, he was awarded a scholarship from the 100th Anniversary Chulalongkorn University Fund for Doctoral Scholarship. His interests are in nanostructures fabrications and applications especially the approaches to create nanostructures with more simple and efficient processes as well as easy for device implementations.

จุฬาลงกรณ์มหาวิทยาลัย
Chulalongkorn University