CHAPTER III

DESIGN STRUCTURES OF HETEROJUNCTION BIPOLAR TRANSISTOR

3.1 Conceptual Design of Heterojunction Bipolar Transistor

In all real transistors only part of the base resistance lies underneath the emitter, and between the edge of the emitter and the base contact. Usually, the outer region of the base is appreciably thicker than the inner region, and the near surface portion of the outer base is more heavily doped than the remainder (Fig. 3.1-a). This design *minimizes* the outer base resistance. If one wishes to obtain the postulated advantages of a wide-gap emitter, the outer base resistance is not permitted to dominate the overall base resistance. For example, the changing from a (diffused or implanted) homojunction emitter to a heterojunction emitter, forced a change in geometry from Fig. 3.1-a to Fig. 3.1-b with a thin outer base. This is in fact the geometry used in the HBTs reported in the literature, except for the transistors reported by Ankri et al. [14] and by Katz et al. [15].

Even though the doping level in the outer base may have been increased, the beneficial effect of this change would be least partially compensated by the reduction in thickness of the outer base. In unfavorable cases, the outer base resistance might even have increased. Ladd and Feucht fully recognized the importance of this problem [16]. The important realization is that the wide-gap emitter configuration contains a built-in design possibility to keep the low outer base resistance [17], [18], [19]. The design is shown in Fig. 3.2.

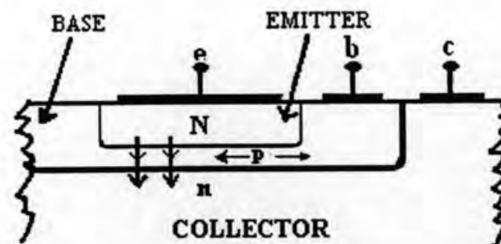

Fig. 3.1-a Design of Homojunction Bipolar Transistor with thicker outer base

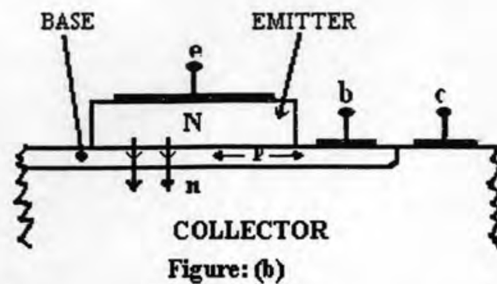

Fig. 3.1-b Design of Heterojunction Bipolar Transistor with thinner outer base

Rather than constructing the wide-gap emitter as an island riding by itself on the top of a uniformly thin narrow-gap base layer, the wide-gap semiconductor may be extended beyond the emitter edge, forming part of the outer base region, with the emitter-base pn junction pulled away from the heteroboundary and towards the surface. Such a configuration should be easily achievable by first growing the top wide-gap layer with the same relatively low n-type doping as the emitter, and then converting the region outside the emitter to heavy p-type doping by diffusion or regrown technique. In homojunction transistors Fig. 3.1-a, the base region is usually much thicker and more heavily doped outside the emitter than between the emitter and collector, reducing the external base resistance. This desirable feature would be lost in heterostructure transistors with the emitter island design shown in Fig. 3.1-b. To appreciate this point fully, recall that in actual structures the horizontal dimensions greatly exceed the vertical ones. In this drawing, the vertical dimensions have been greatly exaggerated relative to the horizontal ones as shown in Fig. 3.2.

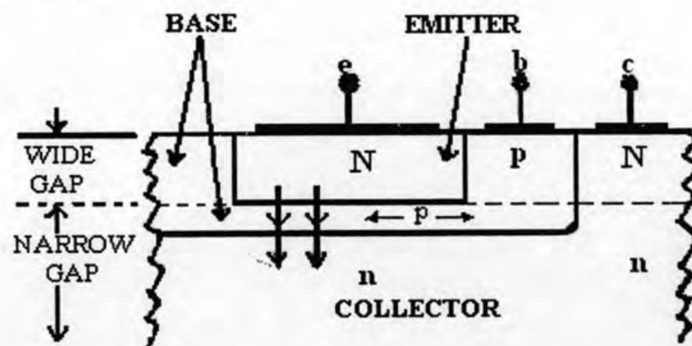

Fig. 3.2 Desirable emitter structure in which the p-n junction does not follow the planar heterointerface, but is pulled up towards the surface.

In such a design the portion of the vertical emitter-base junction that lies within the wide-gap region carries only a negligible current, compared to the horizontal wide-narrow portion under the emitter ohmic contact. The reason for this is illustrated in Fig. 3.3. For injection into the wide-gap region, the electrons would have to climb a barrier that is higher by the energy gap difference ΔE_g. But this reduces the injection current density by the same factor exp $(-\Delta E_g /kT)$ that also reduces the hole injection into the wide-gap emitter. This possibility does not appear to have been as widely recognized as it deserves; it has been used in the devices reported by Ankri et al. [14], and by Katz et al. [15].

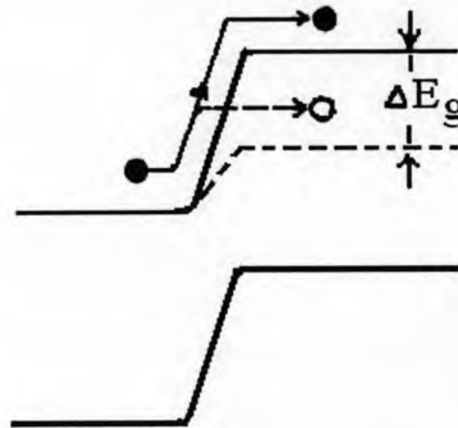

Fig. 3.3 Blocking of injection of electrons into the wide-gap portion of the base region

In the interest of charge collection, the bipolar transistors have been built with a larger collector than emitter area. Since the planar technology which has the two junctions are necessarily of different area the efficient charge collection then need enforces the familiar configuration with the collector at the bottom and the emitter at the top. The exception to this rule is, of course, integrated injection logic (I^2L), but apart from the I^2L exception, the "emitter-up rule" is more employees that it has become hard to imagine that a useful transistor could be built with the inverse order. Now we have just seen that with a wide-gap emitter junction can be designed in such a way that part of the emitter-base junction does not inject carriers. Evidently, with such a design the need for efficient carrier collection can be met even with an emitter larger than the collector, if

those portions of the emitter-base junction that are not immediately opposite to a part of the collector-base junction are inactivated by pulling them onto the high-gap side of the hetero-interface. Once this is done, the transistor might just as well be "flipped," with the emitter on the substrate side and the collector on top, as shown in Fig. 3.4. The inverted configuration has several advantages, to the point that it might very well turn out the "canonical" configuration of future heterostructure bipolar transistor design [20]. The principal (but not the only) advantage of the inverted transistor is that it permits the use of a significantly smaller collector area, with an appropriately smaller collector capacitance. The consequences for the high-speed performance are obvious.

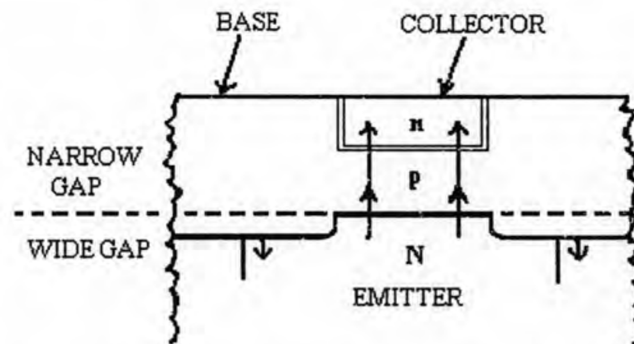

Fig. 3.4 Inverted Collector-up structure of HBT

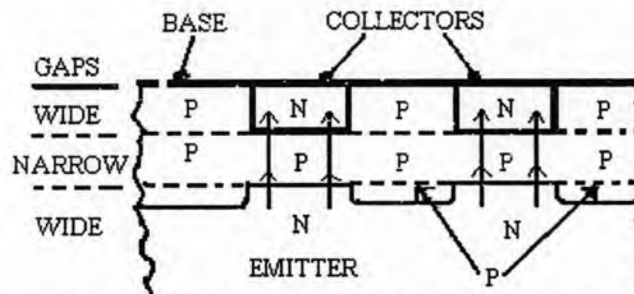

Fig. 3.5 A DH implemtation of I^2L, combining wide-gap collectors with noninjectimg emitter regions between the collectors.

Modem high speed transistors, digital and microwave transistors, typically have a collector area close to three-times the active (emitter) area. Inverting the structure thus permits a reduction of the collector capacitance by close to a factor of 3 due to the emitter area was 3.4-times the collector area. [21]. If the device reduces the collector area by a factor of 1/3 and leaves all other quantities unchanged, the switching time will be reduced

from -18 ps to -7 ps that are analyzed by Dumke et al. [21].Similar improvements would occur in microwave power transistors. However, the total emitter area is larger than the active area; the emitter junction capacitance will increase, at least compared to a heterostructure transistor of conventional emitter-up configuration. But, the emitter junction capacitance per unit area of a heterojunction transistor can in any event be made significantly less than for a homojunction transistor. Hence, a net reduction in emitter capacitance may result even in the face of a larger (inactive) emitter area.

Design for transistors should be obeyed the following conditions,

(1) Suppression of hole injection from base into collector in digital switching transistors under condition of saturation;

(2) Emitter/collect or interchangeability in IC's;

(3) Separate optimization of base and collector especially in microwave power transistor;

If the base region is heavier doped than the collector, a copious injection of holes from the base into the collector takes place, which increases dissipation and slows down the switching speed. In a heterostructure technology, this highly deleterious phenomenon is easily suppressed by the same way hole injection into the emitter with making the wide-gap collector. Just as the wide-gap emitter, the wide-gap collector should be fairly lightly doped, in the interest of a low collector capacitance, and the base should remain heavily doped, in the interest of low base resistance. This choice of relative doping levels remains both possible and desirable in the inverted I^2L configuration, rather than calling for a weakly doped base to suppress collector injection, with its high base resistance penalty. It avoids both the electron injection into those portions of the base where such injection is undesimble because of the absence of a collector opposite to the emitter, and the injection of holes into either collector or emitter. This kind of transistor can be seen in Fig. 3.5. A different advantage lies in the possibility of designing transistors in which the role of emitter and collector can be interchanged by simply changing the biasing conditions as see in Fig. 3.6, while retaining the advantages of a wide-gap emitter regardless of which of the two terminal n-regions is used as the emitter.

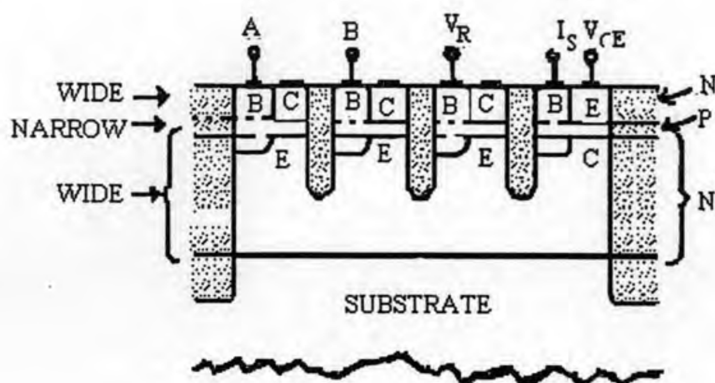

Fig. 3.6 Input stage of a DH implementation of ECL

To achieve this freedom, the transistor need not be geometrically symmetrical as Fig. 3.6 in which the active portion of the lower pn junction covered the same area as the upper pn junction; either the upper junction or the lower junction could be used as the emitter. The DH design makes it possible, within a common three-layer n-p-n epitaxial layer structure, to integrate high-performance wide gap emitter transistors having the conventional emitter-up configuration, with similar transistors having the I^2L like inverted emitter-down configuration.

In the present study of this thesis, the external base layer of HBTs were fabricated by the two processes which are diffuse base process and regrown base process as shown in the Fig. 3.7 and Fig. 3.8. The diffuse base can be used very easily to make the external base by adjusting the diffuse thickness with the variation of temperature. Zinc (Zn) has been used to get the external base as a diffuse material that can change from the n-type material to the p-type material due to the high diffusion coefficient of it. The external base layer is rather thick compared than the internal base and also heavily doped relatively to the internal base which can get the extremely low base resistance and high frequency response.

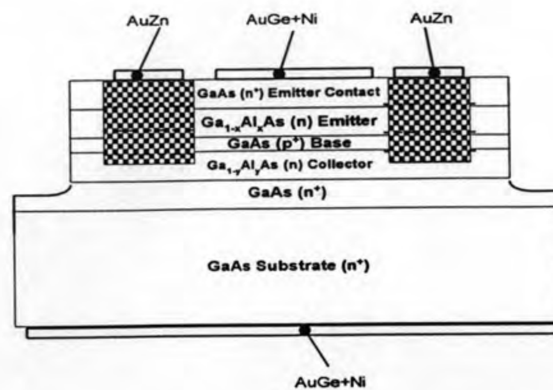

Fig. 3.7 Design structure of the Diffuse Base HBT

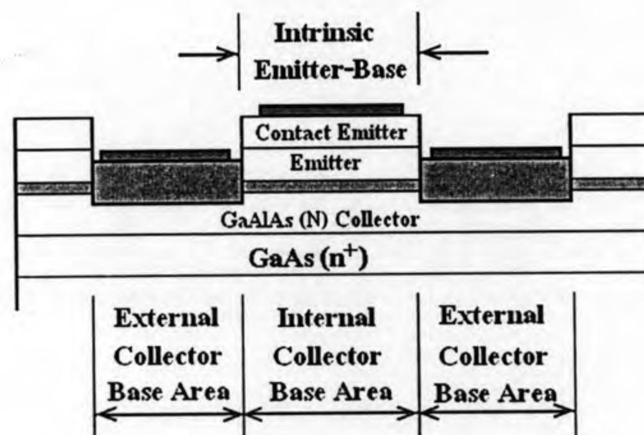

Fig. 3.8 Design structure of the Regrown Base HBT

In the case of regrown base process, the external base layer can be made definitely by the growth interruption time. Moreover, these design structure would be protect some leakage current from the collector base and emitter base junctions and also can be developed not only to the symmetrical characteristic but also the collector-up structures which is also mentioned above. Result, it will cause the extremely low base resistance and high frequency response with suitable current gain for the microwave or milli wave integrated circuit applications. In this we made the single external base layer and double external base layer with three materials that are GaAs , GaAlAs (x=0.2) and GaAs / GaAlAs (x=0.2) as shown in figures 3.9, 3.10 and 3.11 respectively.

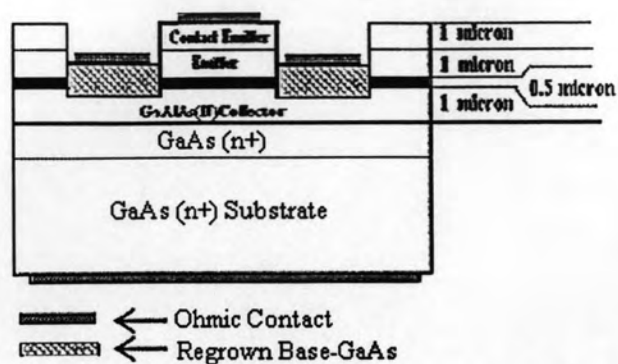

Fig. 3.9 Design structure of single Regrown Base HBT with GaAs

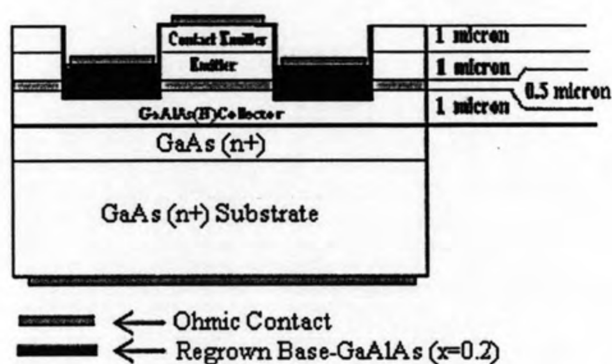

Fig. 3.10 Design structure of single Regrown Base HBT with GaAlAs (x=0.2)

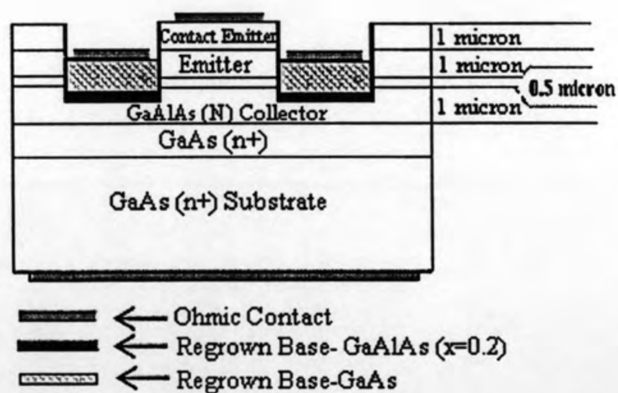

Fig. 3.11 Design structure of double Regrown Base HBT with GaAs / GaAlAs (x=0.2)

3.2 Epitaxial Structure

Fig. 3.12-a and Fig. 3.12-b show a typical structure for a single heterojunction bipolar transistor (SHBT) and double heterojunction bipolar transistor (DHBT). The basic device is an npn-transistor with "emitter up" design having abrupt junctions between the epitaxially grown layers. In practice, several modifications to the basic structure are made to boost up the transistor speed and to make more perfect for the ohmic contacts. Fig. 3.13 shows the heterojunction bipolar transistor with the most common modifications and Fig. 3.14 shows the structure of double heterojunction bipolar transistor in the present thesis. The cross section of DHBTs with epitaxial layers as in Fig. 3.14 was shown in figures 3.9, 3.10 and 3.11. The collector layer is lightly doped to reduce the base-collector capacitance. Emitter layer is the same as collector layer to get the symmetrical characteristics between the EB and CB junctions. The emitter is capped with a heavily doped GaAs layer. This layer shields the oxygen sensitive emitter while serving as a contact layer. It would be rather difficult to form a low resistivity contact directly to AlGaAs.

The epitaxial HBT structure is usually grown either using molecular beam epitaxy (MBE) or metallo-organic vapor phase epitaxy (MOVPE) or liquid phase epitaxy (LPE). Traditional MOVPE uses silicon as donor type dopant in GaAs, and zinc as acceptor type dopant in GaAs. MBE uses typically beryllium for acceptor type doping in GaAs. Both zinc and beryllium diffuse relatively rapidly in GaAs, and Zn redistribution during epitaxial growth with MOVPE has been a concern especially when highly silicon doped layers are involved [22]. When acceptor atoms diffuse from base to emitter side, the pn-junction is shifted away from the heterojunction and the electrical structure is destroyed. Also, it has been difficult to achieve electrically active acceptor concentrations over 5×10^{18} cm^{-3} compare with LPE. In case of LPE technology Germanium (Ge) and Zinc (Zn) has been used as the acceptor type dopants in GaAs to make the internal and external base and also Tellurium (Te) and Tin (Sn) as n-type of collector and emitter layers.

Emitter, moderately doped n-type GaAlAs
Base, heavily doped p-type GaAs
Collector, moderately doped n-type GaAs
GaAs (n-type) Substrate

Fig. 3.12-a A typical structure for a single heterojunction bipolar transistor

Emitter, moderately doped n-type GaAlAs
Base, heavily doped p-type GaAs
Collector, moderately doped n-type GaAlAs
GaAs (n-type) Substrate

Fig. 3.12-b A typical structure for a double heterojunction bipolar transistor

Mask Layer, non-doped GaAlAs
Contact Emitter, heavily doped (n-type) GaAs
Emitter, Lightly doped (n-type) GaAlAs
Base, heavily doped (p-type) GaAs
Collector, Lightly doped (n-type) GaAlAs
Sub-Collector, heavily doped (n-type) GaAs
GaAs (n-type) Substrate

Fig. 3.13 General structure for a double heterojunction bipolar transistor (DHBTs)

Layer	Thickness
Mask Layer of GaAlAs (N)	**2 micron**
GaAs(n^+) Emitter Contact	**1 micron**
GaAlAs(N) Emitter	**1 micron**
GaAs(p^+) Base	**0.5 micron**
GaAlAs(N) Collector	**1 micron**
GaAs (n^+)	
GaAs Substrate (n^+)	

Fig. 3.14 Epitaxial structure of the double heterojunction bipolar transistor in this experiment

The epitaxial structure of our own design symmetrical transistor is represented in Fig. 3.14 and the epitaxial layers of the designed HBTs are explained in detail below.

n^+ - GaAs substrate {100} oriented

The substrate is (Si-doped) n-type. Crystal orientation is {100} to allow proper orientation of transistor mesa isolation patterns with connection metal patterns. The correctly oriented mesa hills will have positive slopes in the direction where metal connection wires enter the mesa hill. This increases the reliability of the process as metal breaks are avoided.

(Te-doped) GaAs buffer layer, 1×10^{19} cm^{-3}

This layer helps decreasing the defect density of the actual epitaxial structure and also to be easy grown for the collector layer.

N (Sn-doped) GaAlAs collector, x=25%, 5×10^{17}, 1- μm

This layer is the collector. It is lightly doped to allow the pn-junction depletion region to be wide thus reducing the base-collector capacitance. The maximum frequency of oscillation f_{max} (or the power gain cut off frequency) of the transistor inversely proportional to the product of base series resistance and base-collector capacitance. Reducing both will increase the transistor high frequency performance. And then, the depletion region depth in thermal equilibrium will be about 218 nm with base doping about 10^{19} cm^{-3}. [23], [24].With a 400 μm^2 device active area this gives base-collector depletion capacitance of C_{bc}= 0.2 pF. Assuming a series resistance of 1 Ω, the charging time constant of the capacitance would be 0.2 ps. [25]. To keep the charging time less than the diffusion transit time of base, the collector series resistance should not exceed 10 Ω. Under normal operation conditions of the transistor, b-c junction would be reversing biased and electrons are accelerated to saturation velocity in the depletion region. An electron with saturation velocity of 2×10^5 ms^{-1} would have the depletion region transit time of about 0.6 ps [26].

p+(Ge-doped) GaAs- base, 5×10^{18} cm-3, <0.5 μm

This layer is the actual base. It is relatively thin to reduce electron transit time from emitter to collector and heavily doped to keep the series resistance low. The doping level is enough to turn the base degenerate. Although simple simulations in chapter 2 suggested that the doping should be reduced for better current gain, it was kept high to make sure a tunneling contact would be formed with base ohmic metal without need for high temperature alloying. With thickness of 1000Å, the base transit time for an electron with saturation velocity of 2×10^5 ms^{-1} would be about 0.5 ps. The diffusion transit time with a typical diffusivity of $D_b = 30$ cm^2s^{-1}would be about 1.7 ps.

N (Sn-doped) AlGaAs emitter, x=20%, 5×10^{17} cm-3, 1-μm

This layer is the actual emitter.

n+ (Te-doped), 1×10^{19}cm-3, GaAs- emitter contact layer, 1-μm

This layer also helps ruling out the spike. In simpler structures this layer is the contact layer for metal, but then it would be prevent ohmic metallization penetration into heterojunction area especially if gold-germanium based ohmic metallization is used. For shallow contacts, a Pd-In metallization scheme could be used where GaAlAs is formed to the semiconductor surface during anneal [27].

N^- (Un-doped) GaAlAs mask layer, x=40%, 6-μm

This layer is un-doped and contains ~40% of Aluminum (Al). It's much thicker than the others to prevent the emitter-contact layer during growth or diffuse the external base. This mask layer is finally selectively removed by Hydrofluoric acid (HF) solution.