References

[1] Kroemer, H.: Heterostructure Bipolar Transistors and Integrated circuits. Proc.IEEE 70, 1 (1982) : 13-25.

[2] The Royal Academy of Sciences Press Release on the Nobel Prize in Physics 2000. October 10, (2000)

[3] Kroemer, H.: Theory of a Wide-Gap Emitter for Transistors. Proc. IRE 45, 11 (1957): 1535-1537.

[4] Morozov, Y. V.: Personalia Zhores Ivanovich Alferov (on his seventieth birthday), Physics – Uspekhi. 43, 3 (2000): 307-08.

[5] W. Shockley,U.S. Patent no. 2569347, Filed 26 June (1948)

[6] Bardeen J., Brattain W. H.: The Transistor, a Semi-Conducting Triode. Phys. Rev. 74, June 25 (1948): 230-331.

[7] Hill, D.: High Voltage HBT Technology, IEEE 20th GaAs IC Symposium 1998 Technical digest. (1998): 149 – 52.

[8] J.P. Bailbe, A. Marty, G. Rey, J. Tasselli and A. Bouyahyaoui, "Electrical Behavior of Double Heterojunction NPN GaAlAs/GaAs/GaAlAs Bipolar Transistors ". Solid State Electron. 28, 6 (1985): 627-638.

[9] Nay Myo Tun, S. Thainoi, C. Antarasena, Proc. EECON-29 EL-26, 2 (2005): 697-701.

[10] Y. Deesirapipat, S. Thainoi, S. Ratanathammaphan and C. Antarasena, "Simple Fabrication Technique of Symmetrical Emitter - Collector Zinc- doped Planar $Ga_{1-x}Al_xAs$/ GaAs/ $Ga_{1-y}Al_yAs$ Double Heterojunction Bipolar Transistors". JJAP 40, 4A, April (2001) : 2127-2131.

[11] Ben G. Streetman, Solid State Electronic Devices, Third Edition (1990)

[12] Kevin F.Brennan, Apiral S.Brown, Theory of Modern Electronic Semiconductor Devices, (2002)

[13] T. Won, S. Iyer, S. Agarwala and H. Morkoc, IEEE Trans. Electron Devices ED-10, 6 (1989) : 274-276.

[14] D. Ankri and A. Scavennec, "Design and evaluation of a planar GaA1As-GaAs bipolar transistor". Electron Lett. 16, 1, Jan. (1980): 44-47.

[15] J. Katz, N. Bar-Chaim, P. C. Chen, S. Margalit, I. Ury, D. Wilt, M. Yust, and k Yariv, " A monolithic integration of GaAs / GaAlAs hetero bipolar transistor and heterostructure laser". AppL Phys. Lett. 37, 2, July (1980): 211-213.

[16] G.O. Ladd and D.L. Feucht, "Performance potential of high - frequency heterojunctiontransistors". IEEE Trans.Electron Devices.17 (1970) : 413-420.

[17] W. Susaki, H. Namizaki, H. Kan, and *k* Ito, J. AppL Phys. 44, 6, June (1973) : 2893-2894.

[18] H. Kroemer, Dev. Res. Conf. 1978, Santa Barbara; see IEEE Trans. 16, Jan. (1969): 102- 107. and Electron Devices.ED-25, Nov. (1978) : 1339.

[19] H. Kroemer, "Heterostructures for everything- device principle of the 1980' s?". Japan J. AppL Phys. 20, 20-1, Jan. (1981): 9-13 (Proc. 12th Conf. Solid-state Devices, Tokyo) and Dev. Res, Bull. Amer. Phys Soc. 24, Mar. (1979): 230.

[20] N. Grote, W. Roth, L. M. Su, and M. N. Svilans, "Realization of a bipolar GaAs / GaAlAs Schottky-collector transistor". Gallium Arsenide and Related Compounds 1980 (Vienna), Inst. Phys. Conf. Ser.56, (1981) : 385-392.

[21] W. P. Dumke, J. M. Woodall, and V. L. Rideout, "GaAs-GaAlAs heterojunction transistor for high frequency operation". Solid-StateElectron.15, 12, Dec. (1972):1339-1334.

[22] Kurishima, K. et al., Growth, Design and Performance of InP-based Heterostructure Bipolar Transistors. K. IEICE Trans. Electron. E78 - C, 9 (1995) :1171- 1180.

[23] Hovinen, A.: Fabrication of a Heterojunction Transistor, Master's Thesis. Electron Physics Laboratory, Helsinki University of Technology, Espoo (1992) (in Finnish)

[24] Hovinen, A.: Process Development and Device Modelling of Gallium Arsenide Heterojunction Bipolar Transistors. Ph.D dissertation, Electron Physics Laboratory, Helsinki University of Technology, Espoo (2001) (in Finnish)

[25] Pruniaux, B. R., Adams, A. C.: Dependence of Barrier Height of Metal Semiconductor (Au-GaAs) on Thickness of Semiconductor Surface Layers. J. Appl. Phys.43 (1972): 1980-83.

[26] Mukherjee, S. D., Woodard, D. W.: Etching and Surface Preparation of GaAs for Device Fabrication, in Howes, M. J., Morgan D. V. (ed.): Gallium Arsenide Materials, Devices and Circuits. New York, John Wiley & Sons, (1985): 119-60.

[27] Wang, L. C., Wang, X. Z., Lau, S. S., Sands, T., Chan, W. K., Kuech, T. F.: Stable and Shallow PdIn ohmic Contacts to n-GaAs. Appl. Phys. Lett. 56 (1990): 2129-31.

[28] Lee, Q., Martin, S. C., Mensa, D., Smith, R. P., Guthrie, J., Rodwell, M. J. W.: Transferred-Substrate Heterojunction Bipolar Transistors. IEEE Eletron. Dev. Lett.20, 8 (1999): 396-98.

[29] Sze, S. M., Physics of Semiconductor Devices. 2nd ed., John Wiley & Sons, New York (1981)

[30] Tosaporn Chavanapranee, "Fabrication and study on Spectrum Response of GaALAs / GaAs Heterojunction Photodiodes". Master Thesis, Chulalongkorn University (2001)

[31] Donald A. Neamen, Semiconductor Physics and Devices. Third Edition (2003)

Appendix

The present research has been submitted to the proceeding of the 29th Electrical Engineering Conference (EECON-29) at Ambassador City Hotel, Jomtien, Chonburi, Thailand on 9-10 October, 2006. The submitted paper is expressed as the following pages from pp. 101-104.

DC Characterization of GaAs/GaAlAs Double Heterojunction Bipolar Transistors with p^+-GaAs Regrown Base

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Abstract GaAlAs/GaAs Double Heterojunction Bipolar Transistors (DHBTs) with p^+-GaAs regrown base have been designed and fabricated by Liquid Phase Epitaxy (LPE) technique. Normal mode gain of 40 and inverted mode gain of 8 were obtained from the same DHBT. Due to the asymmetry of physical structure, inverted mode gains were inferior to those of normal mode and also resulting in offset voltage of 200 mV. Moreover, some DHBTs exhibited a knee-shape characteristic in inverted mode due to influence of spike at emitter-base heterojunction.

Keywords: GaAs, GaAlAs, DHBT, LPE, regrown base, symmetrical emitter-collector, normal mode gain, inverted mode gain, offset voltage

1. Introduction

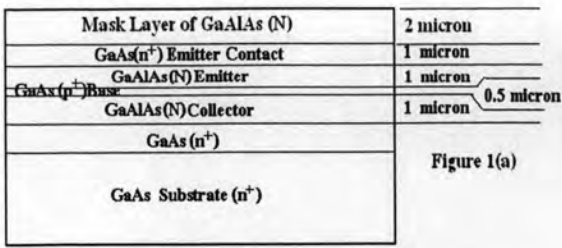
The fabrication of GaAs/GaAlAs heterojunction bipolar transistors (HBT) has been developed and now applied in high speed digital and microwave integrated circuits (ICs). Because the electron mobility of these compound semiconductors is much higher than that of Si, the frequency response of these corresponding devices is therefore higher. Moreover, we can improve the transistor performance with the use of GaAs/GaAlAs heterojunction [1]. First, single heterojunction bipolar transistor (SHBT) with N-GaAlAs emitter and p^+-GaAs base was interesting due to the high injection efficiency inherent in the structure. However, SHBT has several disadvantages especially for their applications in most ICs which the collector should be on the top and similar to that of emitter to reduce the complexity of IC fabrication. SHBTs have the asymmetry between the emitter-base heterojunction and the collector-base homojunction. Therefore, the interchangeability between emitter and collector is impossible. Furthermore, the offset voltage in SHBT is high due to the difference between two junction voltages; this causes plenty of useless power. Hence, the collector-base homojunction should be replaced with the heterojunction similar to that of emitter-base. Double heterojunction bipolar transistors (DHBT) were then proposed to exhibit the symmetrical characteristics [2].

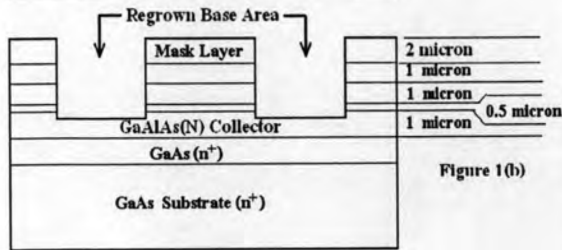
Mesa structures are essentially required to realize these transistors. This is because the collector, base and emitter epilayers are sequentially grown and then contacted by sequential etched. This structure is certainly physically asymmetric. Recently, the Zn doped planar structures have been used to obtain the symmetrical DHBTs. Nevertheless, other problems emerged. The resulting leakage currents degraded the performance of the DHBTs [3]. Hence, the purpose of this study is to obtain a symmetrical emitter-collector DHBT with p^+ regrown base. These designed structures can be developed not only to the symmetrical transistors but also the collector-up transistor structures. Moreover, these transistor structures with regrown base lead to an extremely low base resistance and result in high maximum frequency response.

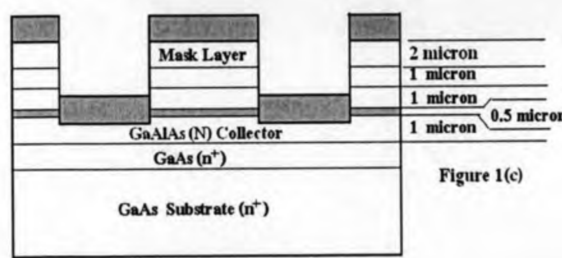
2. Device Fabrication

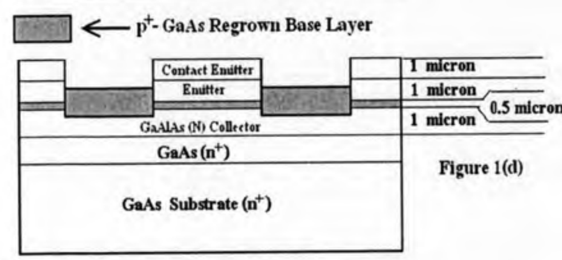
The symmetrical GaAlAs/GaAs DHBT structure, which has been prepared by Liquid Phase Epitaxy(LPE) supercooling technique, is composed of a buffer layer, a collector layer, a base layer, an emitter layer, a contact emitter layer and a mask layer on n^+- GaAs substrate. A detailed layer description of DHBT is summarized in Table 1 and shown schematically in Figure 1(a). The aluminium contents both in emitter and collector layers were fixed at 0.2 to reduce the influence of spike at each heterojunction in reverse bias condition [3]. After growth, the external base area was defined onto the sample by etching down to in between N-GaAlAs collector layer (Fig. 1(b)). The wafer was then reloaded in the LPE furnace to grow the p^+-GaAs external base layer. The surface of the regrown base layer within the defined regrown base area should be in between N-GaAlAs emitter layer (Fig. 1(c)). After second growth, the intrinsic emitter-base junction area was defined by etching the p^+-GaAs regrown base and GaAlAs mask layer deep to the n^+-GaAs contact emitter (Fig. 1(d)). Next, the emitter, collector and base ohmic contacts were performed and finally, the devices were isolated. All transistor sequence processes are shown in Figure 1. **Table 1.** Detail layer description of transistor.

Layer	Composition	Thickness (μm)	Doping Concentration (cm^{-3})
Mask	N-$Ga_{0.6}Al_{0.4}As$	2	-
Contact Emitter	n^+-GaAs	1	10^{19}
Emitter	N-$Ga_{0.8}Al_{0.2}As$	1	5.10^{17}
Base	p^+-GaAs	0.5	5.10^{18}
Collector	N-$Ga_{0.8}Al_{0.2}As$	1	5.10^{17}
Buffer	n^+-GaAs	2	10^{19}









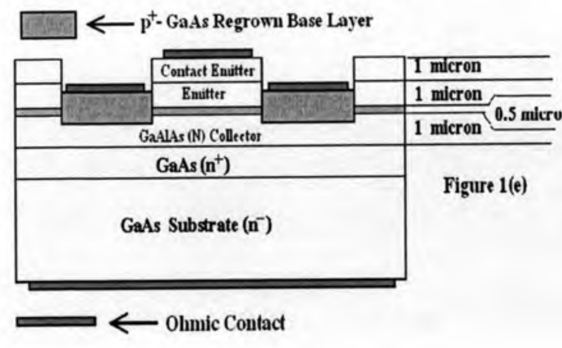


Figure 1. Schematic transistor sequence processes (a) LPE epitaxial layers. (b) Define the regrown base area. (c) Regrow the p^+-GaAs base layer. (d) Define the intrinsic emitter-base area and uncover the contact emitter. (e) Ohmic contact formation

3. Experimental Results

The current voltage characteristics both in normal mode and inverted mode of sample ST51, ST52 and ST53 are shown in Figure 2, 3 and 4, respectively. Every (I,V) characteristic was asymmetric between both modes. Figure 5 is the enlarged normal mode characteristic of sample ST51, whereas Figure 6 is the enlarged inverted mode of sample ST52. All normal mode characteristics were essentially parallel with the voltage axis, resulting in very high values for the Early voltage, meanwhile, some inverted modes had knee-shape characteristic, as clearly seen in Figure 4. The offset voltage of most transistors was 200 mV. The gains of different transistors are summarized in Table 2.

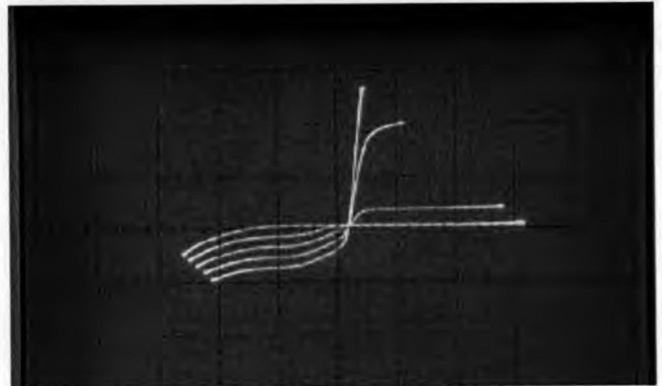


Figure 2. Current-voltage characteristic of ST51
$I_C(I_E)$: 2 mA/div, V_{CE}: 1 volt/div, I_B: 50 μA/step

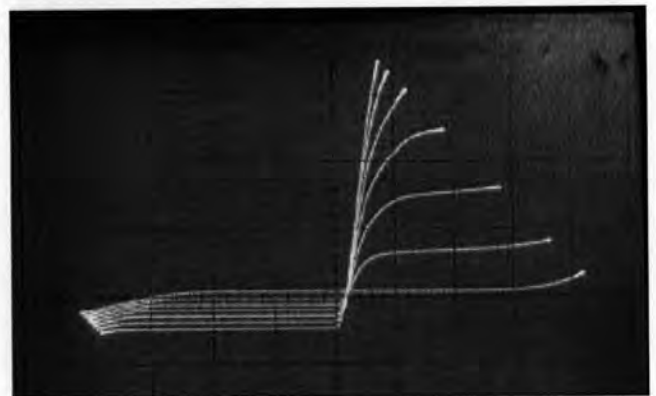


Figure 3. Current-voltage characteristic of ST52
$I_C(I_E)$: 2 m A/div, V_{CE}: 1 volt/div, I_B: 50 μA/step

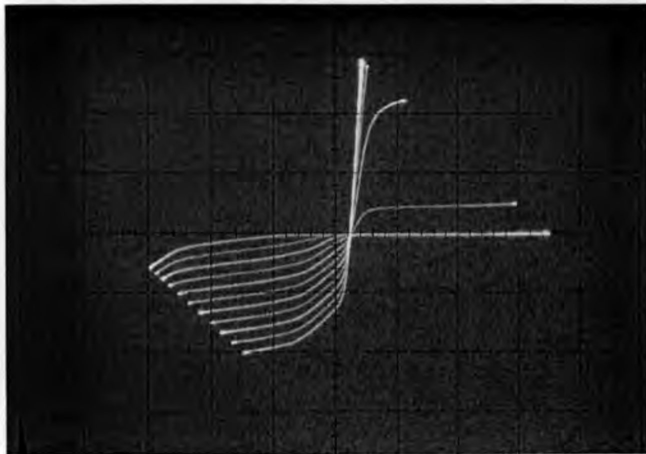


Figure 4. Current-voltage characteristic of ST53 with knee-shape inverted mode $I_C(I_E)$: 2 mA/div, V_{CE}: 1 volt/div, I_B: 100 μA/step

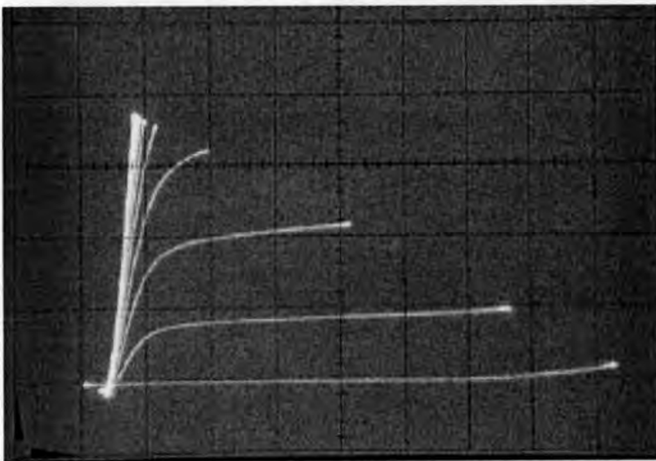


Figure 5 Normal mode current-voltage Characteristic of ST51, I_C: 2 mA/div, V_{CE}: 0.5 volt/div, I_B: 50 μA/step

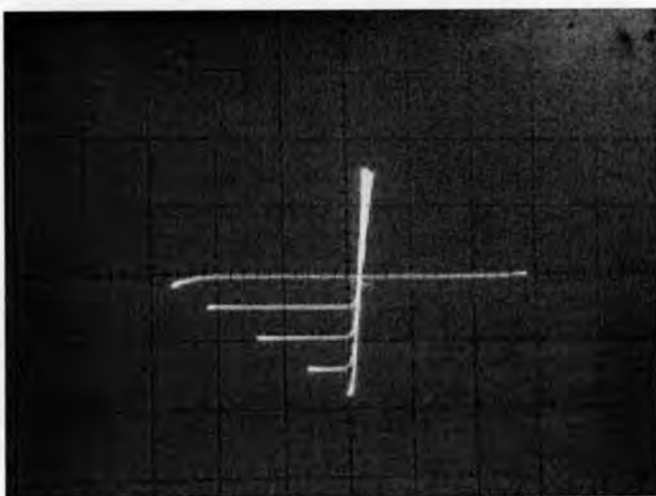


Figure 6. Inverted mode current-voltage characteristic of ST52, I_E: 1 mA/div, V_{CE}: 1 volt/div, I_B: 100 μA/step

Table 2. Normal mode and inverted mode gains

Transistor	Normal mode Gain at (I_C,V_{CE})	Inverted mode Gain at (I_E,V_{CE})
ST51	40 (2 mA,1V)	8 (1mA,1V)
ST52	30 (5 mA,2V)	5 (1 mA,2 V)
ST53	20 (4 mA,1V)	4 (4 mA,1V)

4. Discussion

All (I,V) characteristics were asymmetric. The normal mode gains were approximately 5 to 6 times higher than that of inverted mode for almost transistors, even though the same composition and carrier concentration of emitter and collector were used. This is because the physical structure of these transistors is asymmetric, as clearly seen in Figure 7. In inverted mode, collector-base junction is forward biased. As a result, collector (behaves as emitter) injects electrons both in internal and external base area. Most of electrons injected outside the intrinsic emitter-base junction are mainly lose due to recombination, result in lower gains. Moreover, for defining the regrown base area, the etching depth has to be precisely controlled in between the N- GaAlAs collector layer, as shown schematically in Figure 1(e). In case of etching beyond the bottom of collector layer, deep to the n^+ buffer layer, as shown schematically in Figure 8, the regrown base layer will form p^+-GaAs/ n^+-GaAs homojunction in the external base area. In inverted mode, this homojunction will perform as emitter-base junction parallel to that of collector-base heterojunction. Since, the energy barrier against injected holes of homojunction is lower than that of heterojunction.

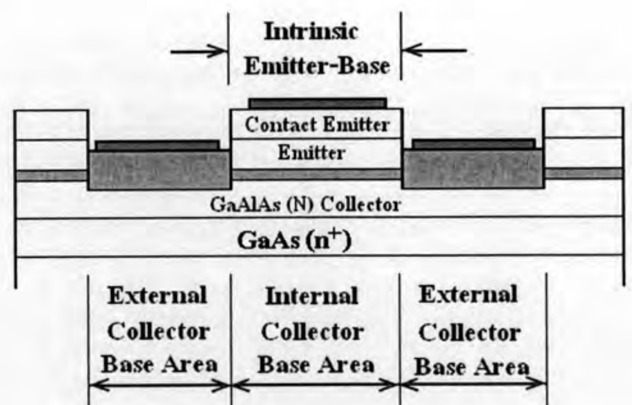


Figure 7. Physical structure of designed transistor, showing the external and internal collector-base areas

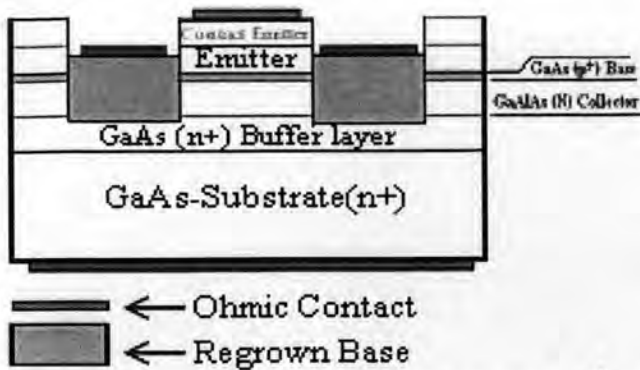


Figure 8. Define the regrown base area deep to the n^+-GaAs buffer layer

These transistors therefore effectively behave as a homojunction bipolar transistor with lower injection efficiency, result in lower gain. Furthermore, the spike at emitter-base heterojunction affects the collection of carriers as indicated by the knee-shape characteristic of Figure 4. In addition, the asymmetry between modes can be supported by the difference between the (I,V) characteristic of emitter-base and collector-base junctions with the third terminal opened, as shown in Figure 9. The differential between two (I,V) curves at a fixed current contribute to the amount of offset voltage.

To improve inverted gains, we have to get rid off the electron injections of external collector-base junction by using the P^+-GaAlAs regrown base in place of p^+-GaAs one. The homojunction of P^+-GaAlAs/ N- GaAlAs in the external base area will suppress the electron injected from collector; consequently, a DHBT will perform symmetrically with very low offset voltage.

5. Conclusion

We have demonstrated how to fabricate GaAlAs/GaAs DHBTs with p^+-GaAs regrown base. LPE technique was used in two steps to grow both the main structure and the regrown base. DHBTs exhibited the asymmetric (I,V) characteristics. The normal mode characteristic was superior to one of inverted mode with offset voltage close to 200 mV. Finally, DHBTs with P^+-GaAlAs regrown base was proposed to obtain the symmetrical transistor structure.

Figure 9. (I,V) characteristics of emitter-base and collector-base junction with the third terminal opened I: 2 mA/div, V: 1 volt/div

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References

[1] H. Kroemer, "Heterostructure Bipolar Transistors and Integrated Circuits", Proc. IEEE, Vol. 70, 1982, pp. 13-25.

[2] J.P. Bailbe, A. Marty, G. Rey, J. Tasselli and A. Bouyahyaoui, "Electrical Behavior of Double Heterojunction NPN GaAlAs/GaAs/GaAlAs Bipolar Transistors", Solid State Electron., Vol. 28, No. 6, 1985, PP627-638.

[3] Y. Deesirapipat, S. Thainoi, S. Ratanathammaphan and C. Antarasena, "Simple Fabrication Technique of Symmetrical Emitter-Collector Zinc-doped Planar $Ga_{1-x}Al_xAs/GaAs/Ga_{1-y}Al_yAs$ Double Heterojunction Bipolar Transistors", JJAP Vol. 40, No. 4A, April 2001, pp. 2127-2131.

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