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4. Nicholas Tsoulfanidis. Measurement and detection of Radiation. University of Missouri, McGRAW-HILL BOOK COMPANY ROLLA, 1983.
5. Texas Instrument. Understanding Data Converters. USA, 1995.
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ภาคผนวก

ภาคผนวก ก.

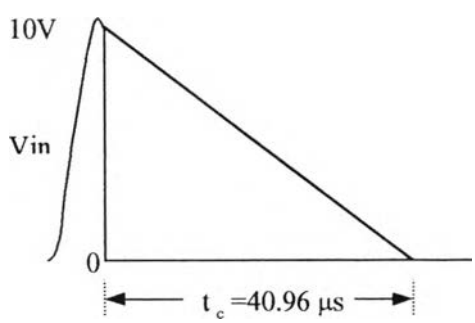
ก.1 การคำนวณค่าความต้านทาน V_{R5}, V_{R6}, V_{R7} และ V_{R8} เพื่อ ปรับค่า conversion gain ของ ADC แต่ละชุด (อ้างอิงลำดับอุปกรณ์ใน รูปที่ 3.4 sheet 1 of 8)

อัตราการลดลงของกระแส (current rampdown) หาได้จากการลดปริมาณประจุบน C1 ผ่านวงจรแหล่งจ่ายกระแสคงที่

$$I_{discharge} = \frac{Q}{t} \qquad \text{.....ก.1}$$

วงจร ADC นี้กำหนดให้ การแปลงผันสัญญาณทางเข้าสูงสุดที่ 10 V และจำนวนช่องวิเคราะห์เท่ากับ 4096 ช่อง โดยใช้ความถี่นาฬิกา 100 MHz

ดังนั้น $t_c = \frac{1}{f} \times n = \frac{1}{100 \times 10^6} \times 4096 = 40.96 \ \mu s$



จากสมการ ก.1 ; $Q = Vin\ C1 = 10 \times (500 \times 10^{-12})$

$= 5 \times 10^{-9}$ C

$$I_{discharge} = \frac{Q}{t} = \frac{5 \times 10^{-9}}{40.96 \times 10^{-6}} = 1.22 \times 10^{-4} \ A$$

ที่วงจรจ่ายกระแสคงที่ ; $I_{RL} = \frac{V_{ref}}{R_L}$, ซึ่ง R_L ในที่นี้คือ V_{R5} , $I_{RL} = I_{discharge}$, $V_{ref} = 5$ V

ดังนั้น $V_{R5} = \frac{V_{ref}}{I_{discharge}} = \frac{5}{1.22 \times 10^{-4}} = 40.98 \ k\Omega$

V_{R5} เลือกที่ปรับค่าได้ละเอียด (multiturns) = 100 kΩ

ก.2 รายละเอียดการทำงานของ ADC model 8706 ของ CANBERRA.

กำหนดระดับสถานะของสัญญาณเป็นดังนี้

ลักษณะสถานะของสัญญาณทั้ง อินพุตและ เอาท์พุต เป็นสัญญาณ TTL

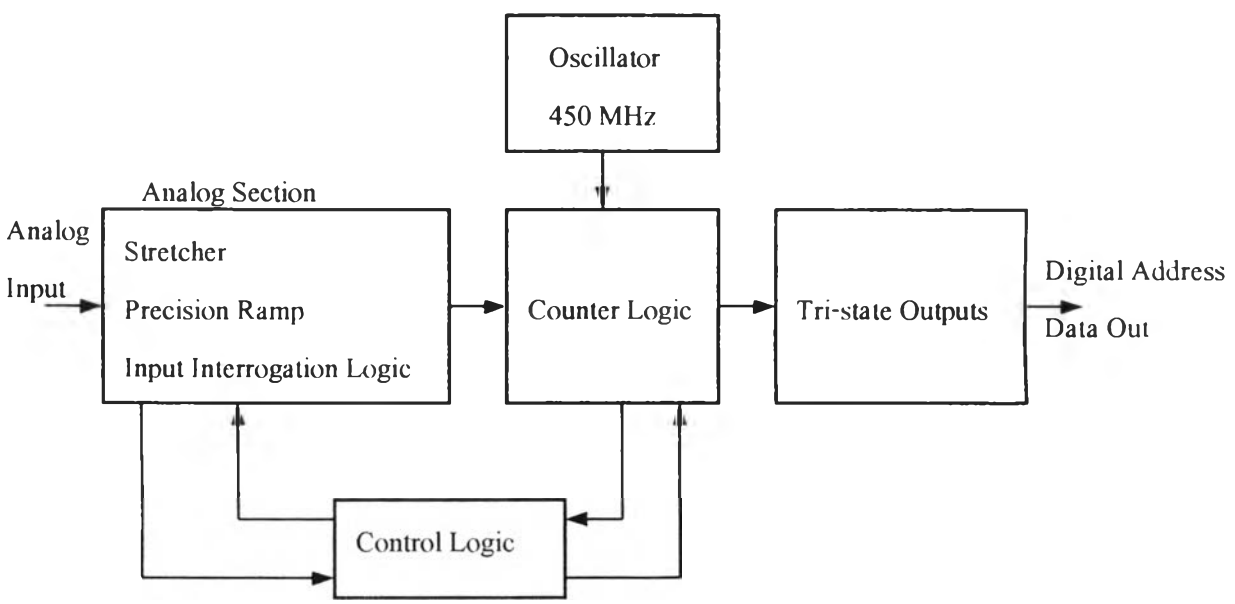
ระดับสัญญาณอินพุต Low = 0 to 1.0 volts

High = 2.0 to 5.0 volts

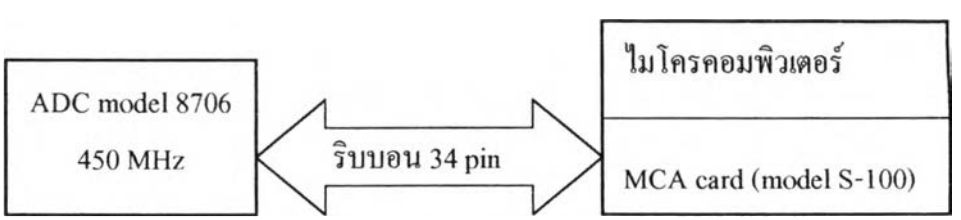
ระดับสัญญาณเอาท์พุต Low = 0 to 0.5 volts

High = 3.0 to 5.0 volts

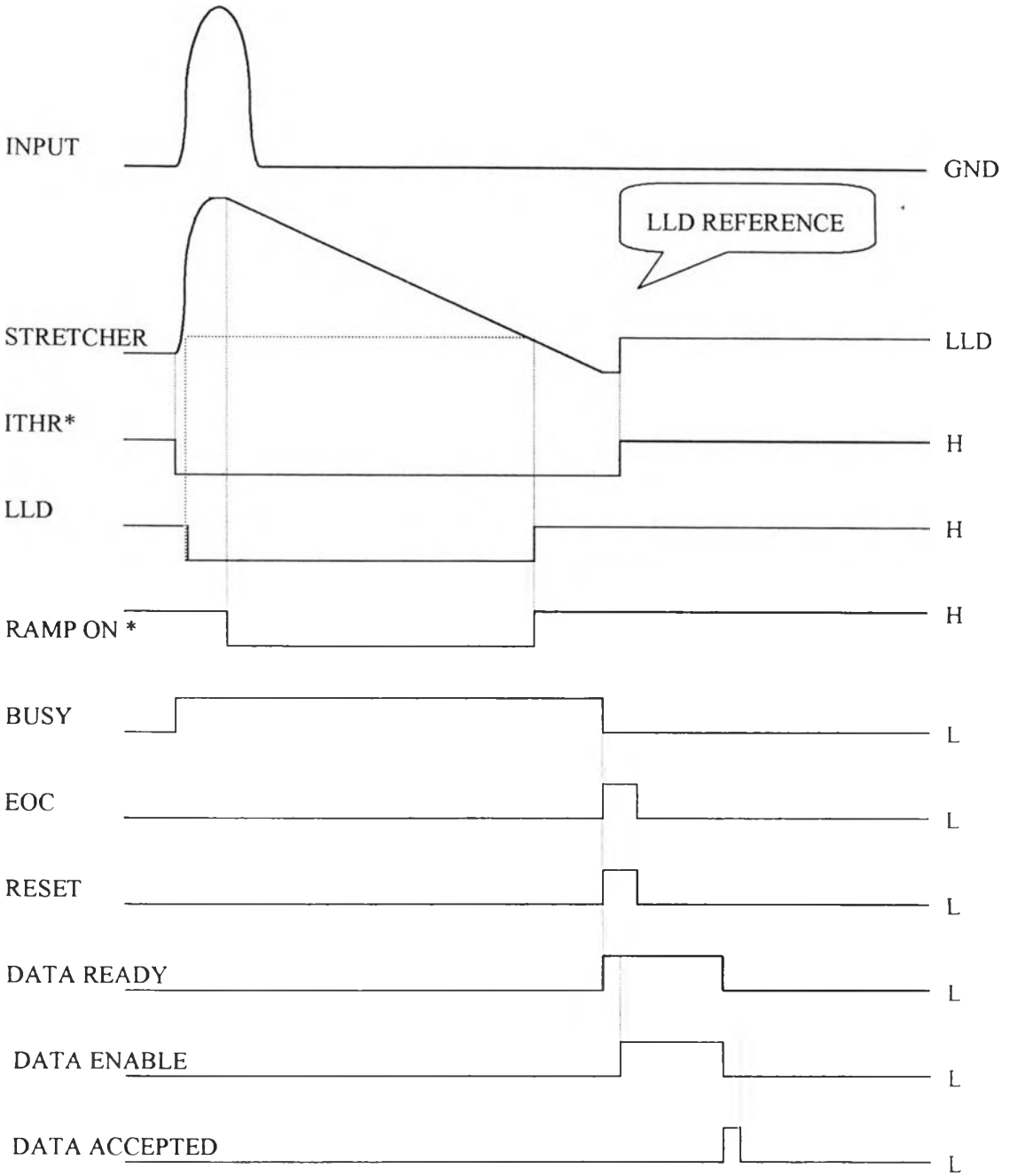
สัญญาณ อินพุตและเอาท์พุตให้ ลอจิก 1 คือ ระดับสัญญาณเป็น High ถ้ามีสัญลักษณ์ (*) ตามท้าย ลอจิก 1 คือระดับสัญญาณเป็น Low



รูปที่ ก.1 แผนภาพการทำงานของ ADC model 8706



รูปที่ ก.2 แผนภาพการติดต่อเชื่อมโยงระหว่าง ADC model 8706 กับ S-100 MCA



รูปที่ ก.3 แผนภาพเวลาการทำงานของ ADC model 8706

FAIRCHILD SEMICONDUCTOR TM

August 1984
Revised April 1999

MM74HC4066
Quad Analog Switch

General Description

The MM74HC4066 devices are digitally controlled analog switches utilizing advanced silicon-gate CMOS technology. These switches have low "ON" resistance and low "OFF" leakages. They are bidirectional switches, thus any analog input may be used as an output and visa-versa. Also the MM74HC4066 switches contain linearization circuitry which lowers the "ON" resistance and increases switch linearity. The MM74HC4066 devices allow control of up to 12V (peak) analog signals with digital control signals of the same range. Each switch has its own control input which disables each switch when LOW. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

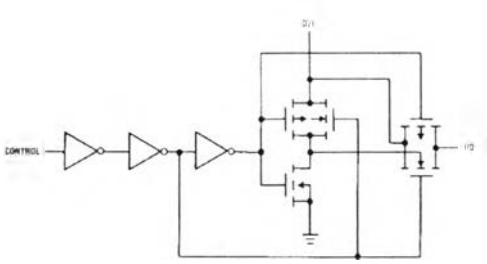
- Typical switch enable time: 15 ns
- Wide analog input voltage range: 0–12V
- Low "ON" resistance: 30 typ. (MM74HC4066)
- Low quiescent current: 80 μA maximum (74HC)
- Matched switch characteristics
- Individual switch controls

Ordering Code:

Order Number	Package Number	Package Description
MM74HC4066M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
MM74HC4066WM	M14B	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC4066SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4066MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC4066N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

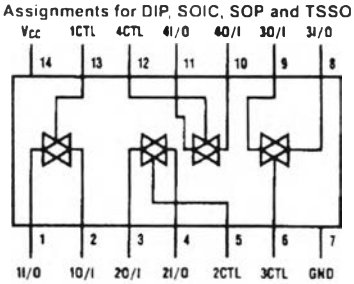
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Schematic Diagram



Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Top View

Truth Table

Input	Switch
CTL	I/O–O/I
L	"OFF"
H	"ON"

Absolute Maximum Ratings(Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +15V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Switch I/O Voltage (V_{IO})	V_{EE}−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	12	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 9.0V		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			9.0V		6.3	6.3	6.3	V
			12.0V		8.4	8.4	8.4	V
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			9.0V		2.7	2.7	2.7	V
			12.0V		3.6	3.6	3.6	V
R_{ON}	Maximum "ON" Resistance (Note 5)	V_{CTL} = V_{IH}, I_S = 2.0 mA V_{IS} = V_{CC} to GND (Figure 1)	4.5V	100	170	200	220	Ω
			9.0V	50	85	105	110	Ω
			12.0	30	70	85	90	Ω
		V_{CTL} = V_{IH}, I_S = 2.0 mA V_{IS} = V_{CC} or GND (Figure 1)	2.0V	120	180	215	240	Ω
			4.5V	50	80	100	120	Ω
			9.0V	35	60	75	80	Ω
			12.0V	20	40	60	70	Ω
R_{ON}	Maximum "ON" Resistance Matching	V_{CTL} = V_{IH} V_{IS} = V_{CC} to GND	4.5V	10	15	20	20	Ω
			9.0V	5	10	15	15	Ω
			12.0V	5	10	15	15	Ω
I_{IN}	Maximum Control Input Current	V_{IN} = V_{CC} or GND V_{CC} = 2–6V			±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current	V_{OS} = V_{CC} or GND V_{IS} = GND or V_{CC} V_{CTL} = V_{IL} (Figure 3)	6.0V	10	±60	±600	±600	nA
			9.0V	15	±80	±800	±800	nA
			12.0V	20	±100	±1000	±1000	nA
I_{IZ}	Maximum Switch "ON" Leakage Current	V_{IS} = V_{CC} to GND V_{CTL} = V_{IH} V_{OS} = OPEN (Figure 2)	6.0V	10	±40	±150	±150	nA
			9.0V	15	±50	±200	±200	nA
			12.0V	20	±60	±300	±300	nA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA
			9.0V		4.0	40	80	μA
			12.0V		8.0	80	160	μA

Note 4: For a power supply of 5V ±10% the worst case on resistance (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages (V_{CC}–GND) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics

V_{CC} = 2.0V–6.0V V_{EE} = 0V–12V, C_L = 50 pF (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C		Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation		2.0V	25	50	30	75	ns
	Delay Switch In to Out		4.5V	5	10	13	15	ns
			9.0V	4	8	10	12	ns
			12.0V	3	7	11	13	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn	R_L = 1 kΩ	2.0V	30	100	125	150	ns
	"ON" Delay		4.5V	12	20	25	30	ns
			9.0V	6	12	15	18	ns
			12.0V	5	10	13	15	ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn	R_L = 1 kΩ	2.0V	60	168	210	252	ns
	"OFF" Delay		4.5V	25	36	45	54	ns
			9.0V	20	32	40	48	ns
			12.0V	15	30	38	45	
f_{MAX}	Minimum Frequency	R_L = 600Ω	4.5V	40				MHz
	Response (Figure 7)	V_{IS} = 2 V_{PP} at (V_{CC}/2)	9.0V	100				MHz
	20 log (V_O/V_I) = −3 dB	(Note 6) (Note 7)						
	Crosstalk Between	R_L = 600Ω, F = 1 MHz						
	any Two Switches	(Note 7) (Note 8)	4.5V	−52				dB
	(Figure 8)		9.0V	−50				dB
	Peak Control to Switch	R_L = 600Ω, F = 1 MHz	4.5V	100				mV
	Feedthrough Noise (Figure 9)	C_L = 50 pF	9.0V	250				mV
	Switch OFF Signal	R_L = 600Ω, F = 1 MHz						
	Feedthrough	$V_{(CT)}V_{IL}$						
	Isolation	(Note 7) (Note 8)	4.5V	−42				dB
	(Figure 10)		9.0V	−44				dB
THD	Total Harmonic	R_L = 10 kΩ, C_L = 50 pF,						
	Distortion	F = 1 kHz						
	(Figure 11)	V_{IS} = 4 V_{PP}	4.5V	.013				%
		V_{IS} = 8 V_{PP}	9.0V	.008				%
C_{IN}	Maximum Control			5	10	10	10	pF
	Input Capacitance							
C_{IN}	Maximum Switch			20				pF
	Input Capacitance							
C_{IN}	Maximum Feedthrough	V_{CTL} = GND		0.5				pF
	Capacitance							
C_{PD}	Power Dissipation			15				pF
	Capacitance							

Note 6: Adjust 0 dBm for F = 1 kHz (Null R_L/R_{ON} Attenuation)

Note 7: V_{IS} is centered at $V_{CC}/2$

Note 8: Adjust input for 0 dBm

AC Test Circuits and Switching Time Waveforms

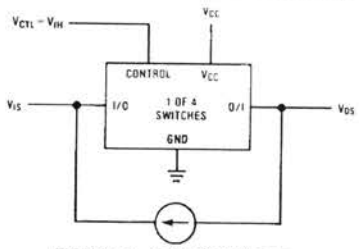


FIGURE 1. "ON" Resistance

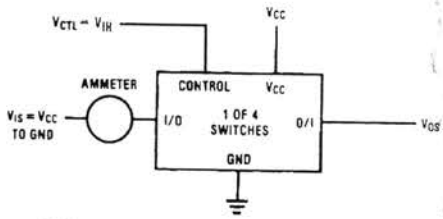


FIGURE 2. "ON" Channel Leakage Current

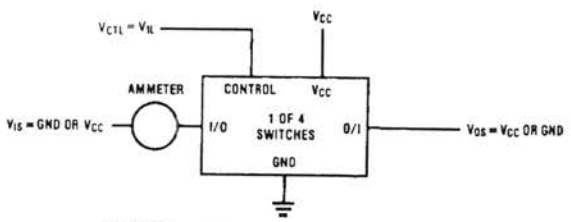


FIGURE 3. "OFF" Channel Leakage Current

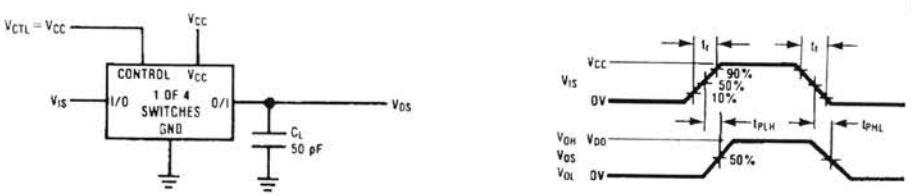


FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

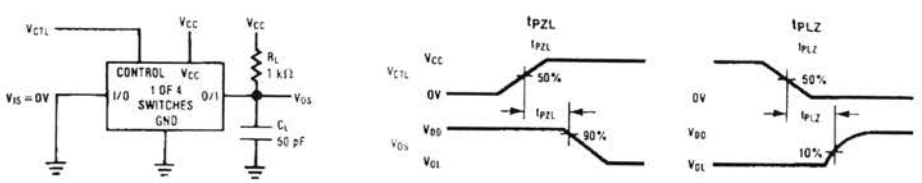


FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

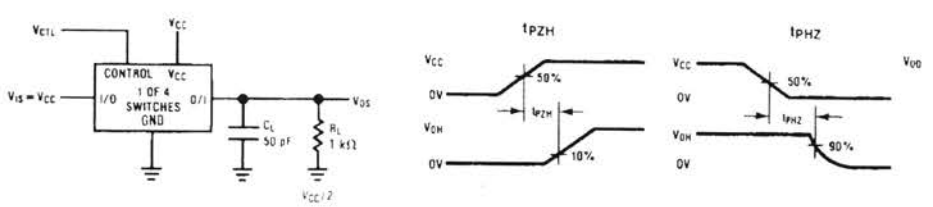


FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

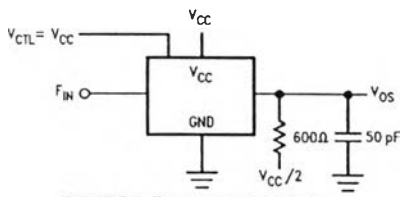


FIGURE 7. Frequency Response

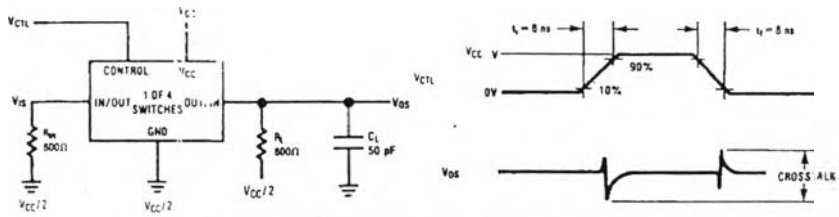


FIGURE 8. Crosstalk: Control Input to Signal Output

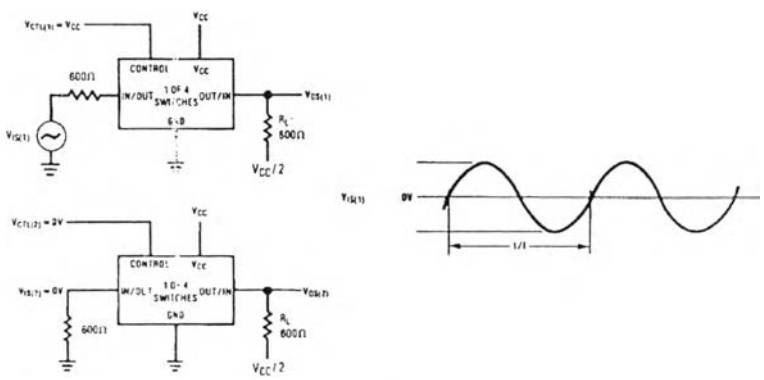


FIGURE 9. Crosstalk Between Any Two Switches

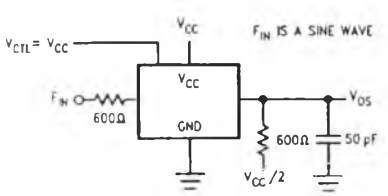


FIGURE 10. Switch OFF Signal Feedthrough Isolation

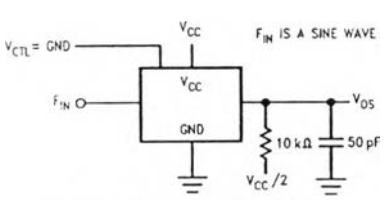
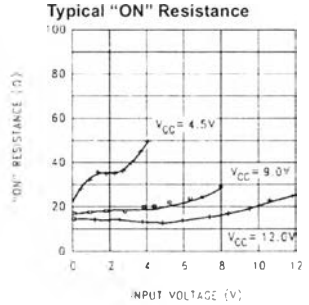


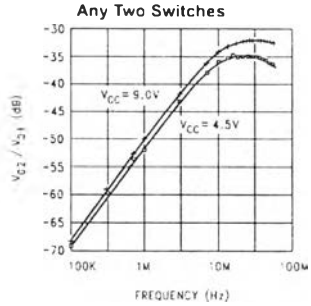
FIGURE 11. Sinewave Distortion

Typical Performance Characteristics

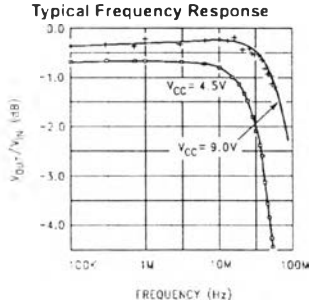
Typical "ON" Resistance



Typical Crosstalk Between Any Two Switches



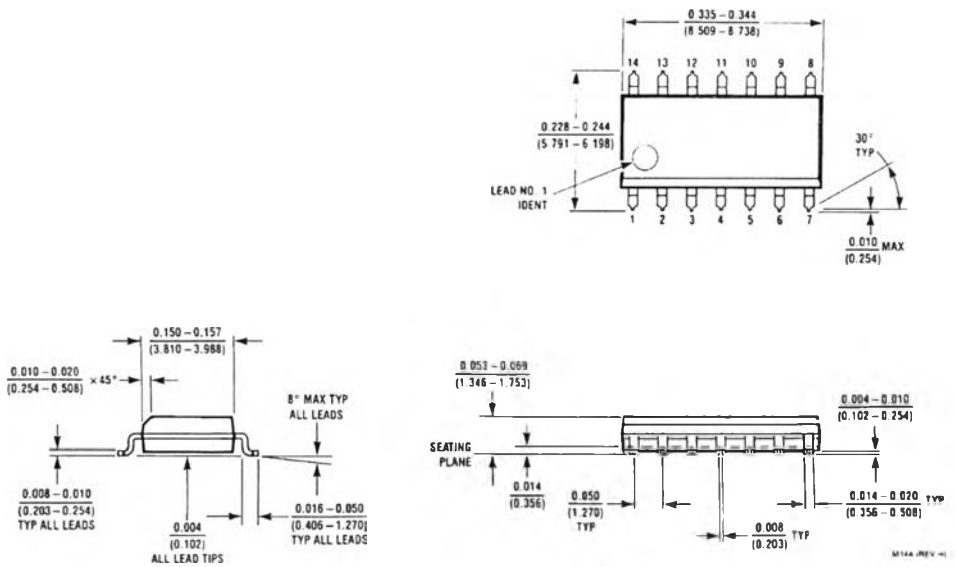
Typical Frequency Response



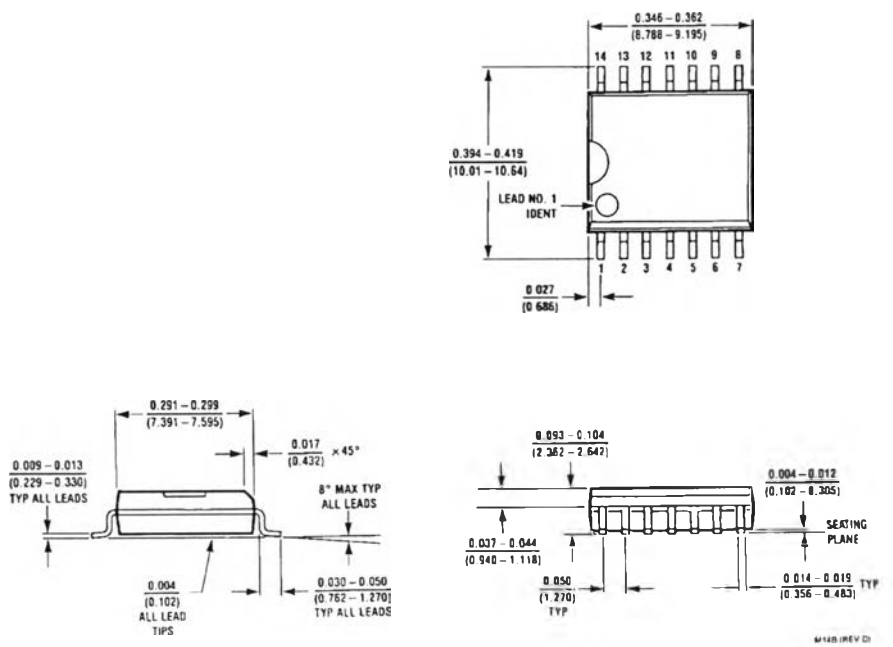
Special Considerations

In certain applications the external load-resistor current may include both V_{CC} and signal line components. To avoid drawing V_{CC} current when switch current flows into the analog switch input pins, the voltage drop across the switch must not exceed 0.6V (calculated from the ON resistance).

Physical Dimensions inches (millimeters) unless otherwise noted

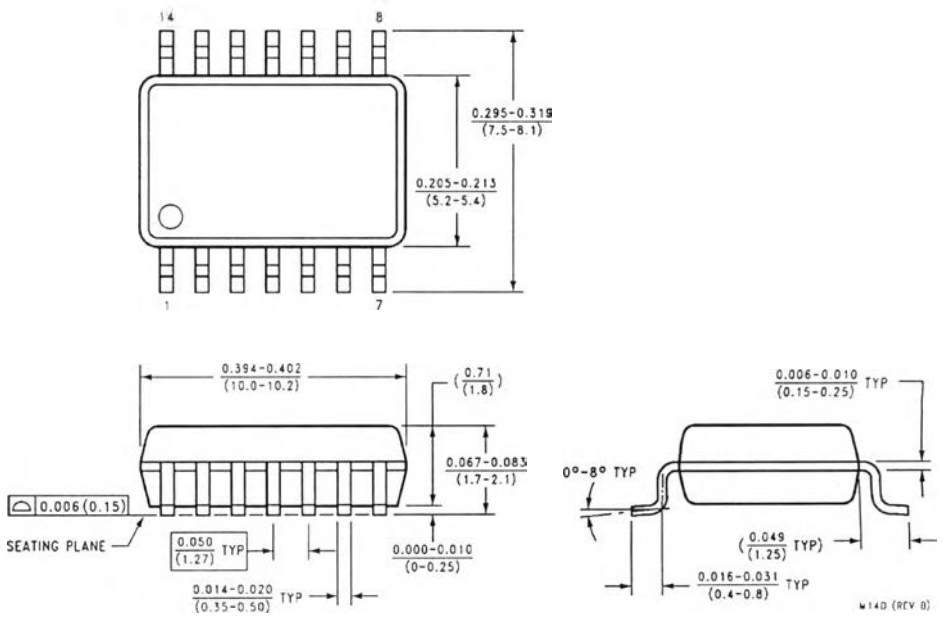


14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
Package Number M14A



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M14B

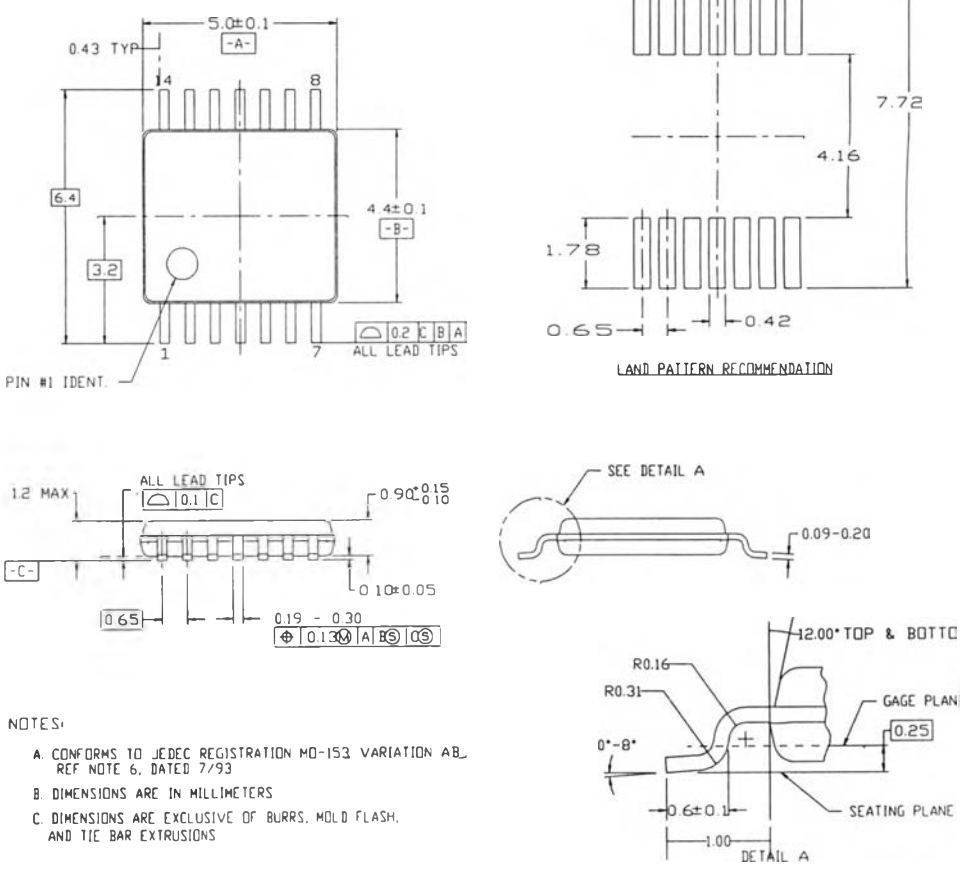
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

14LD, TSSOP, JEDEC MO-153, 4.4MM WIDE



NOTES:

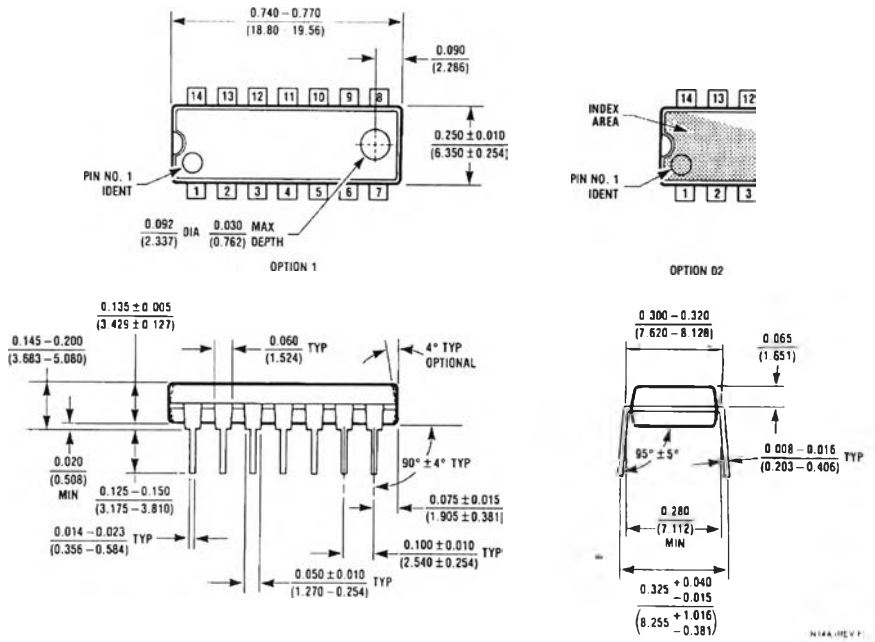
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

Analog Switch
Definition of Terms

R_{ON}: Resistance between the output and the input of an addressed channel.

I_S: Current at any switch input. This is leakage current when the switch is ON.

I_D: Current at any switch input going into the switch. This is leakage current when the switch is OFF.

C_S: Capacitance between any open terminal "S" and ground.

C_D: Capacitance between any open terminal "D" and ground.

I_D–I_S: Leakage current that flows from the closed switch into the body. This leakage is the difference between the current I_D going into the switch and the current I_S going out of the switch.

t_{RAN}: Delay time when switching from one address state to another.

t_{ON}: Delay time between the 50% points of an enable input and the switch ON condition.

t_{OFF}: Delay time between the 50% points of the enable input and the switch OFF condition.

National Semiconductor

Analog Switch/Multiplexer Selection Guide

Part Number	Function	Logic Input	V_S (Typ)	T_{ON}/T_{OFF} ns (Typ)	R_{ON} Ω
AH0014	DPDT	TTL, DTL	+10/−22	350/600	75
AH0015	QUAD SPST	TTL, DTL	+10/−22	100/600	75
AH0019	DUAL DPST	TTL, DTL	+10/−22	100/600	75
AH5011	QUAD SPST	TTL, CMOS	—	150/300	100
AH5012		TTL, CMOS	—	150/300	150
CD4016		CMOS	±7.5	20/40	850
CD4066		CMOS	±7.5	25/50	280
LF11201/LF13201		TTL	±15	90/500	200
LF11202/LF13202		TTL	±15	90/500	200
LF11331/LF13331		TTL	±15	90/500	200
LF11332/LF13332		TTL	±15	90/500	200
LF11333/LF13333		TTL	±15	90/500	200
MM74HC4016		CMOS	±12	5/8	40
AH5020	DUAL SPDT	TTL, CMOS	—	150/300	150
CD4053	TRIPLE SPDT	CMOS	±7.5	160/75	300
MM74HC4053		CMOS	±6.0	15/16	40
AH5009	4-CHANNEL	TTL, CMOS	—	150/300	100
AH5010		TTL, CMOS	—	150/300	150
CD4052	4-CHANNEL	CMOS	±7.5	160/75	300
CD4529B	DIFFERENTIAL	CMOS	±7.5	50	350
LF13509		TTL, CMOS	±18	1600/200	350
MM74HC4052		CMOS	±6.0	15/16	40
CD4051	8-CHANNEL	CMOS	±7.5	160/75	300
CD4529B		CMOS	±7.5	50	350
LF13508		TTL, CMOS	±18	1600/200	350
MM74HC4051		CMOS	±6.0	15/16	40

HARRIS SEMICONDUCTOR

HA-2520, HA-2522, HA-2525

20MHz, High Slew Rate, Uncompensated, High Input Impedance, Operational Amplifiers

November 1996

Features

- High Slew Rate 120V/µs
- Fast Settling 200ns
- Full Power Bandwidth 2MHz
- Gain Bandwidth ($A_V \geq 3$) 20MHz
- High Input Impedance 100MΩ
- Low Offset Current 10nA

Applications

- Data Acquisition Systems
- RF Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Description

HA-2520/2522/2525 comprise a series of operational amplifiers delivering an unsurpassed combination of specifications for slew rate, bandwidth and settling time. These dielectrically isolated amplifiers are controlled at close loop gains greater than 3 without external compensation. In addition, these high performance components also provide low offset current and high input impedance.

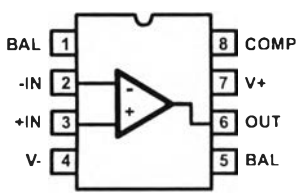
120V/µs slew rate and 200ns (0.2%) settling time of these amplifiers make them ideal components for pulse amplification and data acquisition designs. These devices are valuable components for RF and video circuitry requiring up to 20MHz gain bandwidth and 2MHz power bandwidth. For accurate signal conditioning designs the HA-2520/2522/2525's superior dynamic specifications are complemented by 10nA offset current, 100MΩ input impedance and offset trim capability. MIL-STD-883 product and data sheets are available upon request.

Ordering Information

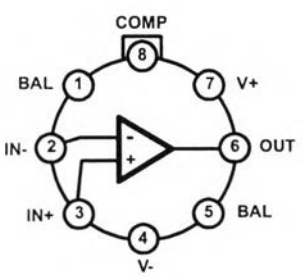
PART NUMBER (BRAND)	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HA2-2520-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-2522-2	-55 to 125	8 Pin Metal Can	T8.C
HA2-2525-5	0 to 75	8 Pin Metal Can	T8.C
HA3-2525-5	0 to 75	8 Ld PDIP	E8.3
HA4P2525-5	0 to 75	20 Ld PLCC	N20.35
HA7-2520-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-2522-2	-55 to 125	8 Ld CERDIP	F8.3A
HA7-2525-5	0 to 75	8 Ld CERDIP	F8.3A
HA9P2525-5 (H25255)	0 to 75	8 Ld SOIC	M8.15

Pinouts

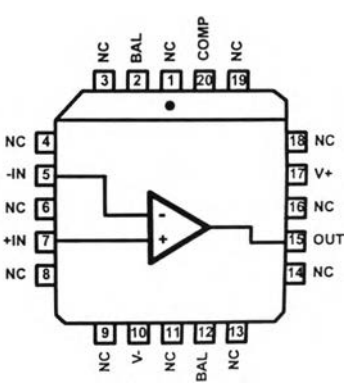
HA-2520/22 (CERDIP)
HA-2525 (PDIP, CERDIP, SOIC)
TOP VIEW



HA-2520/22/25
(METAL CAN)
TOP VIEW



HA-2525
(PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 2894.2

HA-2520, HA-2522, HA-2525

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) 40V
Differential Input Voltage 15V
Output Current 50mA

Operating Conditions

Temperature Range
HA-2520/2522-2 . . . . . -55°C to 125°C
HA-2525-5 . . . . . 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	165	80
PDIP Package	96	N/A
CERDIP Package	135	50
PLCC Package	74	N/A
SOIC Package	157	N/A

Maximum Junction Temperature (Hermetic Packages) . . . . . 175°C
Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC and PLCC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications $V_{SUPPLY} = \pm 15V$

PARAMETER	TEMP (°C)	HA-2520-2			HA-2522-2			HA-2525-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	25	-	4	8	-	5	10	-	5	10	mV
	Full	-	-	11	-	-	14	-	-	14	mV
Offset Voltage Drift	Full	-	20	-	-	25	-	-	30	-	µV/°C
Bias Current	25	-	100	200	-	125	250	-	125	250	nA
	Full	-	-	400	-	-	500	-	-	500	nA
Offset Current	25	-	10	25	-	20	50	-	20	50	nA
	Full	-	-	50	-	-	100	-	-	100	nA
Input Resistance (Note 2)	25	50	100	-	40	100	-	40	100	-	MΩ
Common Mode Range	Full	±10.0	-	-	±10.0	-	-	±10.0	-	-	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 3, 6)	25	10	15	-	7.5	15	-	7.5	15	-	kV/V
	Full	7.5	-	-	5	-	--	5	-	-	kV/V
Common Mode Rejection Ratio (Note 4)	Full	80	90	-	74	90	-	74	90	-	dB
Gain Bandwidth (Notes 2, 5)	25	10	20	-	10	20	-	10	20	-	MHz
Minimum Stable Gain	25	3	-	-	3	-	-	3	-	-	V/V
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 3)	Full	±10.0	±12.0	-	±10.0	±12.0	-	±10.0	±12.0	-	V
Output Current (Note 6)	25	±10	±20	-	±10	±20	-	±10	±20	-	mA
Full Power Bandwidth (Notes 6, 11)	25	1.5	2.0	-	1.2	2.0	-	1.2	2.0	-	MHz
TRANSIENT RESPONSE ($A_V = +3$)											
Rise Time (Notes 3, 7, 8, 10)	25	-	25	50	-	25	50	-	25	50	ns
Overshoot (Notes 3, 7, 8, 10)	25	-	25	40	-	25	50	-	25	50	%
Slew Rate (Notes 3, 7, 10, 12)	25	±100	±120	-	±80	±120	-	±80	±120	-	V/µs
Settling Time (Notes 3, 7, 10, 12)	25	-	0.20	-	-	0.20	-	-	0.20	-	µs

Electrical Specifications $V_{SUPPLY} = \pm 15V$ **(Continued)**

PARAMETER	TEMP (°C)	HA-2520-2			HA-2522-2			HA-2525-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS											
Supply Current	25	-	4	6	-	4	6	-	4	6	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90	-	74	90	-	74	90	-	dB

NOTES:

2. This parameter value is based on design calculations.
3. $R_L = 2k\Omega$.
4. $V_{CM} = \pm 10V$.
5. $A_V > 10$.
6. $V_O = \pm 10.0V$.
7. $C_L = 50pF$.
8. $V_O = \pm 200mV$.
9. $\Delta V = \pm 5.0V$.
10. See Transient Response Test Circuits and Waveforms.
11. Full Power Bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
12. $V_{OUT} = \pm 5V$.

Test Circuits and Waveforms

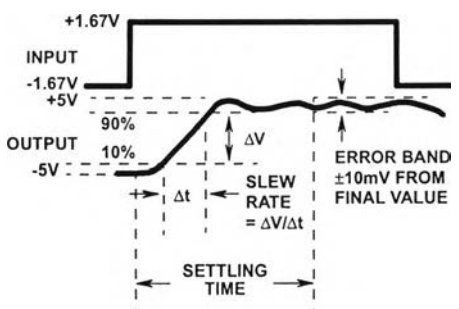
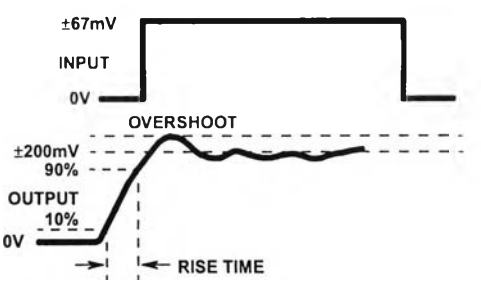


FIGURE 1. SLEW RATE AND SETTLING TIME



NOTE: Measured on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

FIGURE 2. TRANSIENT RESPONSE

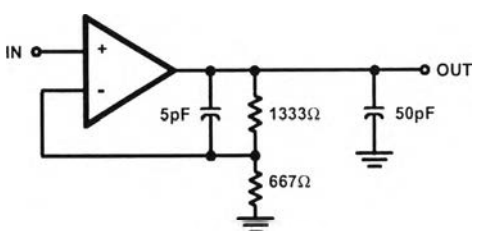
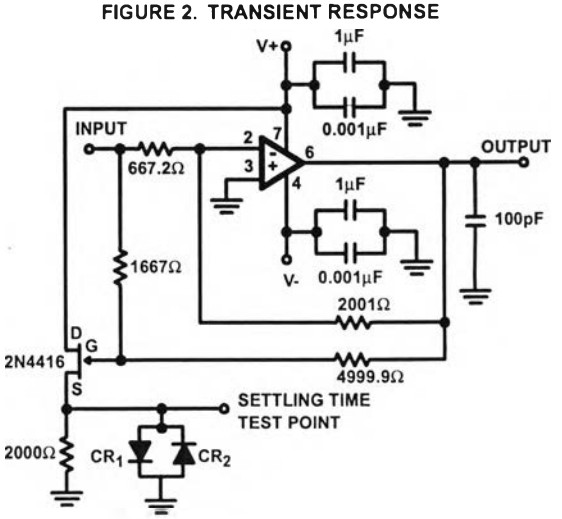


FIGURE 3. SLEW RATE AND TRANSIENT RESPONSE

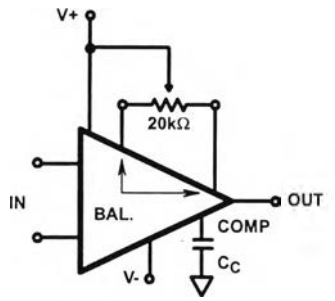


NOTES:

13. $A_V = -3$.
14. Feedback and summing resistor ratios should be 0.1% matched.
15. Clipping diodes CR_1 and CR_2 are optional. HP5082-2810 recommended.

FIGURE 4. SETTLING TIME TEST CIRCUIT

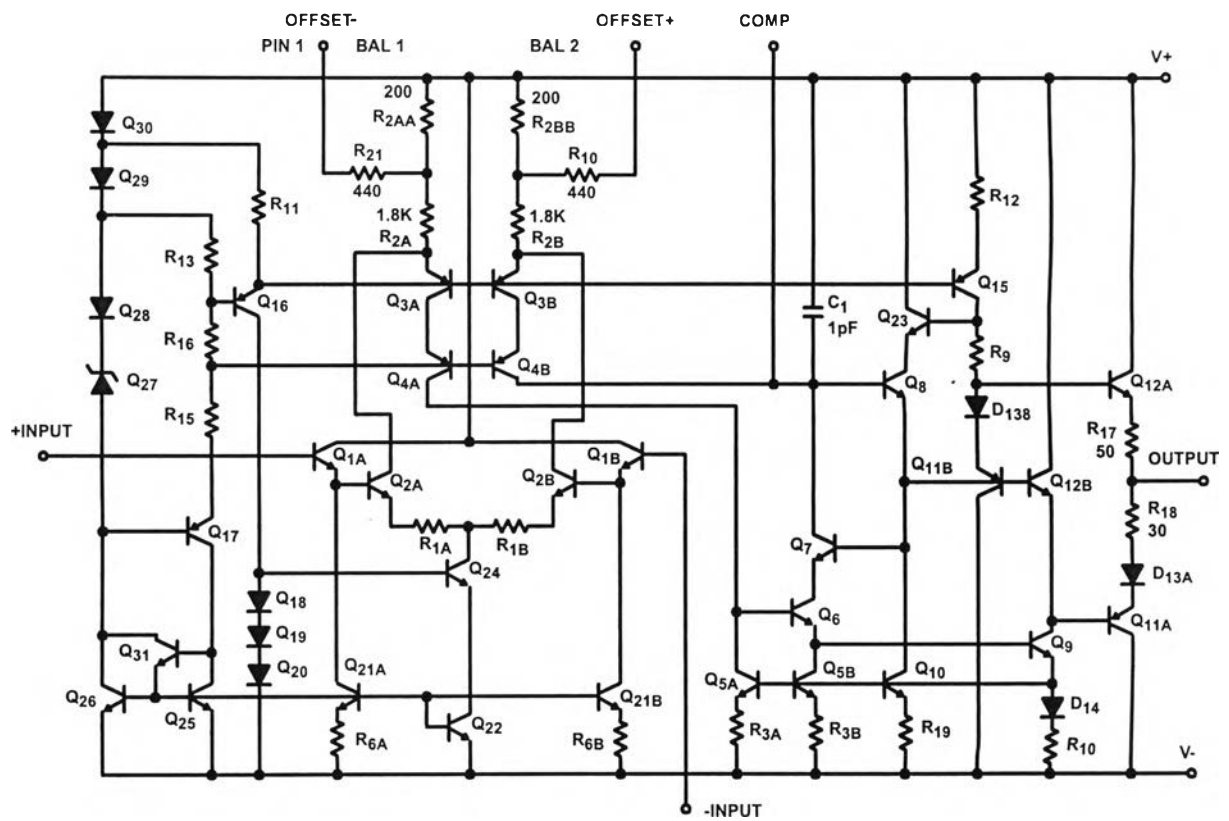
Test Circuits and Waveforms (Continued)



NOTE: Tested offset adjustment range is $|V_{OS} + 1mV|$ minimum referred to output. Typical ranges are ±20mV with $R_T = 20k\Omega$.

FIGURE 5. SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK-UP

Schematic Diagram



Inverting Unity Gain Circuit

Figure 6 shows a Compensation Circuit for an inverting unity gain amplifier. The circuit was tested for functionality with supply voltages from ±4V to ±15V, and the performance as tested was: Slew Rate ≈ 120V/µs; Bandwidth ≈ 10MHz; and Settling Time (0.1%) ≈ 500ns. Figure 7 illustrates the amplifier's frequency response, and it is important to note that capacitance at pin 8 must be minimized for maximum bandwidth.

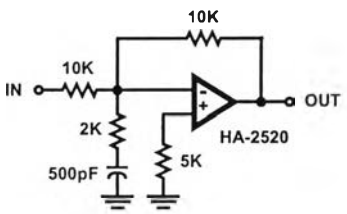


FIGURE 6. INVERTING UNITY GAIN CIRCUIT

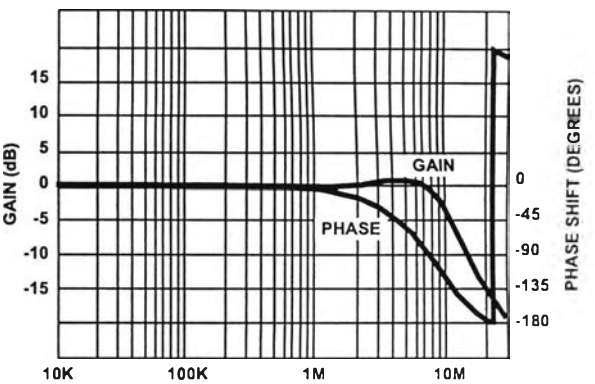


FIGURE 7. FREQUENCY RESPONSE FOR INVERTING UNITY GAIN CIRCUIT

Typical Performance Curves $V_S = \pm15V$, $T_A = 25^oC$, Unless Otherwise Specified

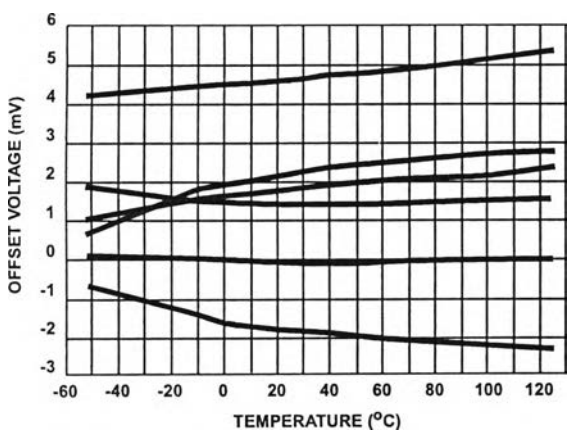


FIGURE 8. OFFSET VOLTAGE vs TEMPERATURE (6 TYPICAL UNITS FROM 3 LOTS)

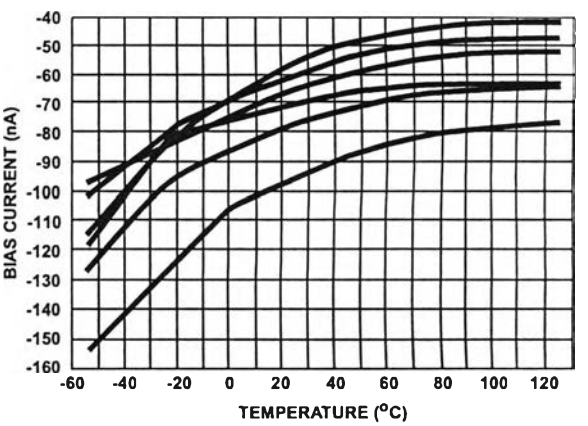


FIGURE 9. BIAS CURRENT vs TEMPERATURE (6 TYPICAL UNITS FROM 3 LOTS)

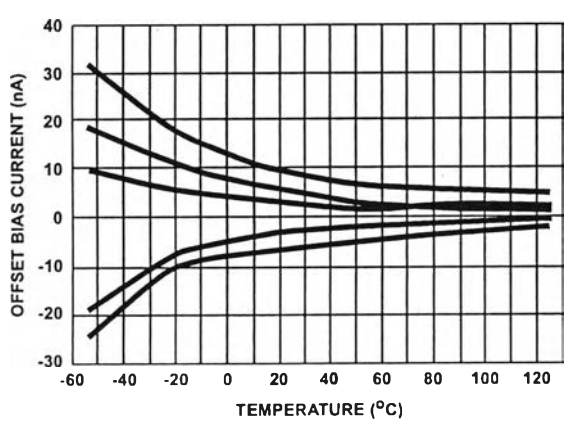


FIGURE 10. OFFSET CURRENT vs TEMPERATURE (5 TYPICAL UNITS FROM 3 LOTS)

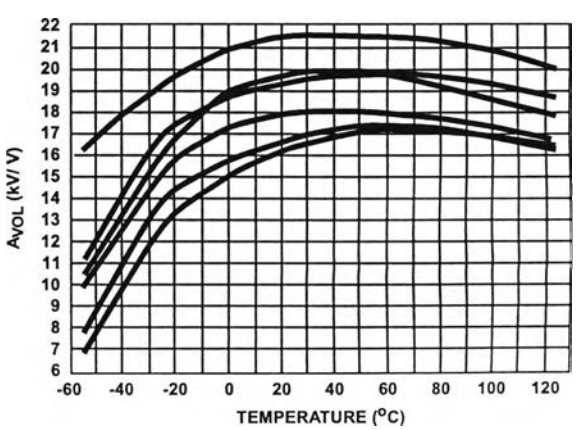


FIGURE 11. OPEN LOOP GAIN vs TEMPERATURE (6 TYPICAL UNITS FROM 3 LOTS)

V_S = ±15V, T_A = 25°C, Unless Otherwise Specified **(Continued)**

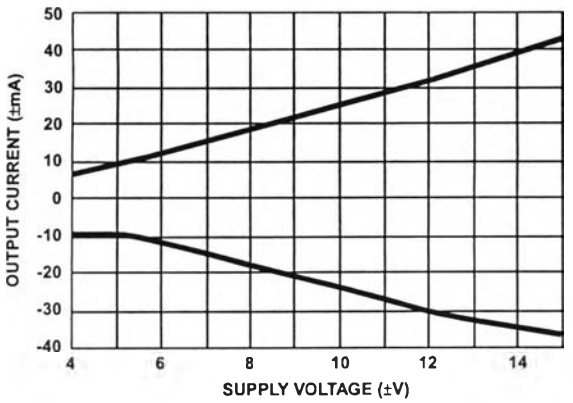


FIGURE 12. OUTPUT CURRENT vs SUPPLY VOLTAGE

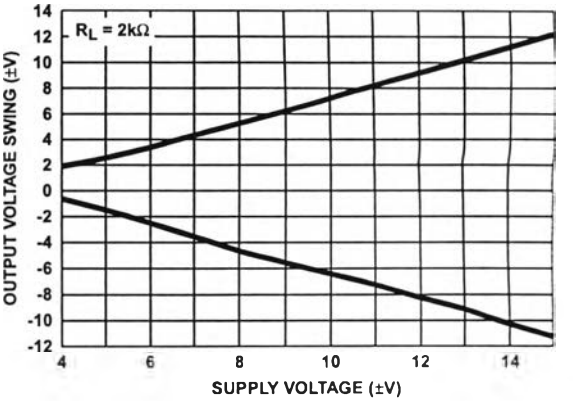


FIGURE 13. OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE

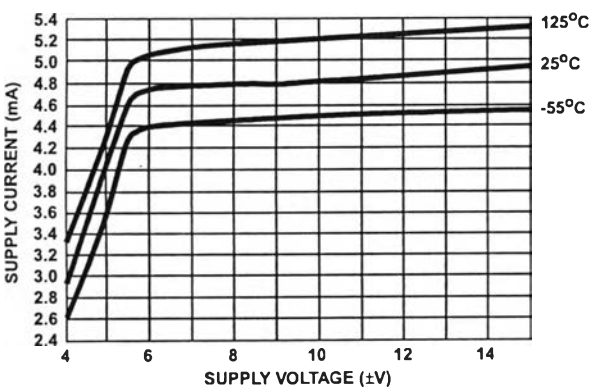


FIGURE 14. SUPPLY CURRENT vs SUPPLY VOLTAGE

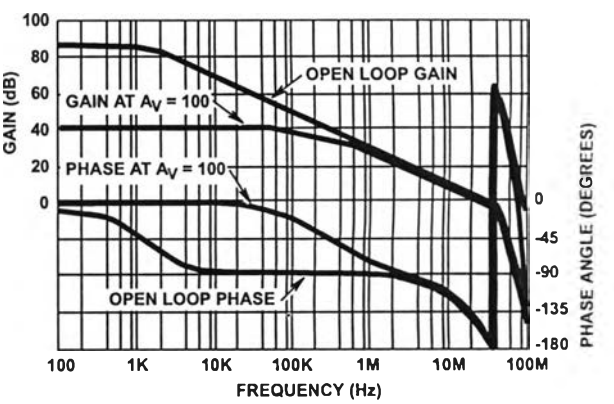


FIGURE 15. FREQUENCY RESPONSE

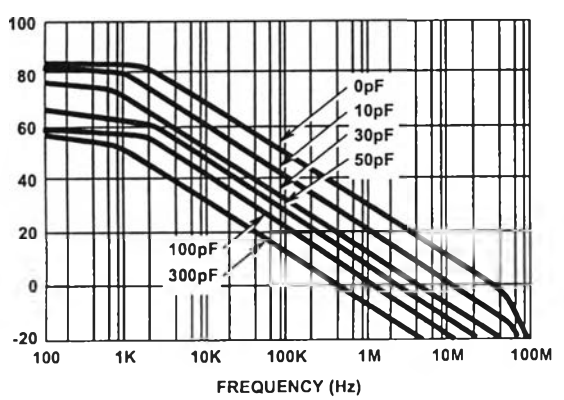


FIGURE 16. OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMP PIN TO GROUND

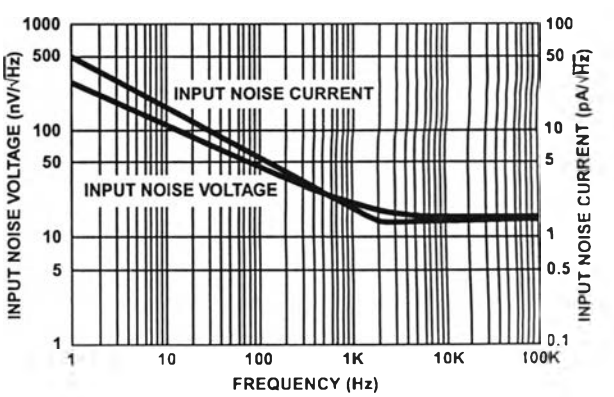


FIGURE 17. INPUT NOISE CHARACTERISTICS

V_S = ±15V, T_A = 25°C, Unless Otherwise Specified **(Continued)**

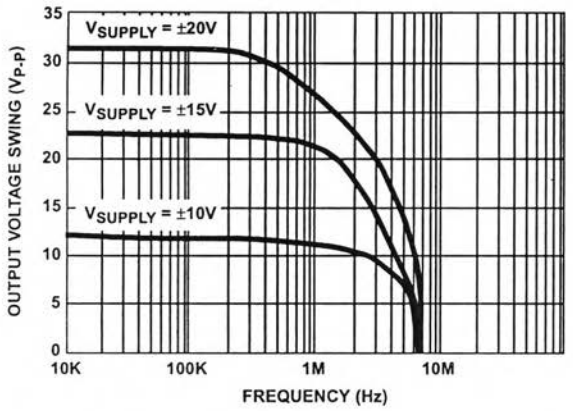


FIGURE 18. OUTPUT VOLTAGE SWING vs FREQUENCY

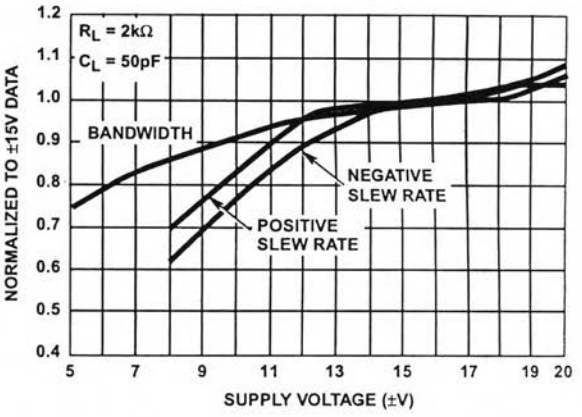


FIGURE 19. NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE

DIE DIMENSIONS:

67 mils x 57 mils x 19 mils
(1700µm x 1440µm x 483µm)

METALLIZATION:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

SUBSTRATE POTENTIAL:

Unbiased

PASSIVATION:

Type: Nitride (Si_3N_4) over Silox (SiO_2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

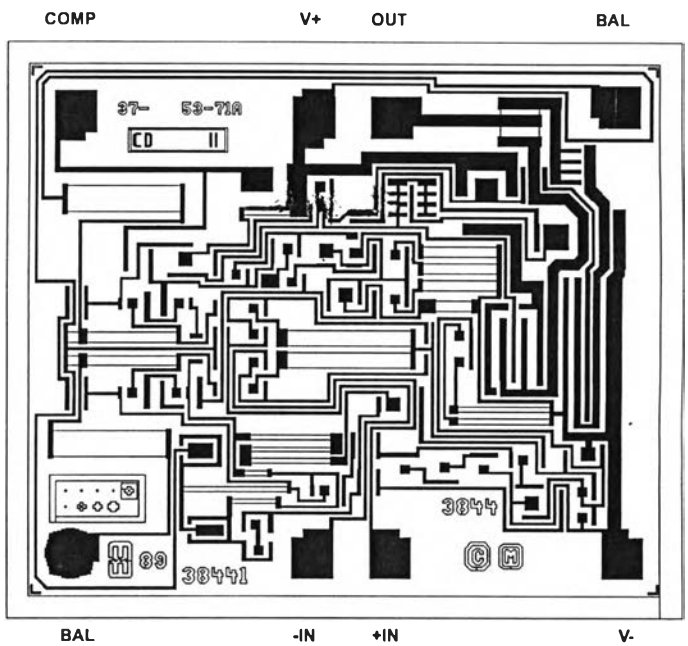
TRANSISTOR COUNT:

40

PROCESS:

Bipolar Dielectric Isolation

HA-2520, HA-2522, HA-2525



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QC-OS-14 Hcmos/TTL compatible oscillator

The QS- OS- 14 is a standa oscillator to drive Hcmos loads 10TTL gates. A tri- state enat function on pin 1 to facilatate te automatic test equipment is future. All metal huosing havin ground can assure best shi minimize EMI radiation. He capability is also available

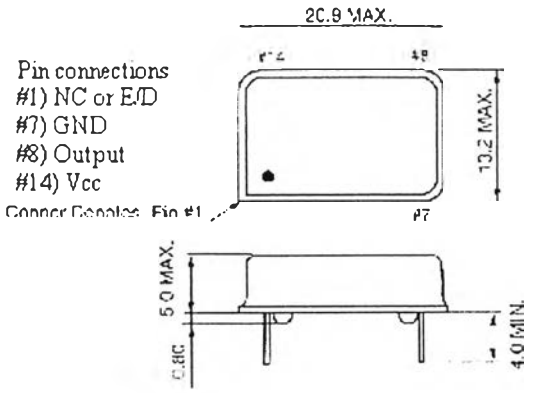
Specifications

Operating temp.	0°C to +70°C
Storage temp.	-40 to +100°C
Supply voltage	5.0V ±0.5Volt DC
E/D function	#1 open - #14 active #1 >2.2V - #14 active #1 < 0.8V - #14 HighZ

Features

- 50pF Hcmos load for 1M 106MHz
- Hcmos/TTL compatible c
- Tri-state Enable/disable
- Industry standard lead sp

Parameters	Conditions	Specifications		
Type		QC-OS-8	QC-OS-8T	QC-OS-8TV
Frequency range	All conditions	1.00 ~ 106.00	1.00 ~ 106.00	1.00 ~ 106.00
Frequency stability	All conditions	±25 (A) ±50 (B) ±100 (C)	±25 (A) ±50 (B) ±100 (C)	±25 (A) ±50 (B) ±100 (C)
Output voltage	Voh Vol	2.4 min / Vdd -0.5 min. 0.4 max. / 0.5 max.		
Output load	All conditions	10 15	10 15	10 50
Rise & fall time	Hcmos-Cl max	8 max.		6 max.
Current consumption	1.00 ~ 25MHz 25.0 ~ 40MHz 40.0 ~ 70MHz 70 ~ 106MHz	20 30 40 55		25 35 50 60
Output symmetry		40 : 60		



Pin connections
#1) NC or E/D
#7) GND
#8) Output
#14) Vcc

ประวัติผู้เขียน

นาย ราชันย์ สุรเณร เกิดวันที่ 27 ธันวาคม พ.ศ. 2514 ที่ อำเภอน้ำพอง จังหวัด ขอนแก่น สำเร็จการศึกษาปริญญาตรีวิศวกรรมศาสตร์บัณฑิต สาขาเทคโนโลยีการวัดคุมทางอุตสาหกรรม จากสถาบันเทคโนโลยีพระจอมเกล้าเจ้าคุณทหารลาดกระบังในปีการศึกษา 2538 ศึกษาต่อระดับปริญญาโท ที่ ภาควิชานิวเคลียร์เทคโนโลยี คณะวิศวกรรมศาสตร์ จุฬาลงกรณ์มหาวิทยาลัย ปัจจุบันทำงาน ตำแหน่ง วิศวกร แผนกซ่อมบำรุง ที่ บริษัท ไทยยูนีค จำกัด